

NTGS4141N, NVGS4141N

MOSFET – Power, Single, N-Channel, TSOP-6 30 V, 7.0 A

Features

- Low $R_{DS(on)}$
- Low Gate Charge
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Pb-Free Package is Available

Applications

- Load Switch
- Notebook PC
- Desktop PC

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	30	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	5.0	A
		$T_A = 85^\circ\text{C}$	3.6	
	$t \leq 10$ s	$T_A = 25^\circ\text{C}$	7.0	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.0	W
		$t \leq 10$ s	2.0	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	3.5	A
		$T_A = 85^\circ\text{C}$	2.5	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	0.5	W
Pulsed Drain Current	$t_p = 10$ μs , $V_{GS}=10\text{V}$	I_{DM}	45	A
Pulsed Drain Current	$t_p = 30$ μs , $V_{GS}=5\text{V}$	I_D	30	A
Operating Junction and Storage Temperature		T_J , T_{STG}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	2.0	A
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 30$ V, $I_L = 10.4$ A, $V_{GS} = 10$ V, $L = 1.0$ mH, $R_G = 25$ Ω)		EAS	54	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	62.5	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	248	

1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

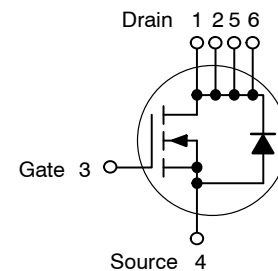


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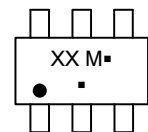
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	21.5 m Ω @ 10 V	7.0 A
	30 m Ω @ 4.5 V	

N-Channel



TSOP-6
CASE 318G
STYLE 1

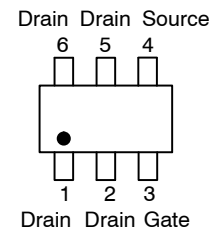
MARKING DIAGRAM



XX = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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2. Surface-mounted on FR4 board using the minimum recommended pad size
(Cu area = 0.0773 in sq).

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			18.4		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25°C		1.0	μA
			T _J = 125°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0		3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			5.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.0 A		21.5	25	mΩ
		V _{GS} = 4.5 V, I _D = 6.0 A		30	35	
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 7.0 A		30		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 24 V		560		pF
Output Capacitance	C _{OSS}			115		
Reverse Transfer Capacitance	C _{RSS}			75		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 7.0 A		12		nC
Threshold Gate Charge	Q _{G(TH)}			0.85		
Gate-to-Source Charge	Q _{GS}			1.9		
Gate-to-Drain Charge	Q _{GD}			3.0		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 7.0 A		6.0		nC
Threshold Gate Charge	Q _{G(TH)}			0.8		
Gate-to-Source Charge	Q _{GS}			1.85		
Gate-to-Drain Charge	Q _{GD}			3.0		
Gate Resistance	R _G			2.8		Ω

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 24 V, I _D = 7.0 A, R _G = 3.0 Ω		6.0		ns
Rise Time	t _r			15		
Turn-Off Delay Time	t _{d(OFF)}			18		
Fall Time	t _f			4.0		

DRAIN - SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2.0 A	T _J = 25°C	0.78	1.0	V
			T _J = 125°C	0.63		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V dI _S /dt = 100 A/μs, I _S = 2.0 A		15		ns
Charge Time	t _a			9.0		
Discharge Time	t _b			6.0		
Reverse Recovery Charge	Q _{RR}			8.0		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES

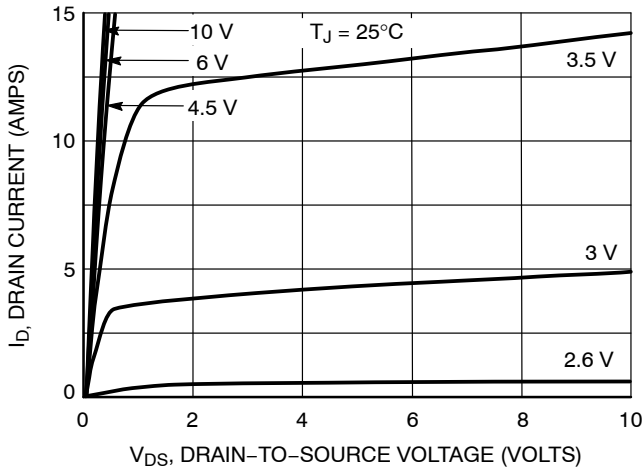


Figure 1. On-Region Characteristics

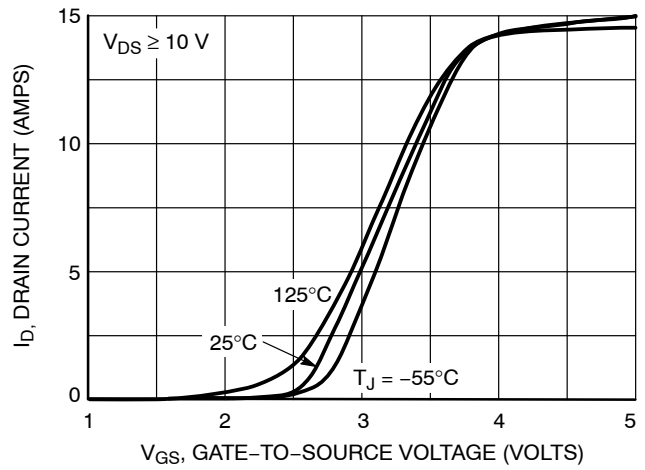


Figure 2. Transfer Characteristics

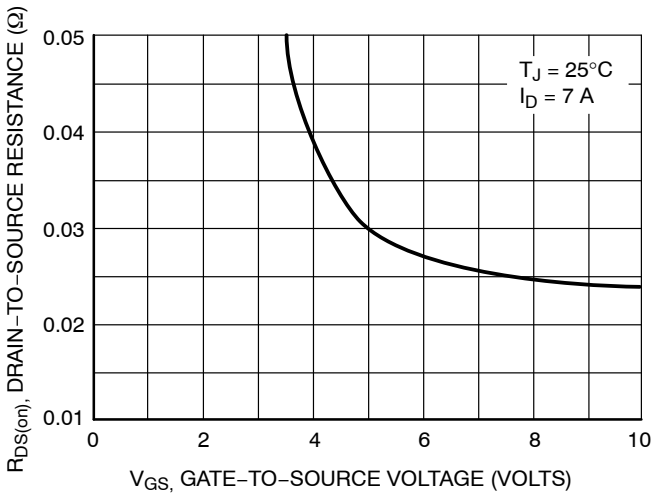


Figure 3. On-Resistance vs. Gate-to-Source Voltage

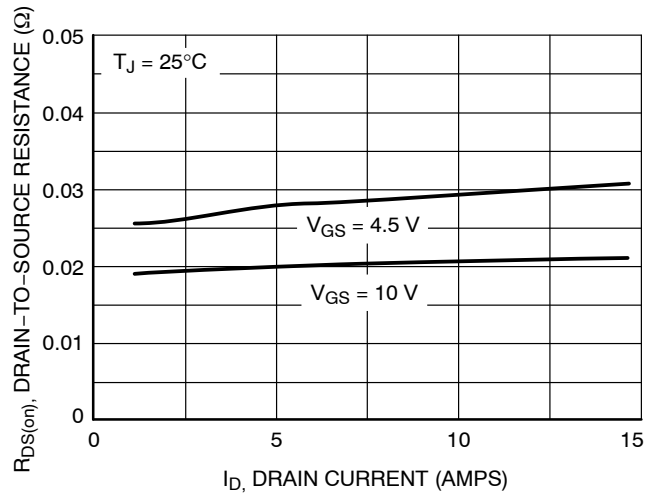


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

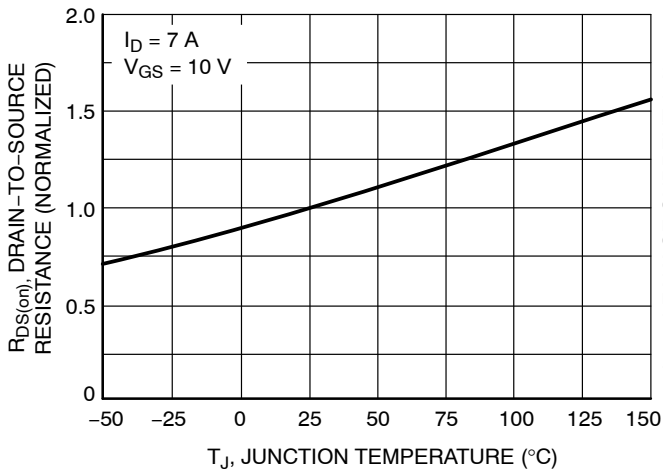


Figure 5. On-Resistance Variation with Temperature

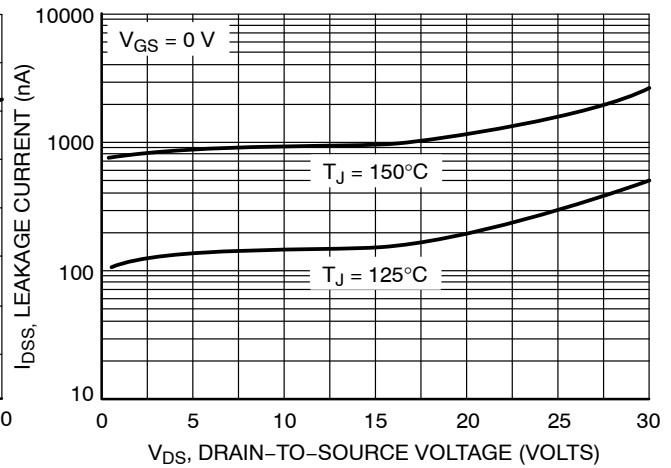
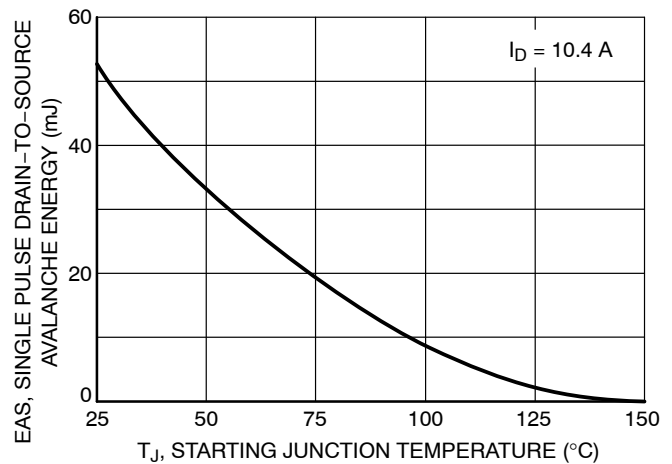
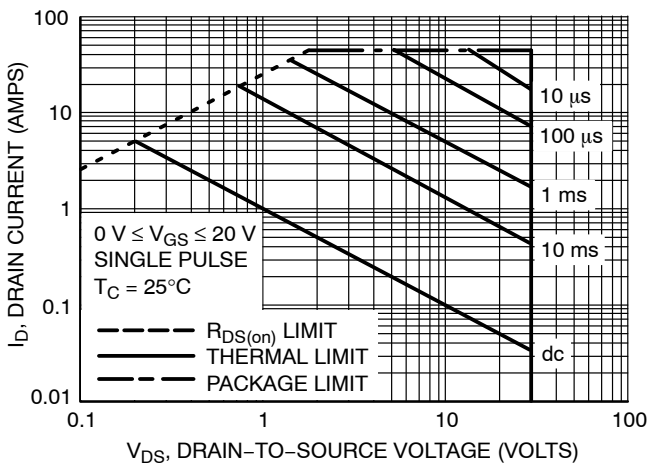
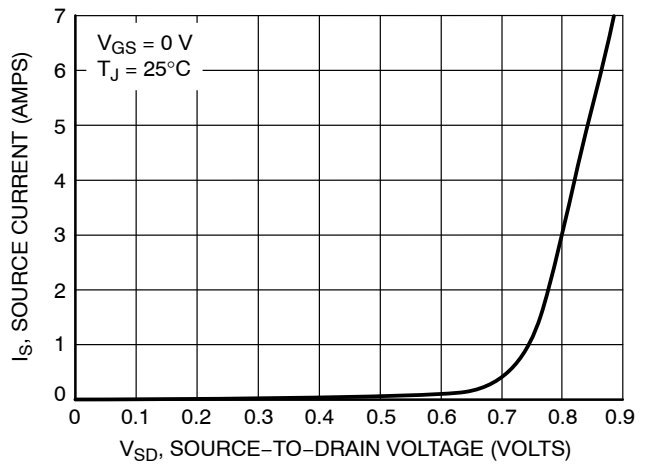
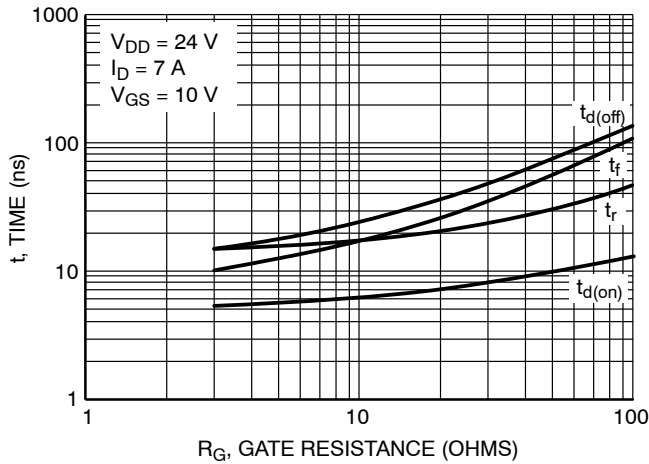
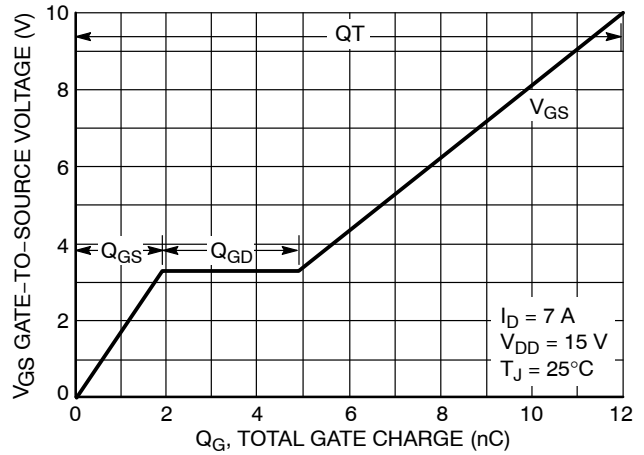
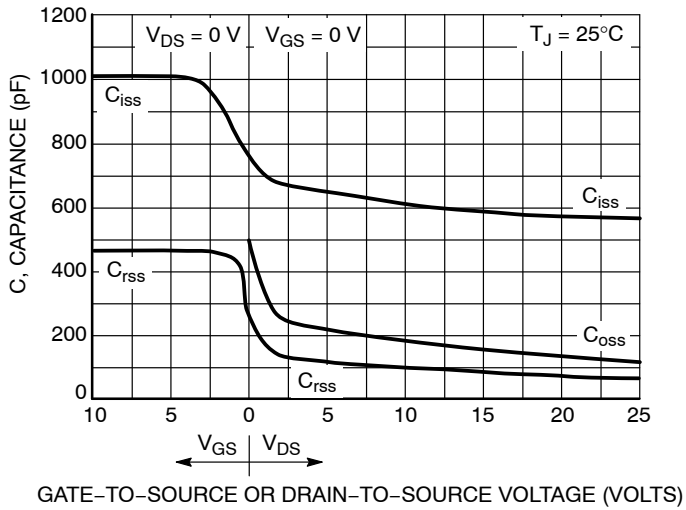


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTGS4141N, NVGS4141N

TYPICAL PERFORMANCE CURVES



NTGS4141N, NVGS4141N

TYPICAL PERFORMANCE CURVES

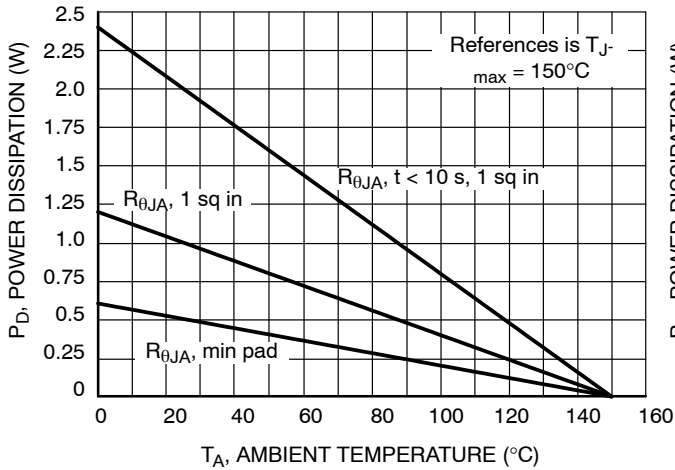


Figure 13. Maximum Power Derating Chart

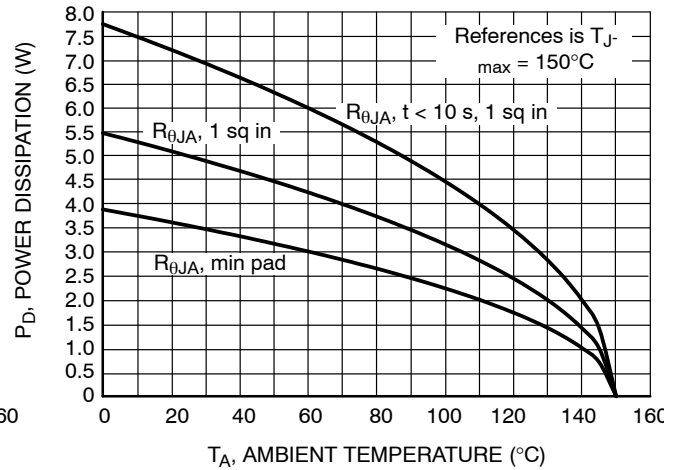


Figure 14. Current Derating Chart

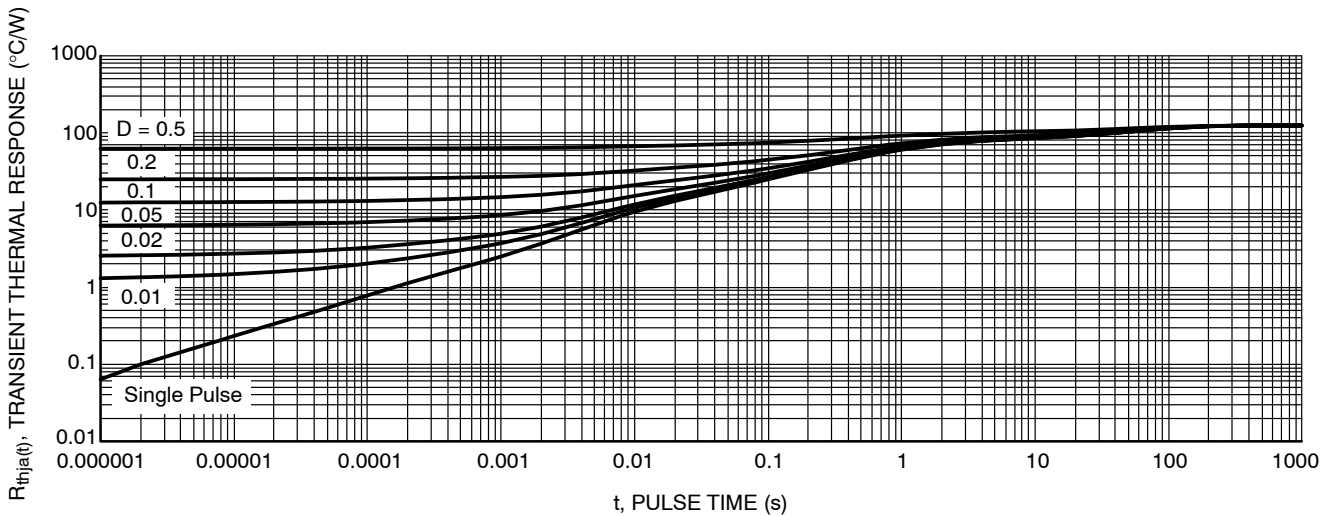


Figure 15. Thermal Response

Table 1. ORDERING INFORMATION

Part Number	Marking (XX)	Package	Shipping [†]
NTGS4141NT1	S4	TSOP-6	3000 / Tape & Reel
NTGS4141NT1G	S4	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NVGS4141NT1G	VS4	TSOP-6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



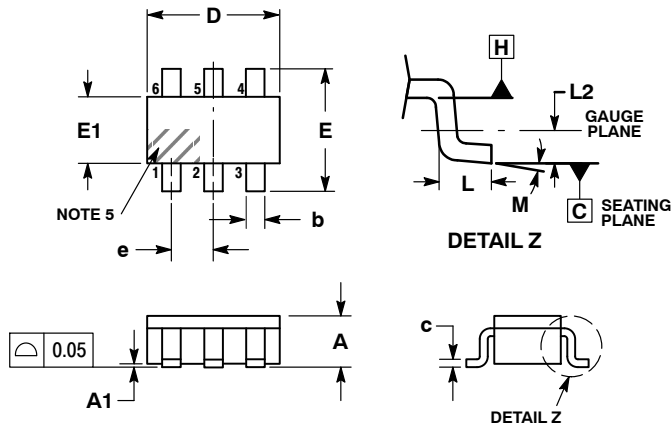
SCALE 2:1

TSOP-6

CASE 318G-02

ISSUE V

DATE 12 JUN 2012



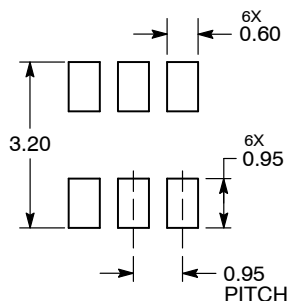
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

- | | | | | | |
|--|--|---|---|---|--|
| <p>STYLE 1:</p> <p>PIN 1. DRAIN</p> <p>2. DRAIN</p> <p>3. GATE</p> <p>4. SOURCE</p> <p>5. DRAIN</p> <p>6. DRAIN</p> | <p>STYLE 2:</p> <p>PIN 1. EMITTER 2</p> <p>2. BASE 1</p> <p>3. COLLECTOR 1</p> <p>4. EMITTER 1</p> <p>5. BASE 2</p> <p>6. COLLECTOR 2</p> | <p>STYLE 3:</p> <p>PIN 1. ENABLE</p> <p>2. N/C</p> <p>3. R BOOST</p> <p>4. Vz</p> <p>5. V in</p> <p>6. V out</p> | <p>STYLE 4:</p> <p>PIN 1. N/C</p> <p>2. V in</p> <p>3. NOT USED</p> <p>4. GROUND</p> <p>5. ENABLE</p> <p>6. LOAD</p> | <p>STYLE 5:</p> <p>PIN 1. EMITTER 2</p> <p>2. BASE 2</p> <p>3. COLLECTOR 1</p> <p>4. EMITTER 1</p> <p>5. BASE 1</p> <p>6. COLLECTOR 2</p> | <p>STYLE 6:</p> <p>PIN 1. COLLECTOR</p> <p>2. COLLECTOR</p> <p>3. BASE</p> <p>4. EMITTER</p> <p>5. COLLECTOR</p> <p>6. COLLECTOR</p> |
| <p>STYLE 7:</p> <p>PIN 1. COLLECTOR</p> <p>2. COLLECTOR</p> <p>3. BASE</p> <p>4. N/C</p> <p>5. COLLECTOR</p> <p>6. EMITTER</p> | <p>STYLE 8:</p> <p>PIN 1. Vbus</p> <p>2. D(in)</p> <p>3. D(in)+</p> <p>4. D(out)+</p> <p>5. D(out)</p> <p>6. GND</p> | <p>STYLE 9:</p> <p>PIN 1. LOW VOLTAGE GATE</p> <p>2. DRAIN</p> <p>3. SOURCE</p> <p>4. DRAIN</p> <p>5. DRAIN</p> <p>6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:</p> <p>PIN 1. D(OUT)+</p> <p>2. GND</p> <p>3. D(OUT)-</p> <p>4. D(IN)-</p> <p>5. VBUS</p> <p>6. D(IN)+</p> | <p>STYLE 11:</p> <p>PIN 1. SOURCE 1</p> <p>2. DRAIN 2</p> <p>3. DRAIN 2</p> <p>4. SOURCE 2</p> <p>5. GATE 1</p> <p>6. DRAIN 1/GATE 2</p> | <p>STYLE 12:</p> <p>PIN 1. I/O</p> <p>2. GROUND</p> <p>3. I/O</p> <p>4. I/O</p> <p>5. VCC</p> <p>6. I/O</p> |
| <p>STYLE 13:</p> <p>PIN 1. GATE 1</p> <p>2. SOURCE 2</p> <p>3. GATE 2</p> <p>4. DRAIN 2</p> <p>5. SOURCE 1</p> <p>6. DRAIN 1</p> | <p>STYLE 14:</p> <p>PIN 1. ANODE</p> <p>2. SOURCE</p> <p>3. GATE</p> <p>4. CATHODE/DRAIN</p> <p>5. CATHODE/DRAIN</p> <p>6. CATHODE/DRAIN</p> | <p>STYLE 15:</p> <p>PIN 1. ANODE</p> <p>2. SOURCE</p> <p>3. GATE</p> <p>4. DRAIN</p> <p>5. N/C</p> <p>6. CATHODE</p> | <p>STYLE 16:</p> <p>PIN 1. ANODE/CATHODE</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. COLLECTOR</p> <p>5. ANODE</p> <p>6. CATHODE</p> | <p>STYLE 17:</p> <p>PIN 1. EMITTER</p> <p>2. BASE</p> <p>3. ANODE/CATHODE</p> <p>4. ANODE</p> <p>5. CATHODE</p> <p>6. COLLECTOR</p> | |

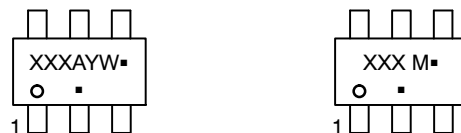
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC

STANDARD

- | | |
|--|---|
| <p>XXX = Specific Device Code</p> <p>A = Assembly Location</p> <p>Y = Year</p> <p>W = Work Week</p> <p>■ = Pb-Free Package</p> | <p>XXX = Specific Device Code</p> <p>M = Date Code</p> <p>■ = Pb-Free Package</p> |
|--|---|

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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