

CM1213A, SZCM1213A

1, 2 and 4-Channel Low Capacitance ESD Protection Arrays

Product Description

The CM1213A family of diode arrays has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N , offering two advantages. First, it protects the V_{CC} rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1213A will protect against ESD pulses up to 12 kV per the IEC 61000-4-2 standard.

Features

- One, Two, and Four Channels of ESD Protection
Note: For 6 and 8-channel Devices, See the CM1213 Datasheet
- Provides ESD Protection to IEC61000-4-2 Level 4
 - ◆ ± 12 kV Contact Discharge
- Low Channel Input Capacitance of 0.85 pF Typical
- Minimal Capacitance Change with Temperature and Voltage
- Channel Input Capacitance Matching of 0.02 pF Typical is Ideal for Differential Signals
- Each CH (I/O) Pin Can Withstand Over 1000 ESD Strikes*
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

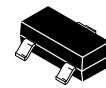
- USB2.0 Ports at 480 Mbps in Desktop PCs, Notebooks and Peripherals
- IEEE1394 Firewire® Ports at 400 Mbps/800 Mbps
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High-Speed Data Line ESD Protection

*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to ± 8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

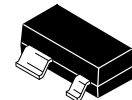


ON Semiconductor®

www.onsemi.com



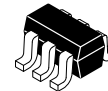
SOT23-3
SO SUFFIX
CASE 318



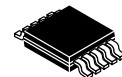
SOT-143
SR SUFFIX
CASE 318A



SC-74
SO SUFFIX
CASE 318F

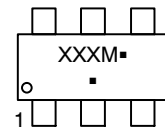
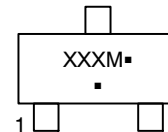


SC70-6
S7 SUFFIX
CASE 419AD

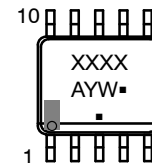


MSOP-10
MR SUFFIX
CASE 846AE

MARKING DIAGRAMS



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

CM1213A, SZCM1213A

BLOCK DIAGRAM

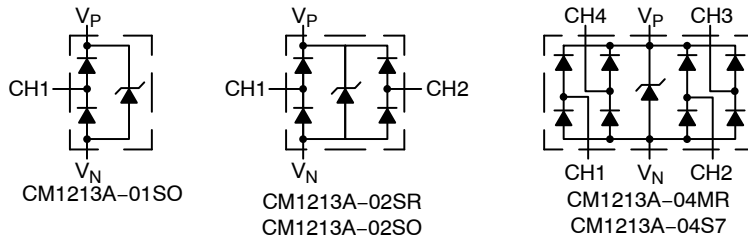


Table 1. ORDERING INFORMATION

Device	Marking	Package	Shipping†
CM1213A-01SO	231	SOT23-3 (Pb-Free)	3,000 / Tape & Reel
SZCM1213A-01SO*			
CM1213A-02SR	D232	SOT143-4 (Pb-Free)	3,000 / Tape & Reel
SZCM1213A-02SR*			
CM1213A-02SO	233	SC-74 (Pb-Free)	3,000 / Tape & Reel
CM1213A-04S7	D38	SC70-6 (Pb-Free)	3,000 / Tape & Reel
CM1213A-04MR	D237	MSOP-10 (Pb-Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

CM1213A, SZCM1213A

Table 2. PIN DESCRIPTIONS

1-Channel, 3-Lead SOT23-3 Package (CM1213A-01SO)			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	V _P	PWR	Positive Voltage Supply Rail
3	V _N	GND	Negative Voltage Supply Rail

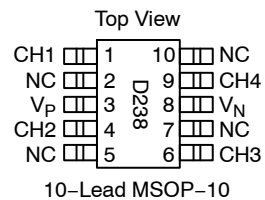
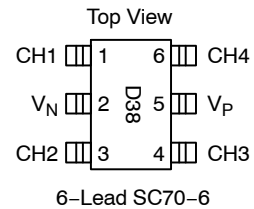
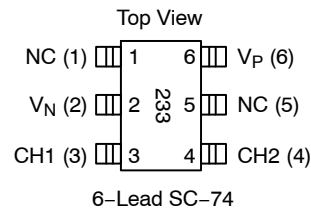
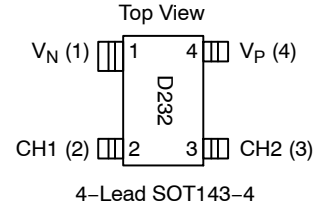
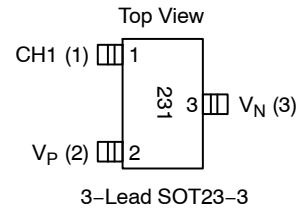
2-Channel, 4-Lead SOT143-4 Package (CM1213A-02SR)			
Pin	Name	Type	Description
1	V _N	GND	Negative Voltage Supply Rail
2	CH1	I/O	ESD Channel
3	CH2	I/O	ESD Channel
4	V _P	PWR	Positive Voltage Supply Rail

2-Channel, SC-74 Package (CM1213A-02SO)			
Pin	Name	Type	Description
1	NC	-	No Connect
2	V _N	GND	Negative Voltage Supply Rail
3	CH1	I/O	ESD Channel
4	CH2	I/O	ESD Channel
5	NC	-	No Connect
6	V _P	PWR	Positive Voltage Supply Rail

4-Channel, 6-Lead SC70-6 (CM1213A-04S7)			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	V _N	GND	Negative Voltage Supply Rail
3	CH2	I/O	ESD Channel
4	CH3	I/O	ESD Channel
5	V _P	PWR	Positive Voltage Supply Rail
6	CH4	I/O	ESD Channel

4-Channel, 10-Lead MSOP-10 Package (CM1213A04MR)			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	NC	-	No Connect
3	V _P	PWR	Positive Voltage Supply Rail
4	CH2	I/O	ESD Channel
5	NC	-	No Connect
6	CH3	I/O	ESD Channel
7	NC	-	No Connect
8	V _N	GND	Negative Voltage Supply Rail
9	CH4	I/O	ESD Channel
10	NC	-	No Connect

PACKAGE/PINOUT DIAGRAMS



CM1213A, SZCM1213A

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Supply Voltage ($V_P - V_N$)	5.5	V
Operating Temperature Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	$(V_N - 0.5)$ to $(V_P + 0.5)$	V
Package Power Rating SOT23-3, SOT143-4, SC-74, and SC70-6 Packages MSOP-10 Package	225 400	mW
ESD IEC 61000-4-2 Contact IEC 61000-4-2 Air ISO 10605 330 pF / 330 Ω Contact ISO 10605 330 pF / 2 k Ω Contact ISO 10605 150 pF / 2 k Ω Contact	± 12 ± 12 ± 9 ± 22 ± 25	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_P (V_{RWM})	Operating Supply Voltage ($V_P - V_N$)			3.3	5.5	V
I_P	Operating Supply Current	V_P pin to V_N pin, ($V_P = 3.3$ V, $V_N = 0$ V)			8.0	μ A
I_{LEAK}	Channel Leakage Current	CH pin to V_N pin, $T_A = 25^\circ\text{C}$; ($V_P = 5$ V, $V_N = 0$ V)		0.1	1.0	μ A
V_F	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 8$ mA; $T_A = 25^\circ\text{C}$	0.60 0.60	0.80 0.80	0.95 0.95	V
V_{BR}	Breakdown Voltage	$I_T = 10$ mA, CH pin to V_N pin	6.5		9.0	V
C_{IN}	Channel Input Capacitance	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V (Note 2)		0.85	1.2	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V (Note 2)		0.02		pF
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	$T_A = 25^\circ\text{C}$, $I_{PP} = 1$ A, $t_P = 8/20$ μ s (Note 2)		+10 -1.7		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	$I_{PP} = 1$ A, $t_P = 8/20$ μ s Any I/O pin to Ground (Note 2)		0.9 0.5		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- All parameters specified at $T_A = 25^\circ\text{C}$ unless otherwise noted.
- Standard IEC 61000-4-2 with $C_{Discharge} = 150$ pF, $R_{Discharge} = 330$ Ω , $V_P = 3.3$ V, V_N grounded.
- These measurements performed with no external capacitor on V_P (V_P floating).

CM1213A, SZCM1213A

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

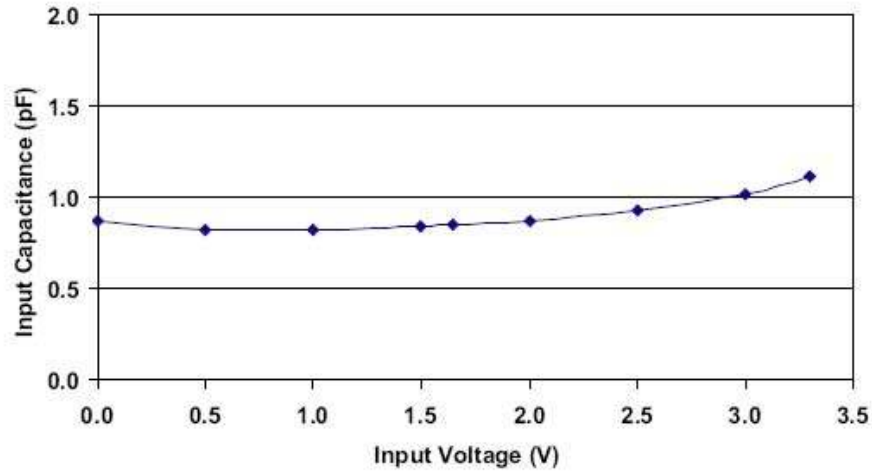


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
($f = 1$ MHz, $V_P = 3.3$ V, $V_N = 0$ V, $0.1 \mu\text{F}$ Chip Capacitor between V_P and V_N , 25°C)

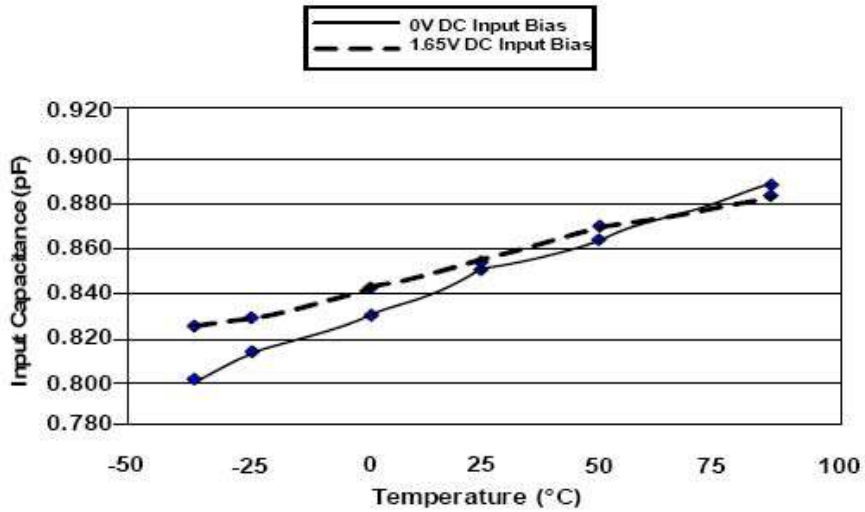


Figure 2. Typical Variation of C_{IN} vs. Temp
($f = 1$ MHz, $V_{IN} = 30$ mV, $V_P = 3.3$ V, $V_N = 0$ V, $0.1 \mu\text{F}$ Chip Capacitor between V_P and V_N)

CM1213A, SZCM1213A

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

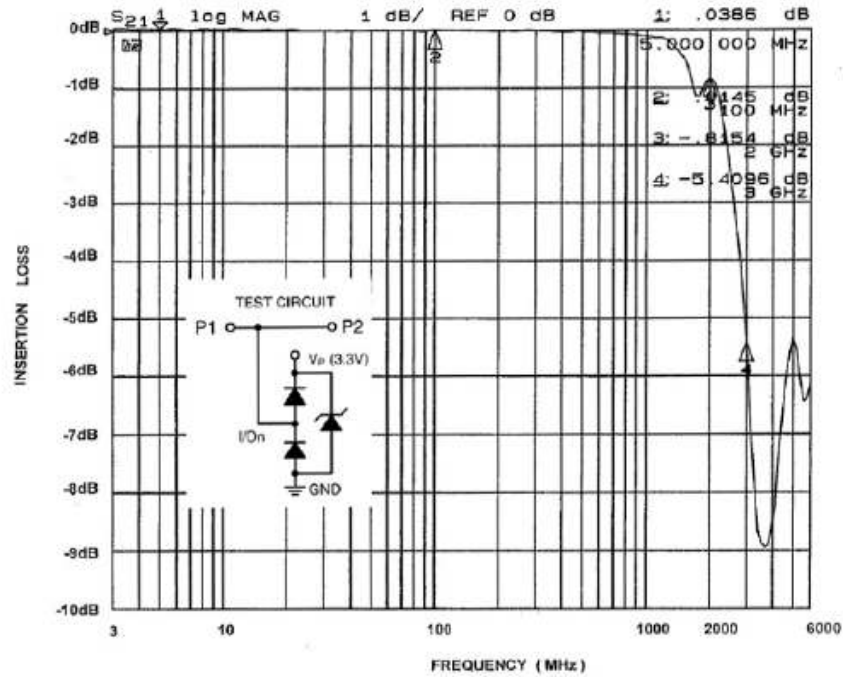


Figure 3. Insertion Loss (S21) vs. Frequency (0 V DC Bias, $V_p=3.3$ V)

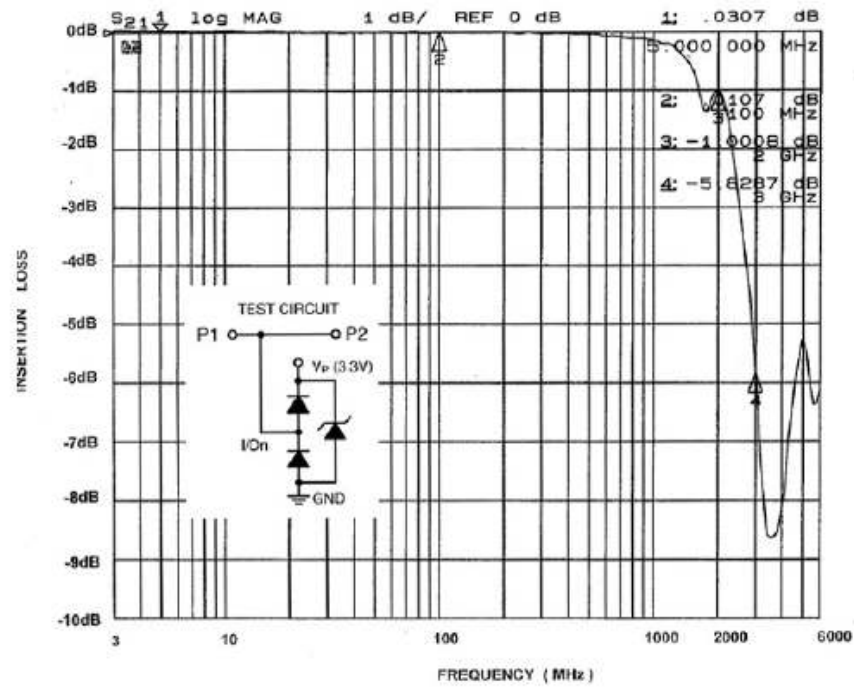


Figure 4. Insertion Loss (S21) vs. Frequency (2.5 V DC Bias, $V_p=3.3$ V)

APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2 . The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd Voltage Drop of } D_1 + V_{\text{SUPPLY}} + L_1 \times d(I_{\text{ESD}}) / dt + L_2 \times d(I_{\text{ESD}}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here $d(I_{\text{ESD}})/dt$ can be approximated by $\Delta I_{\text{ESD}}/\Delta t$, or $30/(1 \times 10^{-9})$. So just 10 nH of series inductance (L_1 and L_2 combined) will lead to a 300 V increment in V_{CL} !

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1213A has an integrated Zener diode between V_P and V_N . This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL} , especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22 μF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also ON Semiconductor Application Note “Design Considerations for ESD Protection”, in the Applications section.

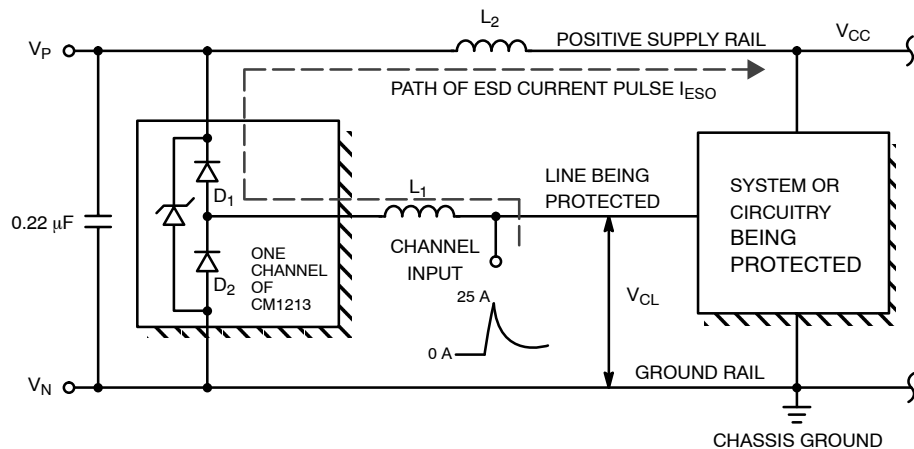
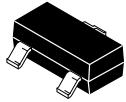


Figure 5. Application of Positive ESD Pulse between Input Channel and Ground

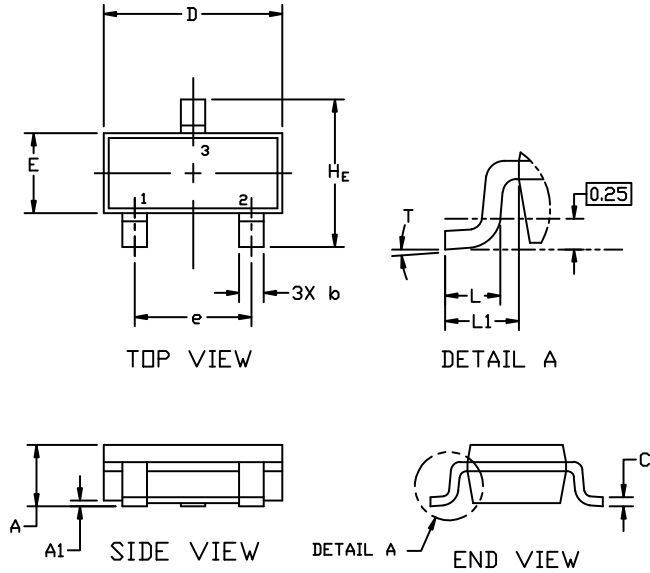
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23 (TO-236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

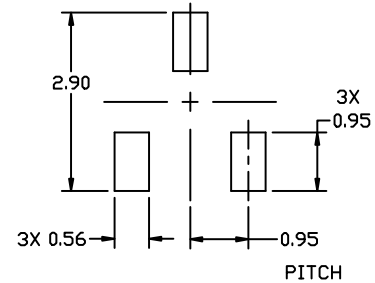
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H _E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42226B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-23 (TO-236)	PAGE 1 OF 2

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



**SOT-23 (TO-236)
CASE 318
ISSUE AT**

DATE 01 MAR 2023

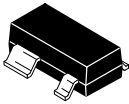
- | | | | | | |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:
CANCELLED | STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE | | |
| STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE | STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE | STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE | STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE |
| STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE | STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE | STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE | STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE | STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE-ANODE | STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE |
| STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT | STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE | STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION |
| STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE | STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE | | | | |

DOCUMENT NUMBER:	98ASB42226B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-23 (TO-236)	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

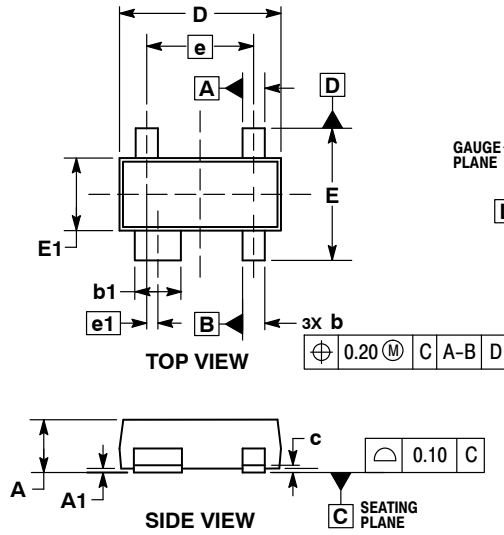
ON Semiconductor®



SCALE 4:1

SOT-143 CASE 318A-06 ISSUE U

DATE 07 SEP 2011

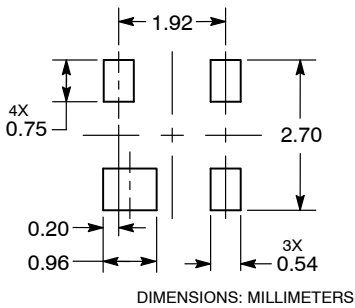


NOTES:

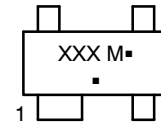
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, AND GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.12
A1	0.01	0.15
b	0.30	0.51
b1	0.76	0.94
c	0.08	0.20
D	2.80	3.05
E	2.10	2.64
E1	1.20	1.40
e	1.92 BSC	
e1	0.20 BSC	
L	0.35	0.70
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- | | | | | | |
|---|---|---|---|--|--|
| <p>STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. EMITTER
4. BASE</p> | <p>STYLE 2:
PIN 1. SOURCE
2. DRAIN
3. GATE 1
4. GATE 2</p> | <p>STYLE 3:
PIN 1. GROUND
2. SOURCE
3. INPUT
4. OUTPUT</p> | <p>STYLE 4:
PIN 1. OUTPUT
2. GROUND
3. GROUND
4. INPUT</p> | <p>STYLE 5:
PIN 1. SOURCE
2. DRAIN
3. GATE 1
4. SOURCE</p> | <p>STYLE 6:
PIN 1. GND
2. RF IN
3. VREG
4. RF OUT</p> |
| <p>STYLE 7:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SOURCE</p> | <p>STYLE 8:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. N/C</p> | <p>STYLE 9:
PIN 1. GND
2. IOUT
3. VCC
4. VREF</p> | <p>STYLE 10:
PIN 1. DRAIN
2. N/C
3. SOURCE
4. GATE</p> | <p>STYLE 11:
PIN 1. SOURCE
2. GATE 1
3. GATE 2
4. DRAIN</p> | |

DOCUMENT NUMBER:	98ASB42227B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-143	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

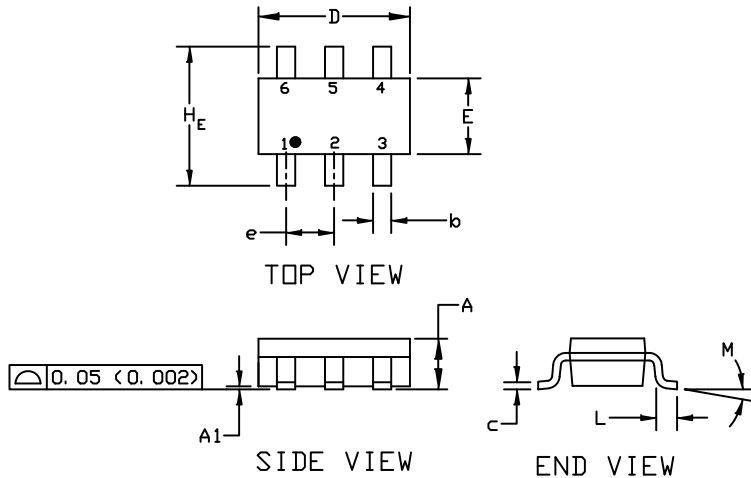
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

SC-74
CASE 318F
ISSUE P

DATE 07 OCT 2021

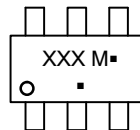


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
HE	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0*	---	10*	0*	---	10*

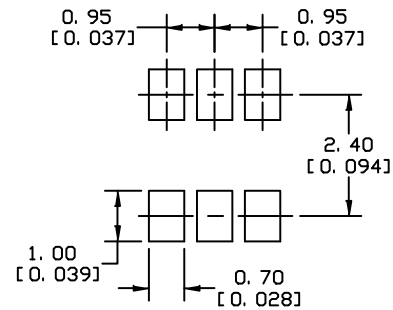
GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

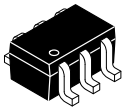
SOLDERING FOOTPRINT

- | | | | | | |
|--|---|--|---|--|--|
| <p>STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE</p> | <p>STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE</p> | <p>STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1</p> | <p>STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3</p> | <p>STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4</p> | <p>STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE</p> |
| <p>STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1</p> | <p>STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1</p> | <p>STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

DOCUMENT NUMBER:	98ASB42973B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-74	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

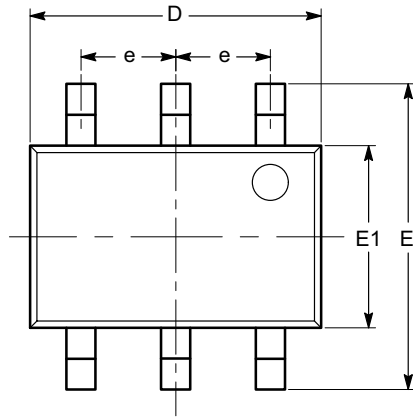
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



1

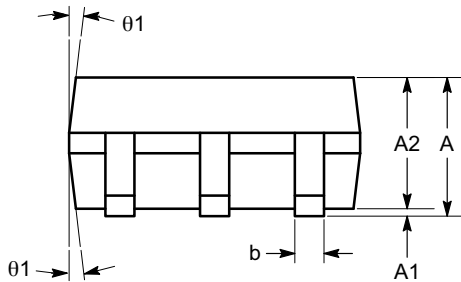
SC-88 (SC-70 6 Lead), 1.25x2
CASE 419AD
ISSUE A

DATE 07 JUL 2010

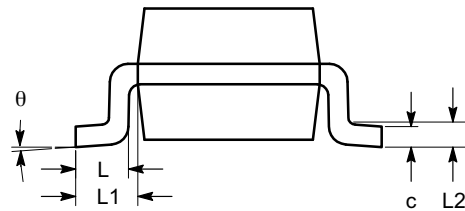


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
θ	0°		8°
θ_1	4°		10°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

DOCUMENT NUMBER:	98AON34266E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-88 (SC-70 6 LEAD), 1.25X2	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

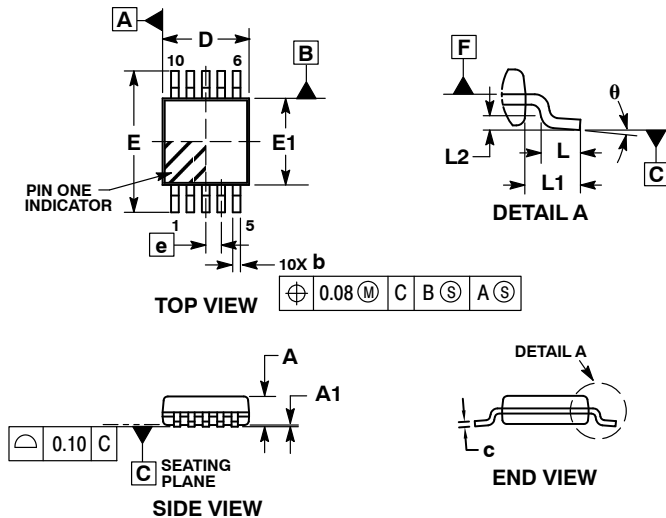
ON Semiconductor®



SCALE 1:1

MSOP10, 3x3
CASE 846AE
ISSUE A

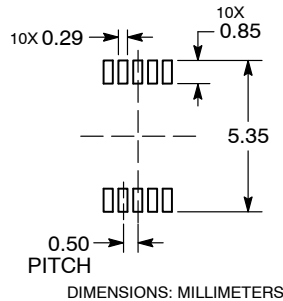
DATE 20 JUN 2017



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSIONS: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 MM IN EXCESS OF MAXIMUM MATERIAL CONDITION.
 4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 MM PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
 5. DATUMS A AND B TO BE DETERMINED AT DATUM F.
 6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

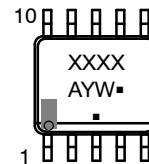
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	---	---	1.10
A1	0.00	0.05	0.15
A2	0.75	0.85	0.95
b	0.17	---	0.27
c	0.13	---	0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.50 BSC		
L	0.40	0.70	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°	---	8°

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON34098E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	MSOP10, 3X3	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales