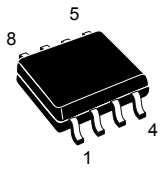
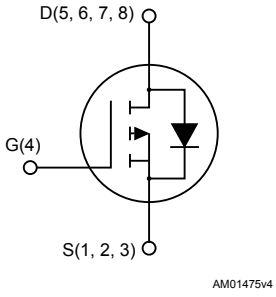
STS9P3LLH6

Datasheet

P-channel -30 V, 12 mΩ typ., -9 A, STripFET H6 Power MOSFET in an SO-8 package



SO-8



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STS9P3LLH6	-30 V	15 mΩ	-9 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STS9P3LLH6

Product summary	
Order code	STS9P3LLH6
Marking	9K3L
Package	SO-8
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_{amb} = 25°C	-9	A
	Drain current (continuous) at T_{amb} = 100°C	-5.6	
I_{DM}(2)	Drain current (pulsed)	-36	A
P_{TOT}(1)	Total power dissipation at T_{amb} = 25°C	2.7	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *This value is rated according to R_{thJA}.*
2. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}(1)	Thermal resistance, junction-to-ambient	47	°C/W

1. *When mounted on 1 inch² FR-4 board, 2 oz. Cu., t ≤ 10 s.*

2 Electrical characteristics

T_C= 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = -1 mA	-30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = -30 V			-1	µA
		V_{GS} = 0, V_{DS} = -30 V, T_C = 125 °C(1)			-10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ±20 V			-100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = -10 V, I_D = -4.5 A		12	15	mΩ
		V_{GS} = -4.5 V, I_D = -4.5 A		18.0	22.5	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = -25 V, f = 1 MHz, V_{GS} = 0 V	-	2615	-	pF
C_{oss}	Output capacitance		-	340	-	pF
C_{rss}	Reverse transfer capacitance		-	235	-	pF
Q_g	Total gate charge	V_{DD} = -15 V I_D = -9 A, V_{GS} = -4.5 V (see Figure 13. Gate charge test circuit)	-	24	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	8	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = -15 V, I_D = -4.5 A, R_G = 4.7 Ω, V_{GS} = -10 V (see Figure 12. Switching times test circuit for resistive load)	-	13.2	-	ns
t_r	Rise time		-	93	-	ns
$t_{d(off)}$	Turn-off delay time		-	50	-	ns
t_f	Fall time		-	18	-	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = -4.5 A, V_{GS} = 0	-		-1.1	V
t_{rr}	Reverse recovery time	V_{DD} = -24 V, T_J = 150 °C, I_{SD} = -4.5 A, di/dt = 100 A/µs (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	20		ns
Q_{rr}	Reverse recovery charge		-	16		nC
I_{RRM}	Reverse recovery current		-	-1.6		A

1. *Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

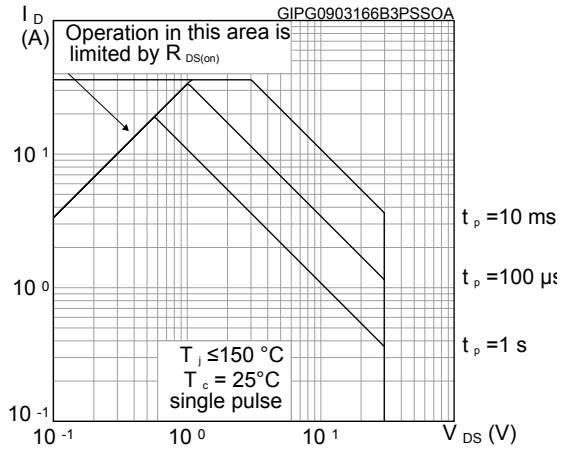


Figure 2. Thermal impedance

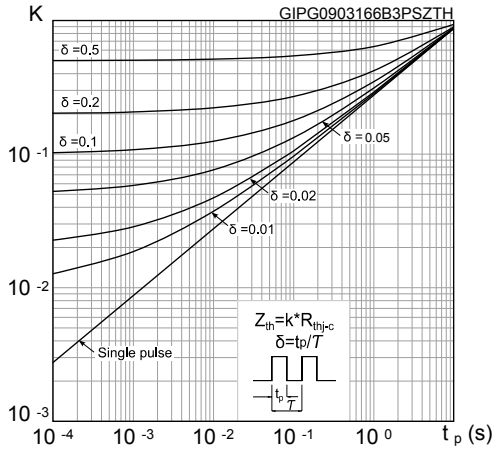


Figure 3. Output characteristics

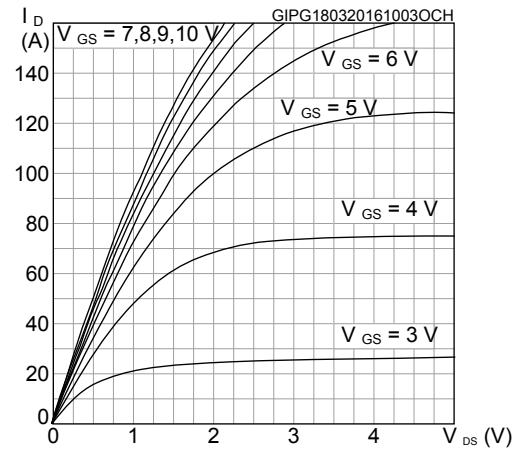


Figure 4. Transfer characteristics

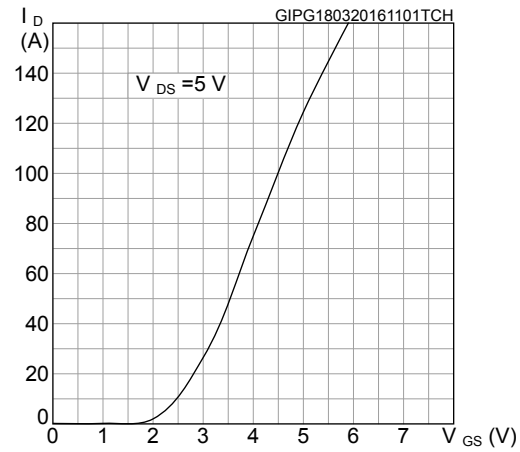


Figure 5. Gate charge vs gate-source voltage

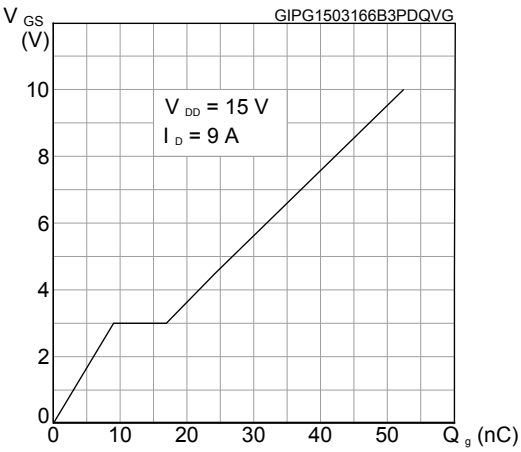


Figure 6. Static drain-source on-resistance

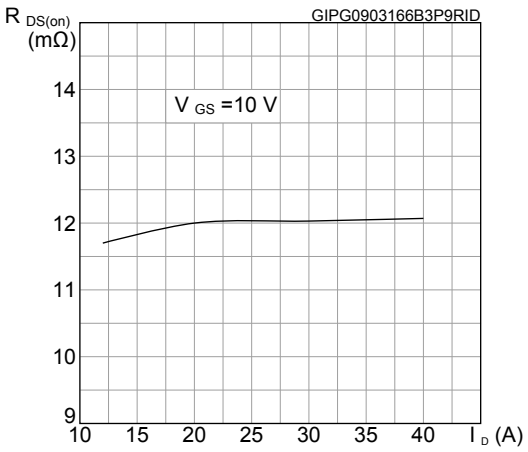


Figure 7. Capacitance variations

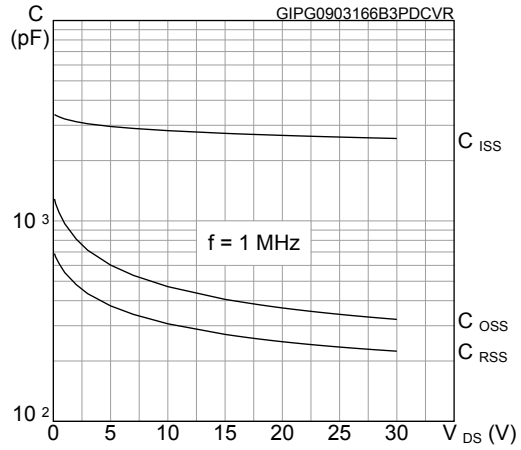


Figure 8. Normalized gate threshold voltage vs temperature

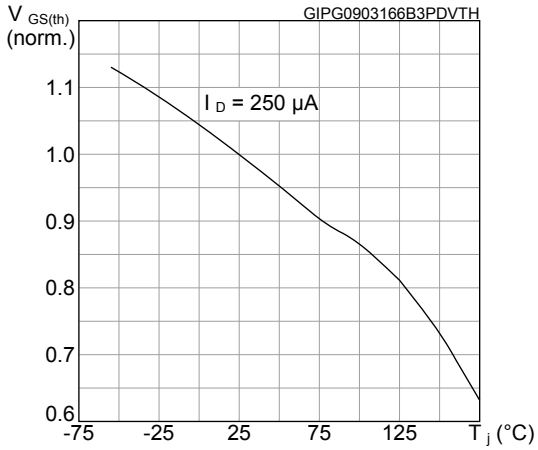


Figure 9. Normalized on-resistance vs temperature

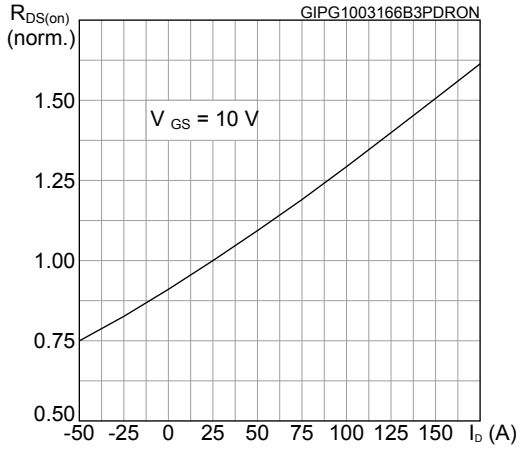


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

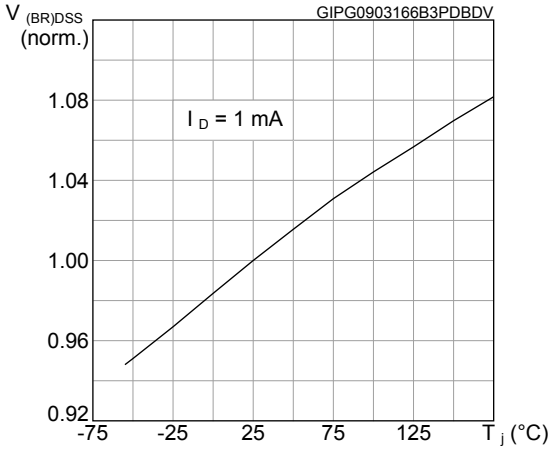
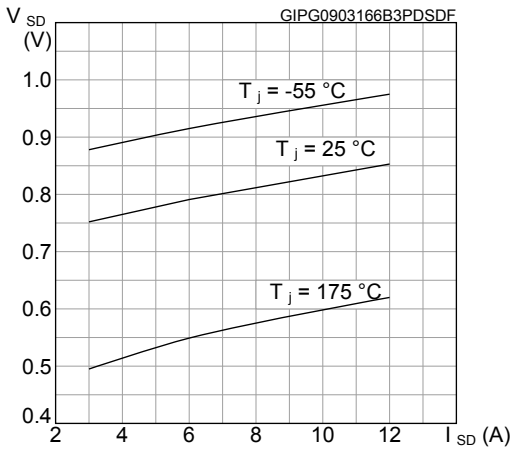


Figure 11. Source-drain diode forward characteristics



Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

3 Test circuits

Figure 12. Switching times test circuit for resistive load

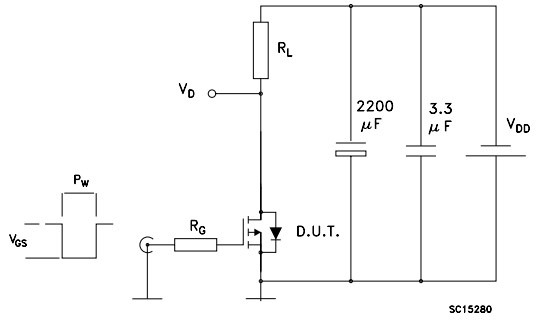


Figure 13. Gate charge test circuit

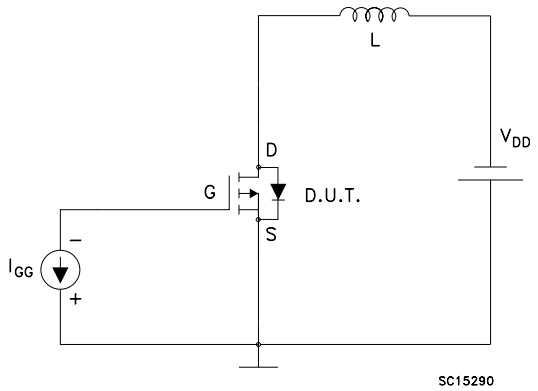
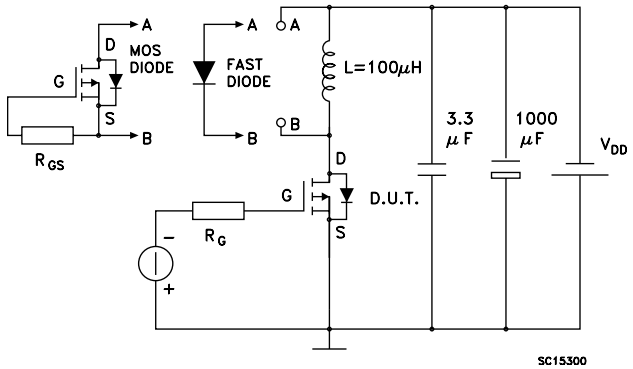


Figure 14. Test circuit for inductive load switching and diode recovery times

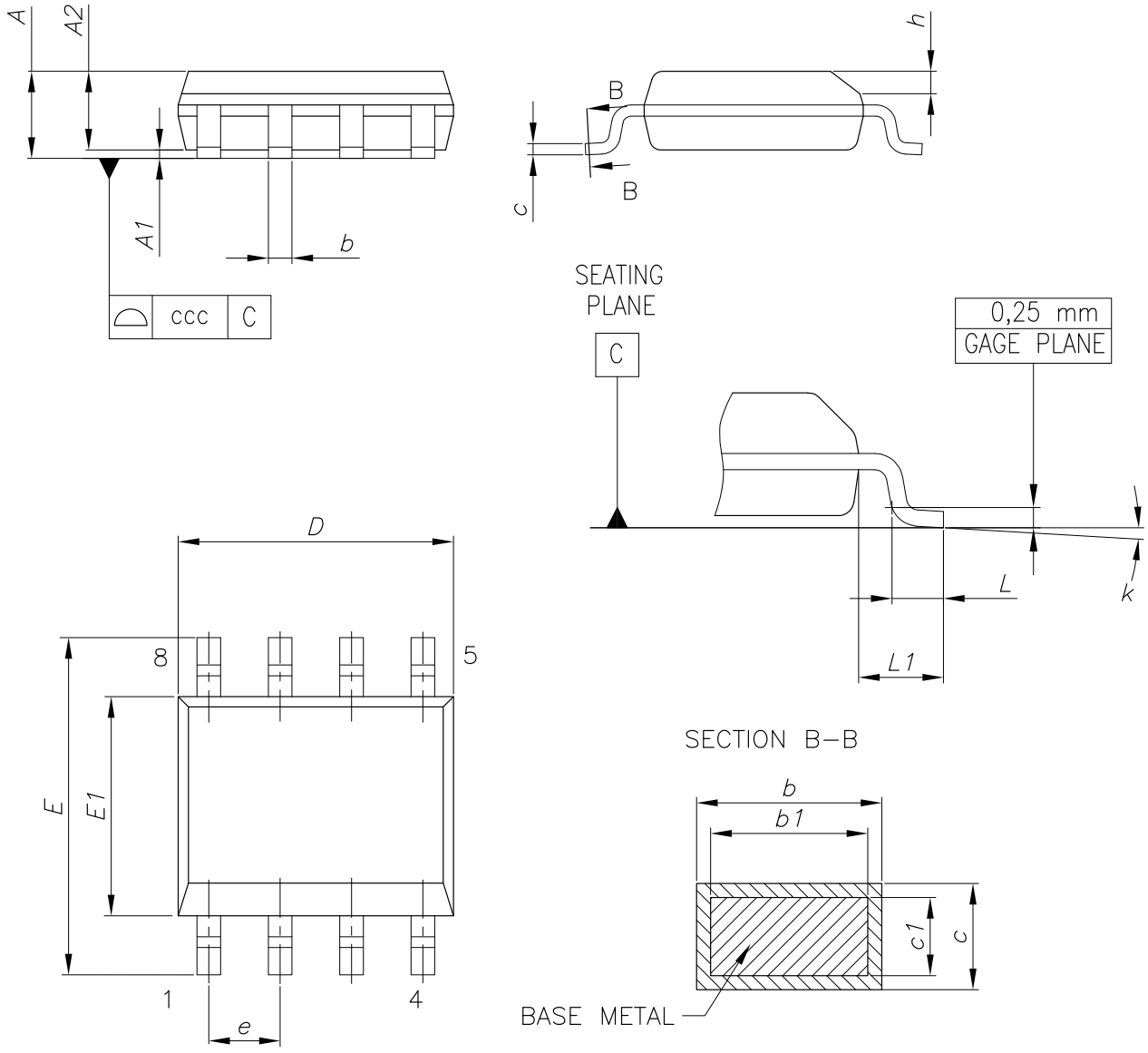


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

Figure 15. SO-8 package outline

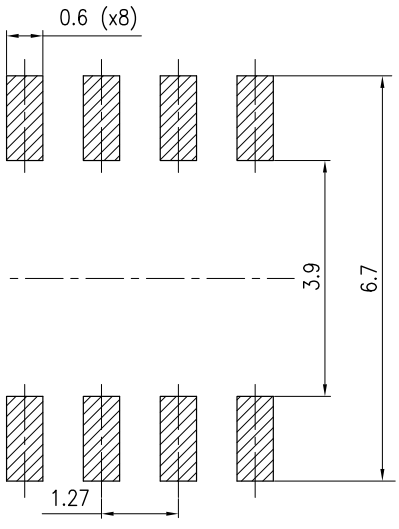


0016023_So-807_fig2_Rev10

Table 7. **SO-8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 16. **SO-8 recommended footprint (dimensions are in mm)**



0016023_So-807_footprint_Rev10

4.2 SO-8 packing information

Figure 17. **SO-8 tape and reel dimensions**

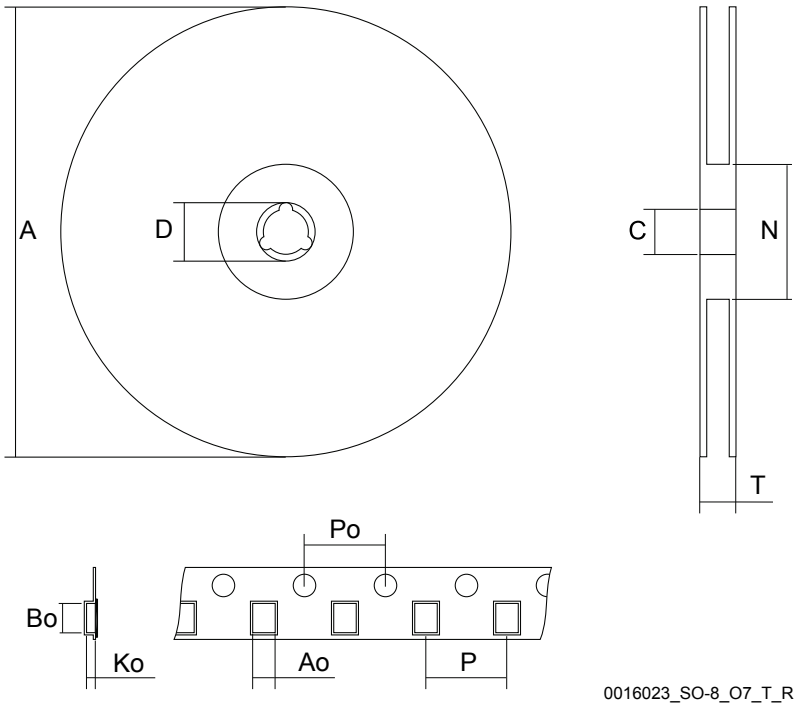


Figure 18. **Tape orientation**

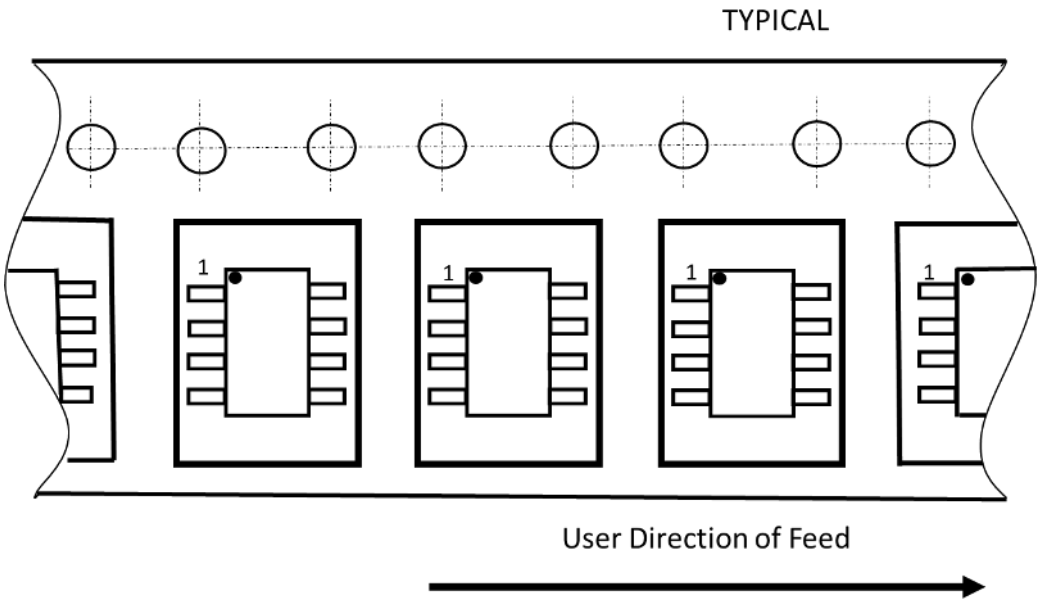


Table 8. **SO-8 tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5		6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
22-Jan-2014	1	Initial release.
15-Mar-2016	2	Modified: title and $R_{DS(on)}$ max value in cover page. Modified: *Table 4: "On/off states"*, *Table 5: "Dynamic"*, *Table 6: "Switching times"* and *Table 7: "Source drain diode"*. Minor text changes.
17-Feb-2021	3	Updated Internal schematic. Updated Section 4.2 SO-8 packing information. Minor text changes.

Contents