MIC2267

Input Current Limiting Synchronous Buck Regulator

USB Power Maximizer™

General Description

The MIC2267 is a USB Power Maximizer™ which transfers the maximum power from the limited USB current source by shaping the input current limit profile. It incorporates a high efficiency, integrated synchronous step down regulator. Internal 150mΩ switches and adjustable operating frequency allows the MIC2267 to achieve greater than 90% efficiency across a broad load range. It replaces the USB current limit switch, 5V buck regulator and minimizes capacitance for many USB applications. The adjustable frequency control can be utilized to move harmonics away from sensitive frequency bands.

The MIC2267 allows the input current limit profile to be shaped for various applications. With a current mode control with external compensation, the MIC2267 transient response can be optimized over load and output capacitance making it highly flexible for many applications.

Additional features include 1µA shutdown current, output current limit and thermal shutdown protection. The MIC2267 is available in a 12-pin 3mm x 3mm MLF® with a junction operating range from –40°C to +125°C.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

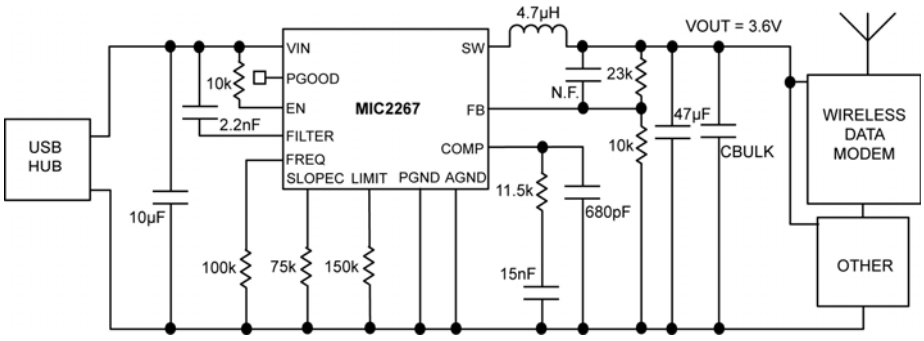
Features

- Input voltage range: 3.0V to 5.5V
- Output voltage adjustable down to 1.0V
- Up to 96% efficiency at 500mA output
- Efficiency >90% across a broad load range
- Fast transient response
- Adjustable frequency from 400kHz to 1.5MHz
- Adjustable input current limiting 100mA to over 1A
- 100% maximum duty cycle
- Fully integrated MOSFET switches
- Micropower shutdown
- Thermal shutdown and output current limit protection
- 12-pin 3mm x 3mm MLF®
- Junction temperature range: –40°C to +125°C

Applications

- USB power
- Wireless router cards
- General buck converter applications

Typical Application



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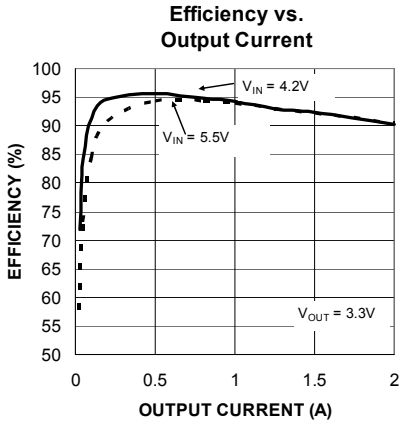


Efficiency $5V_{IN}$ to $3.3V_{OUT}$

USB Power Maximizer is a trademark of Micrel, Inc.

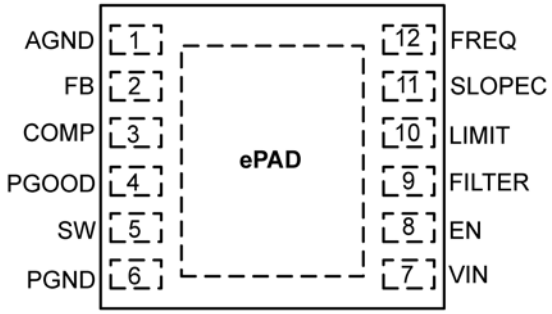
Ordering Information

Part Number	Voltage	Mark Code	Temperature Range	Package[1]
MIC2267YML	Adjustable	2267	–40°C to +125°C	12-Pin 3mm x 3mm MLF®

Note:

1. Package is GREEN RoHS compliant. Lead finish is NiPdAu. Mold compound is halogen free.

Pin Configuration



12-Pin 3mm x 3mm MLF® (ML)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	AGND	Analog Ground: The ground return for the low power blocks of the MIC2267.
2	FB	Feedback (Input): Input to the error amplifier. Connect a resistor divider between VOUT and ground to adjust the output voltage.
3	COMP	Compensation Pin: Output of the internal gm error amplifier. Place a series connected, Resistor and Capacitor to GND for external compensation.
4	PGOOD	Power Good (Output): Open drain of an N-Channel MOSFET. Connect a resistor to VIN or VOUT for power good signalling.
5	SW	Switch (Output): Internal power MOSFET output switches.
6	PGND	Power Ground: The ground return for the switching currents.
7	VIN	Power Supply Voltage (Input): Requires bypass capacitor to GND
8	EN	Enable/Delay (Input): Apply a Logic High to start the device. Apply Logic Low to stop the device; placing it in a low quiescent current mode.
9	FILTER	Input Current Limit Filter: Place a capacitor to VIN to adjust the time constant for the input current limit filter.
10	LIMIT	Input Current Limit: Place a resistor to ground to adjust the average current limit from the input supply.
11	SLOPEC	Slope Compensation: Sets current mode slope compensation
12	FREQ	Frequency Control: The switching frequency is adjusted from 400kHz to 1.5MHz with a resistor from this pin to ground.
ePAD	HS Pad	Exposed Heatsink Pad: Thermal connection between die and external ground plane. A solid connection to a large ground plane is required for full output power. This pad must be connected to ground.

Absolute Maximum Ratings [1]

Supply Voltage (V_{IN}) ..... –0.3V to +6V
Output Switch Voltage (V_{SW}) ..... –0.3V to +6V
Power Good Voltage (V_{PGOOD}) ..... –0.3V to +6V
Enable Input Voltage (V_{EN}) ..... –0.3V to V_{IN}
Feedback Voltage (V_{FB}) ..... –0.3V to V_{IN}
AGND to PGND Voltage ..... –0.3V to +0.3V
Switch Current (I_{SW}) ..... Internally Limited
Power Dissipation ..... Internally Limited
Lead Temperature (soldering, 10sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C
ESD Human Body Model Rating [3] 2kV
ESD Machine Model Rating [3] 200V

Operating Ratings [2]

Supply Voltage (V_{IN}) ..... +3.0V to +5.5V
Power Good Voltage (V_{PGOOD}) ..... 0V to +5.5V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
Feedback Voltage (V_{FB}) ..... 0V to V_{IN}
AGND to PGND Voltage ..... –0.3V to +0.3V
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
3mm x 3mm MLF®-12(θ_{JA}) ..... 61°C/W
3mm x 3mm MLF®-12(θ_{JC}) ..... 27°C/W

Electrical Characteristics [4]

$V_{IN} = V_{EN} = 5.0V$, $V_{OUT} = 3.3V$, $I_{LOAD} = 10mA$, $C_{IN} = 10\mu F$, $L = 4.7\mu H$, $C_{OUT} = 47\mu F$, $R_{FREQ} = 100k\Omega$; $R_{SLOPEC} = 100k\Omega$, $R_{LIM} = 100k\Omega$, $R_{COMP} = 11.5k\Omega$, $C_{COMP} = 15nF$, $T_A = 25°C$; **bold** values indicate $–40°C \le T_J \le 125°C$; unless noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Input Supply					
Input Voltage Range (V_{IN})		**3.0**		**5.5**	V
V_{IN} UVLO Threshold	Rising	**2.75**	2.9	**3.0**	V
V_{IN} UVLO Hysteresis			320		mV
Quiescent Current	PWM Mode, $V_{EN} > 1.8V$, $V_{FB} = 0.9V$, $I_{OUT} = 0A$		1		mA
Shutdown Current	$V_{EN} = 0V$		1	5	µA
Reference Voltage					
Feedback Voltage	±2% over temperature	**0.98**	1	**1.02**	V
Feedback Bias Current	$V_{FB} = 1V$		1		nA
Output Voltage Line Regulation	$V_{IN} = V_{EN} = 4V$ to 5.5V, $I_{LOAD} = 100mA$		0.2		%
Output Voltage Load Regulation	$100mA < I_{LOAD} < 1.2A$		0.2		%
Enable Control					
Enable Logic High Threshold			1.2	**1.8**	V
Enable Logic Low Threshold		**0.4**	1		V
Input Current Limit					
Input Current Limit	$V_{FB} = 0.5V$, $R_{LIMIT} = 107k\Omega$	0.5	0.7	0.9	A
	$V_{FB} = 0.5V$, $R_{LIMIT} = 68.1k\Omega$	0.7	1.1	1.5	
	$V_{FB} = 0.5V$, $R_{LIMIT} = 46.4k\Omega$	1.1	1.6	2.1	

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

Electrical Characteristics [4]

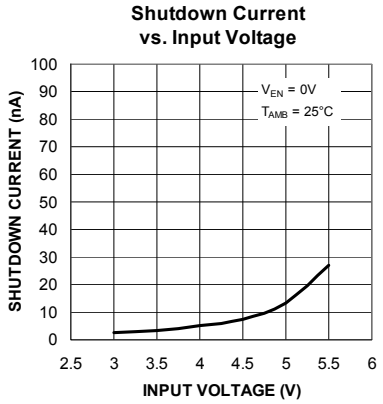
$V_{IN} = V_{EN} = 5.0V$, $V_{OUT} = 3.3V$, $I_{LOAD} = 10mA$, $C_{IN} = 10\mu F$, $L = 4.7\mu H$, $C_{OUT} = 47\mu F$, $R_{FREQ} = 100k\Omega$; $R_{SLOPEC} = 100k\Omega$, $R_{LIM} = 100k\Omega$, $R_{COMP} = 11.5k\Omega$, $C_{COMP} = 15nF$, $T_A = 25°C$; **bold** values indicate $–40°C \le T_J \le 125°C$; unless noted.

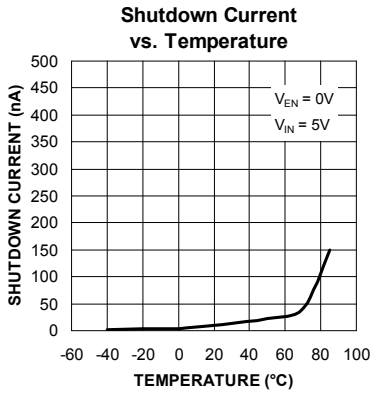
Parameter	Conditions	Min.	Typ.	Max.	Units
Soft Start					
Soft Start			Adaptive		
Internal FETs					
Top MOSFET RDS(ON)	$I_{SW} = 500mA$, $V_{FB} = 0.9V$		136	225	mΩ
Bottom MOSFET RDS(ON)	$I_{SW} = 500mA$, $V_{FB} = 1.1V$		100	225	mΩ
Oscillator/PWM					
Oscillator Frequency	$R_{FREQ} = 250k\Omega$	0.32	0.4	0.48	MHz
	$R_{FREQ} = 100k\Omega$	0.8	1	1.2	
	$R_{FREQ} = 60k\Omega$	1.2	1.5	1.8	
Maximum Duty Cycle	$V_{FB} < 0.5V$	100			%
Thermal Protection					
Over Temperature Shutdown			160		°C
Over Temperature Shutdown Hysteresis			20		°C
Power Good					
Power Good Threshold	V_{OUT} Rising (V_{OUT} % below nominal)	**6.5**	10	**12.5**	%
Power Good Output Low Voltage	$V_{FB} = 0.9V$, $I_{PGOOD} = 5mA$		130	200	mV
Power Good Leakage Current	$V_{FB} = 1.0V$, $V_{PGOOD} = 5.5V$			1	µA
				2	

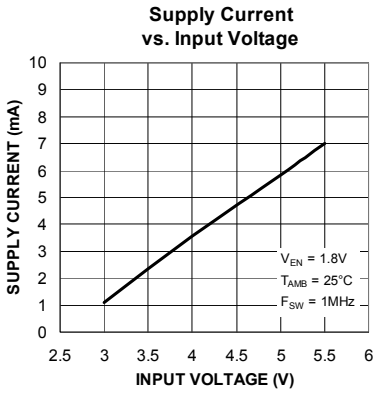
Note:

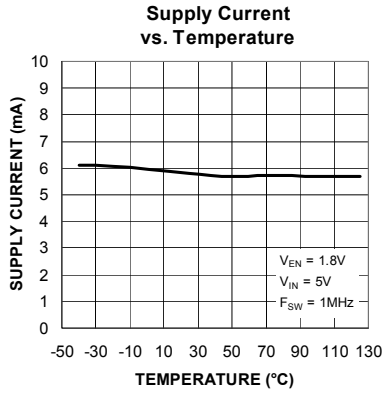
4. Specification for packaged product only.

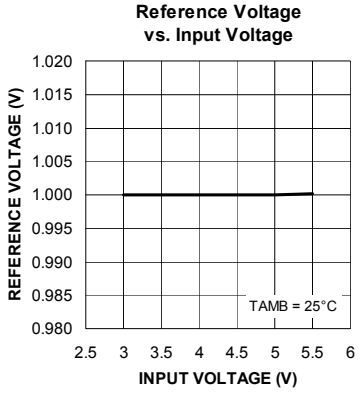
Typical Characteristics

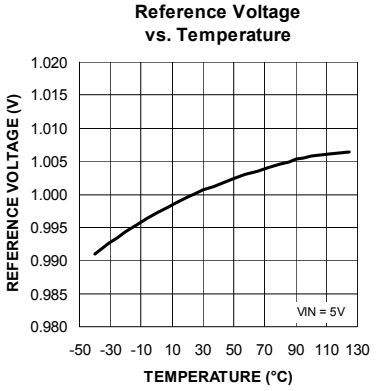


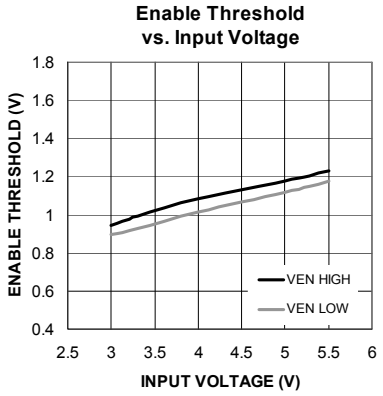


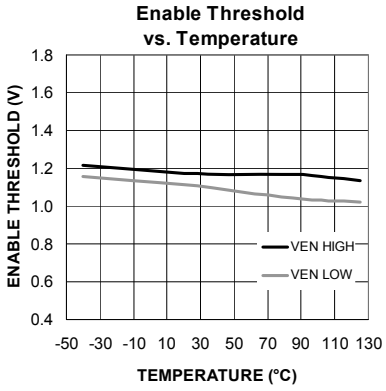


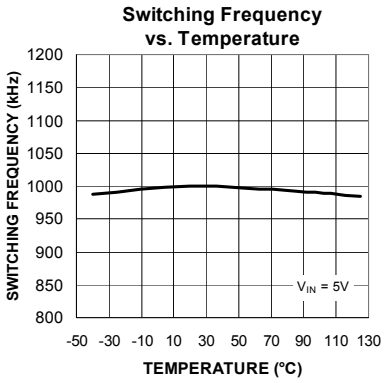


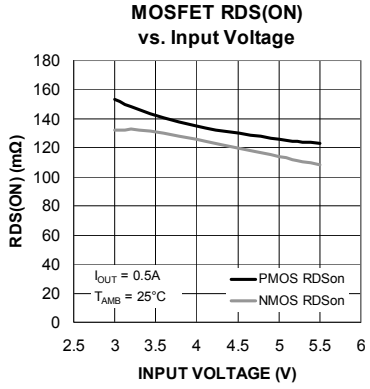


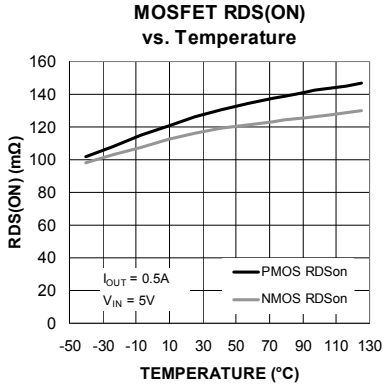


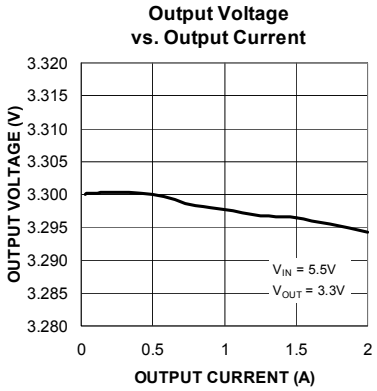




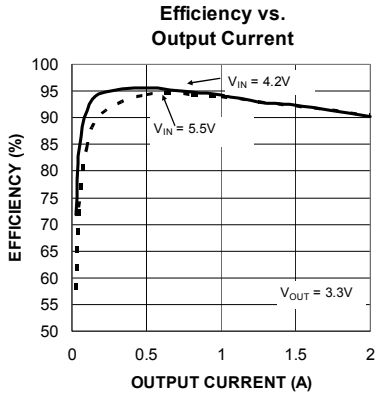


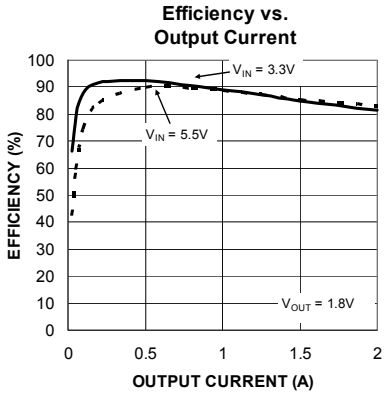


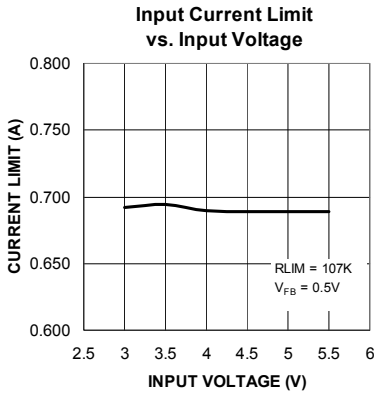


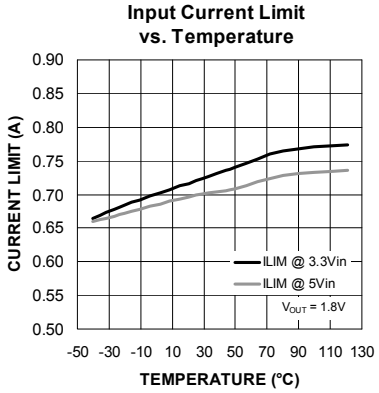


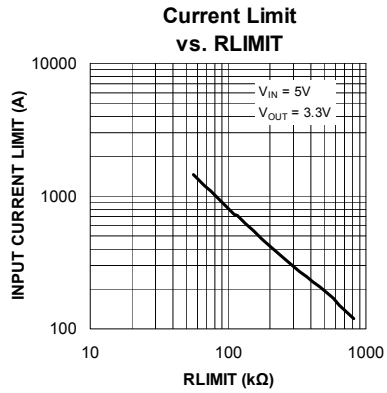
Typical Characteristics (Continued)

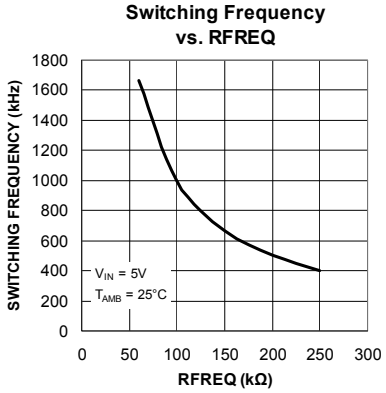






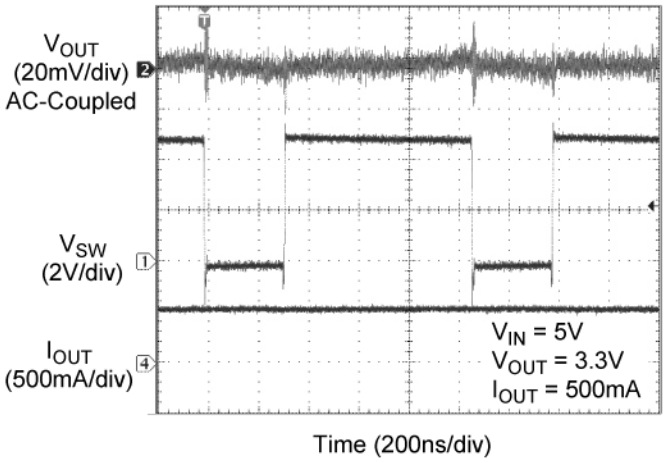




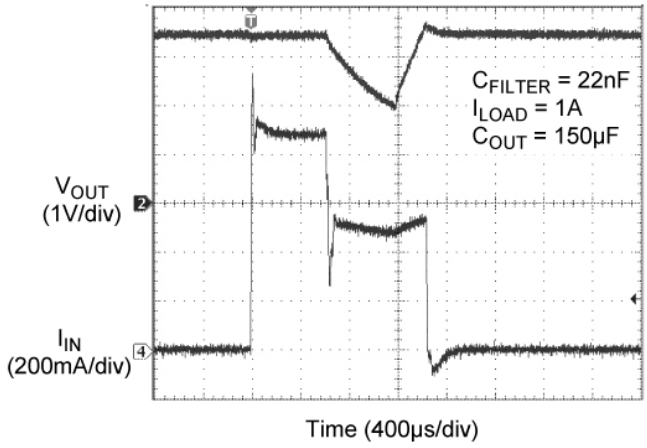


Functional Characteristics

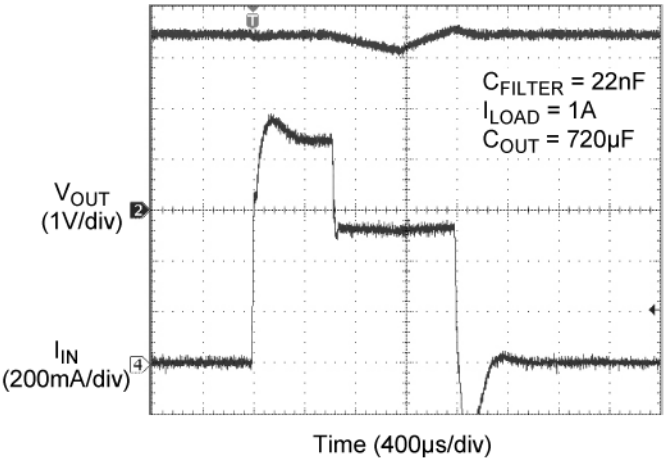
Switching Waveform



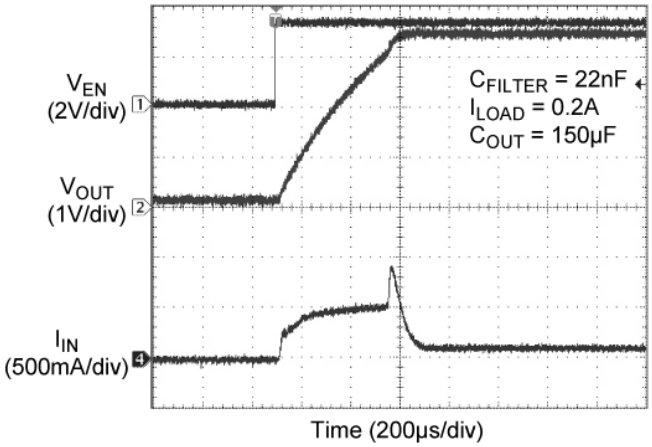
Load Step - Over Current



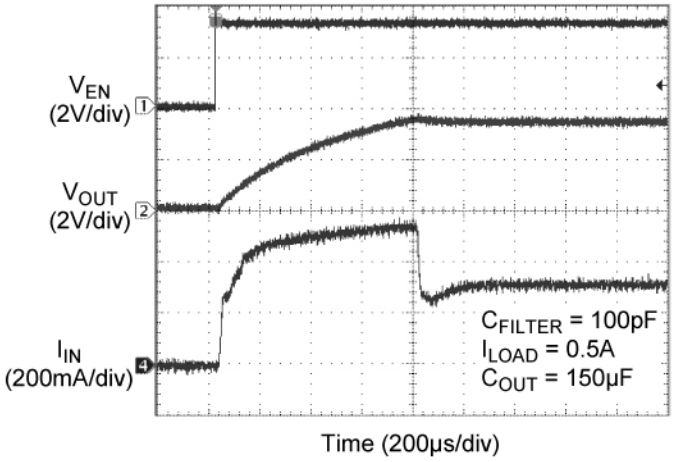
Load Step - Over Current



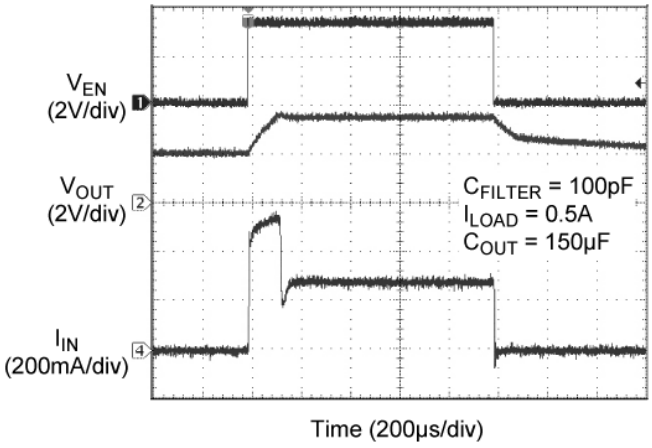
Startup Waveform



Startup Waveform

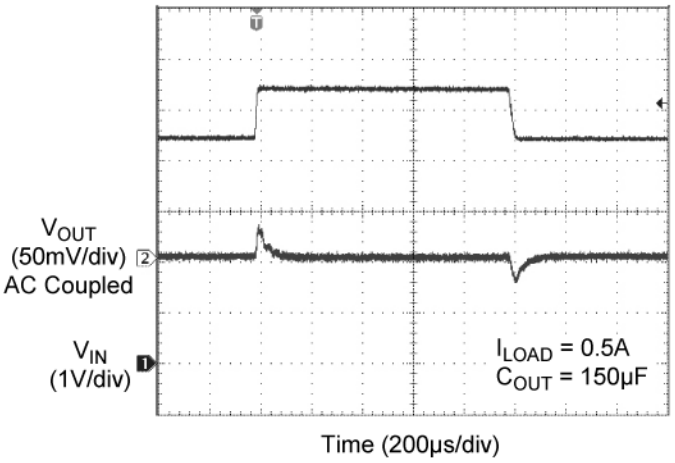


Startup Waveform - Pre-Bias=2V

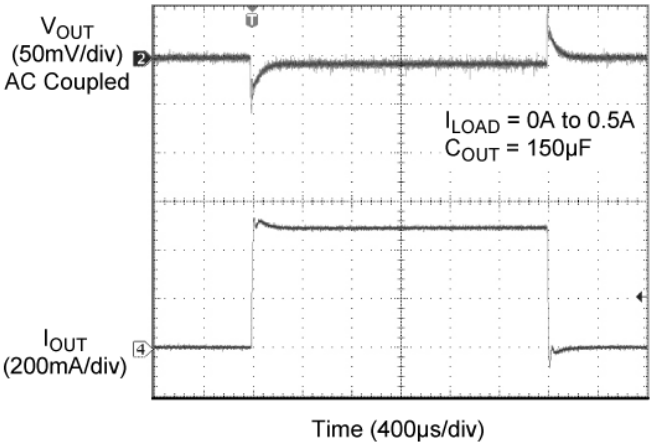


Functional Characteristics (Continued)

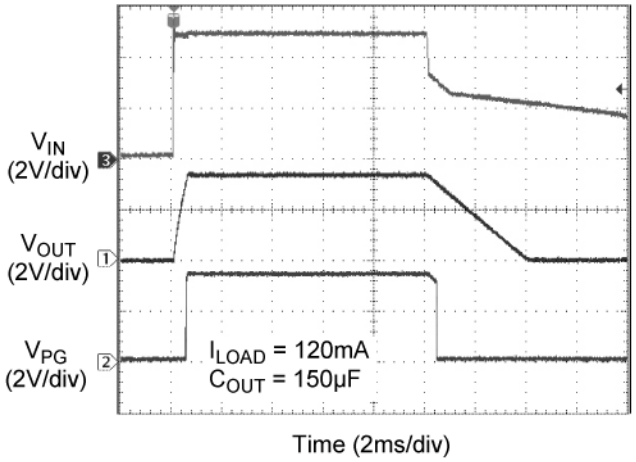
Line Transient Waveform



Load Transient Waveform



PG - Pulled-Up to VOUT



Functional Diagram

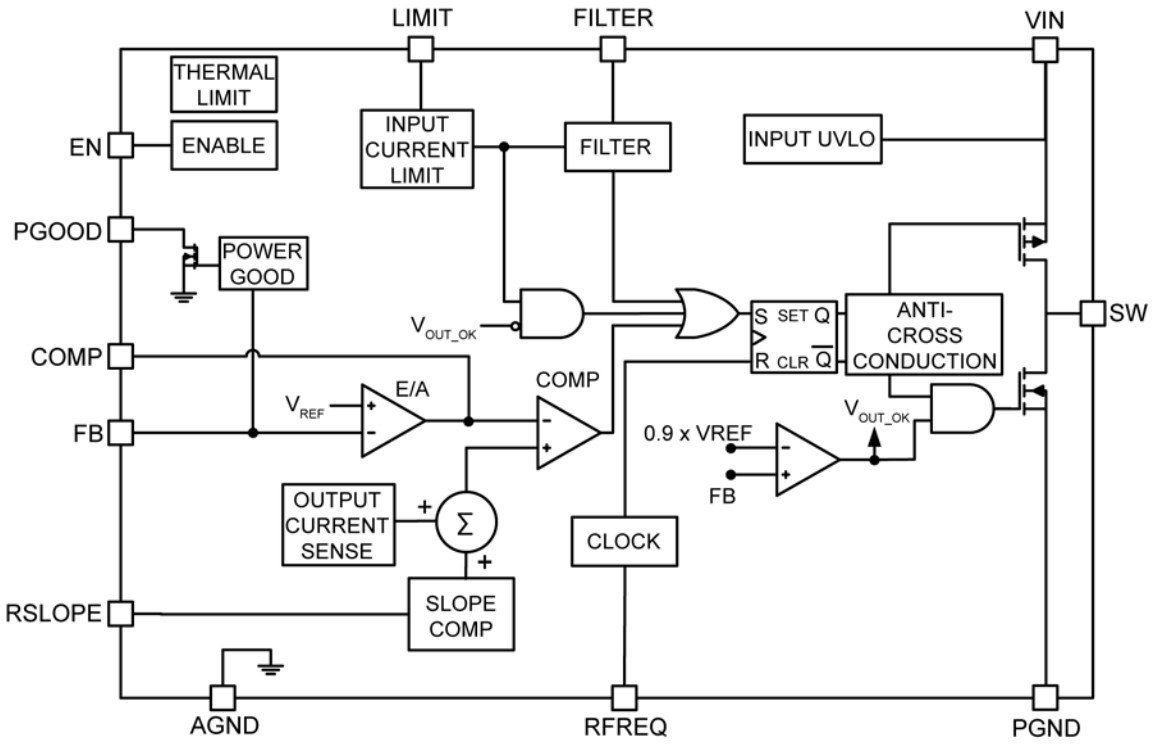


Figure 1. MIC2267 Functional Block Diagram

Functional Description

The MIC2267 is an input current limited, 2A synchronous buck regulator. The part offers control of the input average current limit and the time constant of the current limit response, allowing full control of the input current profile during load steps and plug in events. The P-Channel high side switch allows for 100% duty cycle operation. Optimization of the loop bandwidth can be achieved using the available connections to the slope compensation ramp and error amplifier nodes. For logic control and error flagging, the MIC2267 has an enable function and a Power Good function.

V_{IN}

The input supply (V_{IN}) provides power to the internal power MOSFETs and the analog control circuitry. The V_{IN} operating range is 3V to 5.5V. A minimum bypass capacitor of 10µF should be placed close to the input (V_{IN}) pin and the ground (PGND) pin. Refer to the *Layout Recommendations* section for details on placing the input capacitor.

LIMIT

The current limit as set by the R_{LIMIT} resistor (Nominally, I_{LIMIT} = 75k/R_{LIMIT}) is converted to the total charge allowed in one cycle (Q_{TOT}). So if the current limit is 1A and the frequency is 1MHz, since Q = I x T, the total charge allowed Q_{TOT} = 1µC. If for example, a 1µF capacitor C_{TOT} is used to store this charge, since Q = C x V, the voltage would be 1V.

If a replica of the input current is then integrated and the resultant input charge per cycle:

$$Q_{IN} = \int_0^T I_{IN}(t).dt$$

Is stored on a similar 1µF capacitor C_{INT}, then input current limit is reached when the voltage on the C_{INT} capacitor reaches 1V, i.e. $Q_{IN} \geq Q_{TOT}$. Once this condition is satisfied and the FILTER delay time has elapsed, the P-Channel switch cycle is terminated. At the beginning of each cycle the integration storage capacitors are discharged. In the actual circuit the storage capacitor is in the order of 5pF and the replica current is scaled down accordingly.

This is, effectively, cycle by cycle input current limit where the average input current in each cycle is limited. The advantage of this scheme is that when the input current budget has been used up for that cycle and the top switch goes off, the output can still draw current from ground and switching continues in an efficient manor. Conventional input current limit schemes which utilize an input switch will effectively drop V_{IN} and leave the switcher at 100% duty cycle; in effect current limiting like an LDO current limits.

FILTER

The filter pin can be used to implement a delay to the input current limit, thus allowing acceptable bursts of current to pass, unaffected. However the magnitude of the over current will act to shorten the allowable pulse width; effectively regulating charge passed; thus for a given input capacitor, the droop during over current peaks can be kept constant.

The Delay circuit is an identical circuit to the LIMIT circuit except that the current being stored on the integrating capacitor is first sent through a single pole RC filter i.e. a replica of the P-Channel Drain current is fed into a parallel RC. The R is set internally to 50kΩ (±20%) and the C is the external (C_{FILTER}). The FILTER current limit is set to 80% of the nominal input current limit, i.e., in the previous example, whereas the LIMIT circuit has to charge the storage capacitor C_{INT} to 1V, the FILTER current limit circuit only has to charge the integration storage capacitor C_{INTFIL} to 0.8V.

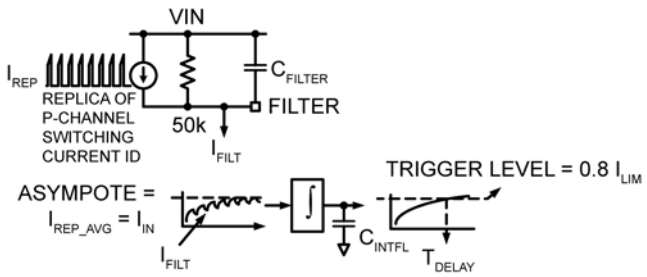


Figure 2. MIC2267 FILTER Pin Operation

The rising function after the integration block (voltage on C_{INTFIL}) is actually discharged to 0v each cycle, but for clarity, it is shown as an 'envelope' to show its rising characteristic.

$$T_{DELAY} = -\ln\left(1 - 0.8 \times \frac{I_{LIM}}{I_{IN}}\right) \times 50k\Omega \times C_{FILTER}$$

Typically, C_{INTFIL} takes time to reach this 80% trip level. Therefore, asserting current limit on the current cycle is highly dependant on internal delays and the extremity of the over current. Therefore, if the filter circuit reaches the 80% trigger level in a given cycle (n), the actual current limit is allowed to work during the next cycle (n+1).

When V_{OUT} < 90% V_{OUT} nominal, e.g. during startup or large load transients, the filter/delay function is disabled. This is to allow a defined startup current limit and reduce voltage peaks.

ENABLE (EN)

This is the enable pin. Taking this pin above 1.8V will enable the part to begin switching. Taking this pin below 0.4V will put the part into the shutdown mode where nominally, the part will consume < 1µA.

POWER GOOD (PGOOD)

This is an open drain output which can be connected via a pull up resistor to V_{OUT} or an external voltage up to 5.5V. This pin is pulled low while the part is enabled and the output is below 90% of the nominal output voltage. When the trigger threshold of nominally >90% nominal V_{OUT} is crossed, the PGOOD N-Channel FET is switched off and the pin will be high impedance.

Note that the power good function is inactive while the part is in shutdown (EN=Low). I.E. If the PG pull up resistor is connected to VIN, PG will be high when EN is below the enable threshold.

COMP

COMP is the output connection of the voltage error transconductance amplifier. The MIC2267 is a current mode controller and therefore will require just a capacitor and resistor connected from COMP to AGND to create a single pole, single zero compensator to stabilize the loop. An additional capacitor from COMP to AGND can be added to reduce switching jitter due to high frequency switching noise entering the loop.

If desirable, slope compensation can be increased/ reduced to improve stability/transient response over a wide duty cycle range including 100%. In such cases, additional compensation may be added to this pin if required.

FB

Connect this pin to the junction of the output voltage feedback resistors. The regulation loop will set the output voltage to the correct level determined by these feedback resistor values. The output voltage will be:

$$V_{OUT} = V_{REF}(1+R1/R2)$$

For most applications, R2 can be set to 10k and R1 can be found by:

$$R1 = R2(V_{OUT}/V_{REF} - 1)$$

SLOPEC

To guarantee stability in a current mode controller operating at duty cycle >50%, a compensation ramp (m) is required. This ramp 'm' is added to the inductor current sense ramp (or alternatively, it can also be subtracted from the error voltage which has the same effect).

A resistor to ground from the SLOPEC pin sets the amplitude of 'm' over the switching period.

Ideally, the magnitude of the compensation ramp (m) is for many cases, set to ½ inductor discharge ramp (m2). I.E. m= ½ m2

Where:

$$m2 \propto Vo/L \times F_{SW}$$

and

$$m \propto 67700/R_{SLOPEC}$$

Therefore, for the ideal ½ m2 slope:

$$R_{SLOPEC} = 2 \times F_{SW} \times L \times 67700/Vout$$

Where duty cycle can approach 100%, excess phase shift in the loop can lead to a phenomenon called "sub-harmonic oscillation". Additional compensating slope 'm' may be required in these cases.

It can be shown that ensuring m = m2 will ensure stability regardless of voltage loop gain for the case where DC ~ 100%. Therefore, a value of $R_{SLOPEC} = F_{SW}$.x L x 67700/Vout will ensure stability at the expense of some line regulation.

AGND and PGND

Connect AGND to the quiet, signal reference points and decouple closely to the IC. Connect PGND to the high current carrying paths close to the C_{OUT} and C_{IN}. Refer to layout guide section later in the datasheet for more detailed information.

FREQ

A resistor R_{FREQ} from this pin to ground allows the frequency of the MIC2267 to be programmed over the range 400kHz to 1.5MHz.

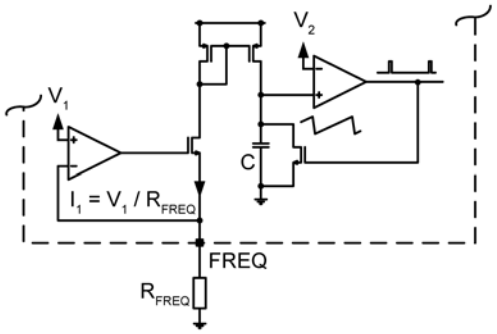


Figure 3. MIC2267 FREQ Pin Internal Blocks

To set the frequency, this pin is forced to V_1, the resulting current through the resistor R_{FREQ} sets the internal reference current which charges a capacitor (C). At the beginning of the clock cycle, C begins charging. When it reaches V_2, a clock pulse is generated and C is discharged to ground; marking the beginning of the next clock cycle.

This produces a clock frequency F_{SW} of:

$$F_{SW} = 1/(C \times R_{FREQ})$$

Where C = 10pF

SW

This is the center connection output of the P-channel and N-channel Power MOSFETs. Connect this pin to the Power inductor as close to the IC as possible. Refer to the *Layout Recommendations* section for details on placing the power inductor.

Application Information

FILTER

The USB 2.0 specification requires that current surges during transitions should result in a droop at an upstream USB port <330mV. In addition to the 10µF allowable USB "device" input capacitance; there is also a mandatory 120µF capacitor at each upstream Hub VBUS terminal. This presents a challenge as there is an amount of energy available within this hub capacitance that can be tapped only if the droop can somehow be limited remotely at the device end. Since the MIC2267 implements a charge limit system, this available energy can be utilized by adjusting C_{FILTER}.

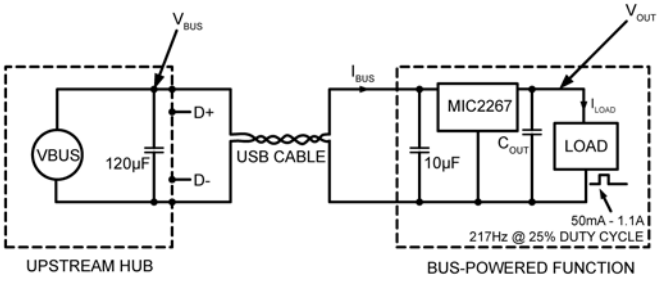
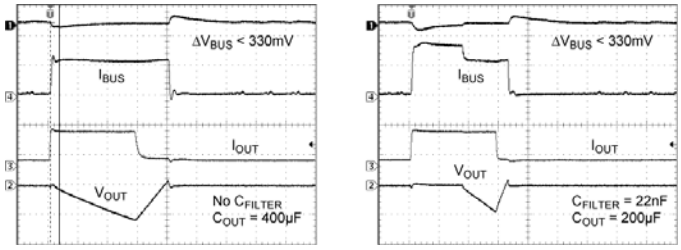


Figure 2. USB Bus Powered Function Example

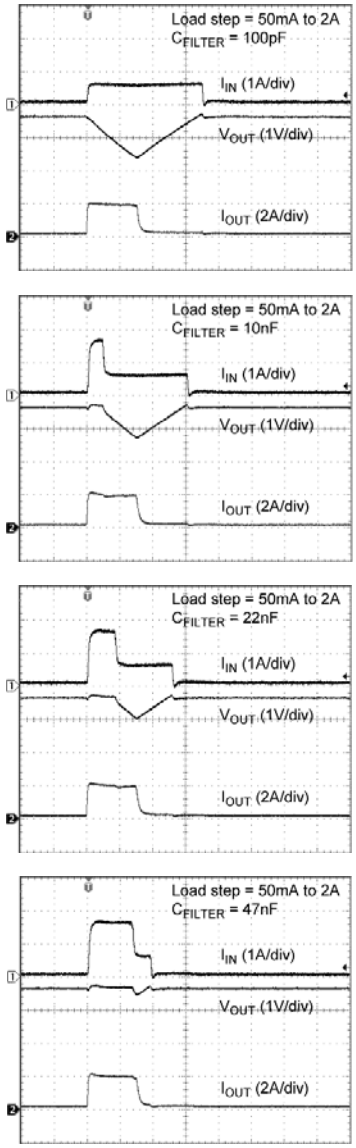


Where actual C_{BUS} is higher than 120µF, the FILTER capacitor can be increased to allow greater current limit delay times. This can help further reduce the value of output bulk holdup capacitors (C_{OUT}) in applications that require large, short term load pulses such as TDMA wireless data modems.

The FILTER capacitor should be placed as close as possible to the FILTER and VIN pins to set the input current limit delay time. Recommended minimum value is 100pF.

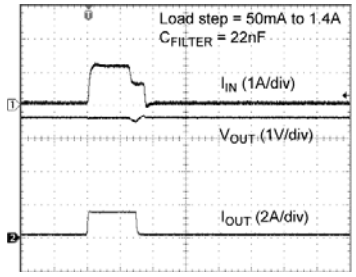
Effect of Changing FILTER Capacitor on V_{OUT}

C_{OUT} = 447µF, V_{OUT} = 3.3V, Load pulse width = 600µs:



Reducing over current peak increases limit delay time in accordance with the T_{DELAY} equation:

$$T_{DELAY} \approx -\ln\left(1 - 0.8 \times \frac{I_{LIM}}{I_{IN}}\right) \times 50k\Omega \times C_{FILTER}$$



LIMIT

Resistor values of between 750kΩ and 46kΩ should be used to set the current limit between 0.1A and 1.6A. To set the nominal LIMIT resistor value:

$$R_{LIMIT} = 75k\Omega/I_{LIMIT}$$

In USB applications for example, two LIMIT resistors can be used to switch between 1 unit load (100mA) and 5 unit loads (500mA).

Due to a minimum on time implemented during current limit operation, there is lower limit to V_{OUT} where input current limit is regulated. When V_{OUT} sees a near short circuit at higher switching frequency, I_{IN} will be higher than the set I_{LIMIT}. Circuit losses will tend to keep this to a maximum of 250mA.

The limit can be found by:

$$V_{OUTMIN} = \left((V_{IN} + 0.8) \cdot F_{SW} \cdot 200ns\right) - 0.8$$

e.g., for V_{IN} = 5v and F_{SW} = 1MHz, V_{OUTMIN} = 0.36V

COMP

As the MIC2267 uses a current mode control, the control loop only requires a single pole/zero compensator to optimise stability and transient response. The recommended values are 11kΩ and 15nF. An additional 680pF capacitor can also be added to reject switching frequency noise.

FB

Connect a resistor divider between the V_{OUT} load terminal connection and output ground reference connection to minimize resistive voltage drops affecting load regulation.

For most applications, R2 can be set to 10kΩ and R2 can be found by:

$$R1 = R2(V_{OUT}/V_{REF} - 1)$$

SLOPEC

Connect a resistor between this pin and AGND as close to the MIC2267 as possible to reduce the possibility of noise adding into the control loop.

As described in the theory of operation, the ideal slope can be calculated as:

$$R_{SLOPEC} = 2.\ F_{SW}\ .\ L\ .\ 67700/V_{OUT}$$

This value can be scaled towards ½ this value to ensure stability up to and including 100% duty cycle.

FREQ

Connect a resistor between this pin and AGND as close to the MIC2267 as possible to reduce the possibility of switching noise causing frequency jitter.

Set the nominal switching frequency using:

$$F_{SW} = 1/ (C.R_{FREQ})$$

Where nominal C = 10pF

INDUCTOR

The MIC2267 was designed to work with 3.3µH to 10µH inductor values.

If a low ripple voltage output is a key design goal, then larger value inductors will reduce switching ripple current and output ripple voltage, but can also have larger DCR values in small packages; which can reduce efficiency. Inversely, if high efficiency is the key target, Lower value inductors will increase switching ripple current and therefore increase output ripple voltage, but will typically have lower DCR values in small packages and can improve efficiency.

As the MIC2267 uses input current limiting, care should be taken that during a short circuit condition, the inductor can operate with the power dissipated in it during this fault condition. Helpfully, The MIC2267 switches the low side driver off during a short circuit, which ensures most of the power dissipation occurs within the IC. e.g.:

P_{FAULT} = 5v x 1A = 5W

$V_{NFET} \approx 0.7V$

$V_{L\_DCR} = I_{IN}$ x DCR = 1A x 50mΩ = 0.05V

Power in the inductor DCR = 7% overall dissipation.

P_{L_DCR} = 0.36W

The MIC2267 thermal limit protection will therefore limit the power in the inductor and protect from over dissipation. Protection is further improved by designing a low thermal resistance connection between the inductor and the IC. To achieve this, a short, wide PCB trace from the inductor to the SW pin is recommended. Connecting the inductor close to the SW pin is also good design practice as it minimizes the area available for radiating switching frequency harmonics around the local area of the switching regulator.

C_{IN}

Connect a ceramic capacitor of X5R or X7R dielectric from the VIN pin to PGND as close to the MIC2267 as possible to decouple the high di/dt switching current paths. A minimum value of 10µF is recommended for most applications. An additional 22µF can be useful in reducing ringing effects if long power leads are used to connect power.

C_{OUT}

Connect a ceramic capacitor of X5R or X7R dielectric from V_{OUT} to PGND as close as possible to the inductor and C_{IN} ground connection to reduce the effect of high di/dt ground currents from interfering with internal signals. A minimum of 47µF is recommended for most applications. Additional bulk capacitance such as electrolytic, tantalum or ceramic can be added to improve transient performance and hold up during large load transients.

5V Pass Through

Some applications will require a legacy 5v supply to be available which also benefits from the current limit protection. The circuit in Figure 5 allows for a low current bias supply to be provided while still providing current limit protection.

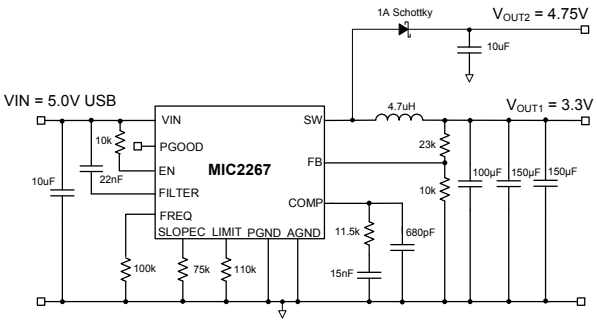


Figure 3. Standard MIC2267 Circuit with Protected ~5v Bias Supply

Below are some oscilloscope shots of the Pass through circuit operating under the following conditions:

Normal operation:

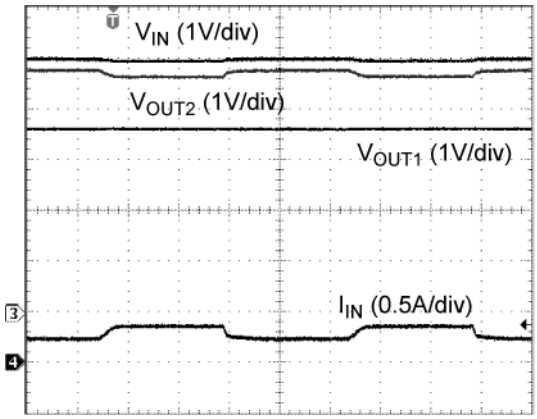
V_{OUT1} = 3.3v @ 200mA Continuous Load

V_{OUT2} = 4.75v @ 80mA to 200mA Pulsing Load

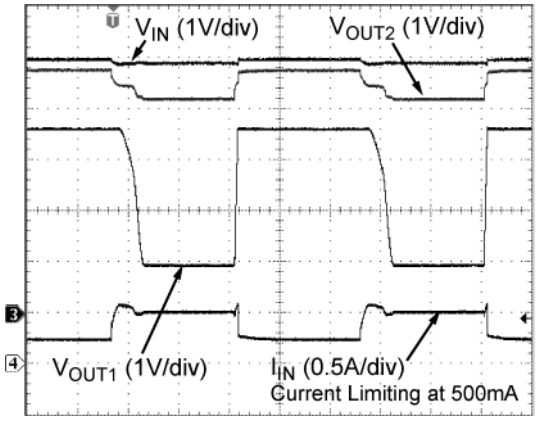
Over Current peaks applied:

V_{OUT1} = 3.3v @ 200mA Continuous Load

V_{OUT2} = 4.75V @ 80mA to 600mA Pulsing Load



Normal operation; no Over Current



Over Current Peaks applied on V_{OUT2}

PCB Layout Guidelines

To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC2267 converter.

IC

1. The 10µF ceramic capacitor, which is connected to the VIN pin, must be located right at the IC. The VIN pin is noise sensitive and placement of the capacitor is critical. Use wide traces to connect to the VIN and PGND pins.
2. The signal ground pin (AGND) must be connected directly to the ground planes. The common connection of PGND and AGND should be at the LOAD GND terminal.
3. Place the IC close to the point of load (POL).
4. Use fat traces to route the input and output power lines.
5. Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

1. Place the input capacitor next.
2. Place the input capacitors on the same side of the board and as close to the IC as possible.
3. Keep both the VIN and PGND connections short.
4. Place several vias to the ground plane close to the input capacitor ground terminal.
5. Use either X7R or X5R dielectric input capacitors.
6. Do not use Y5V or Z5U type capacitors.
7. Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
8. If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
9. In “Hot Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply with power is suddenly applied.

Inductor

1. Keep the inductor connection to the switch node (SW) short.
2. Do not route any digital lines underneath or close to the inductor.
3. Keep the switch node (SW) away from the feedback (FB) pin.
4. To minimize noise, place a ground plane underneath the inductor.

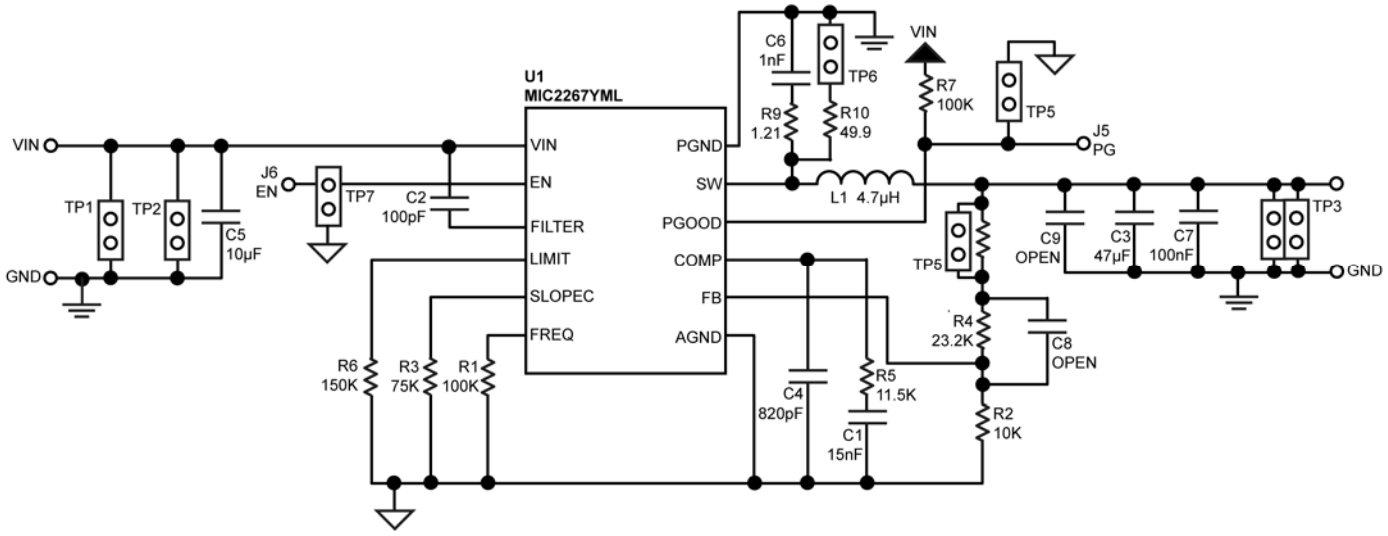
Output Capacitor

1. Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
2. Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
3. The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

RC Snubber

1. Place the RC snubber on the same side of the board and as close to the SW pin as possible.

MIC2267 Typical Application Circuit



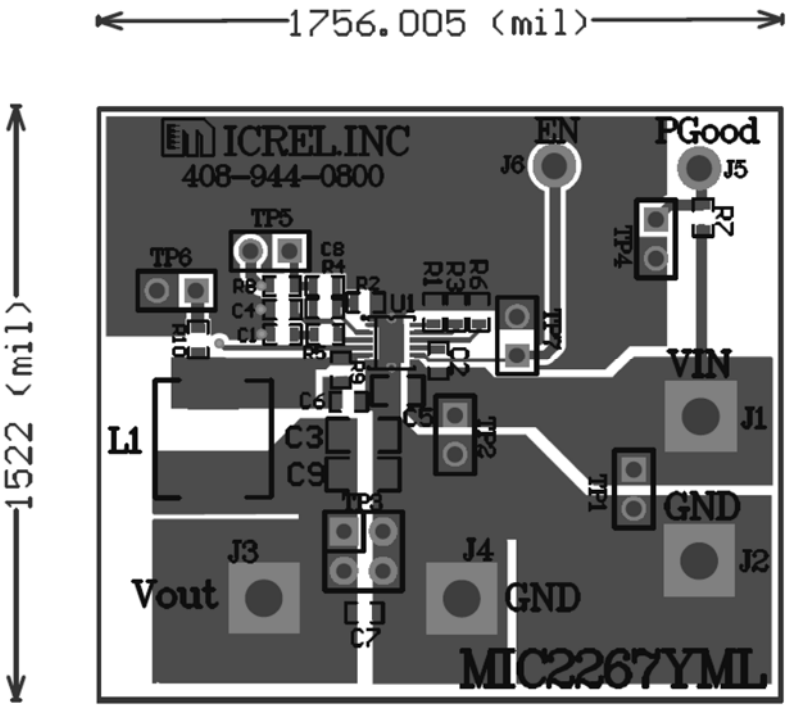
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
L1	VLF5014ST-4R7M1R7	TDK[1]	4.7µH, 2A inductor	1
C3	12066D476MAT2A	AVX[4]	47µF, 6.3V, X5R ceramic capacitor	1
C9	Not Fitted 1210 size			0
C5	08056D106MAT2A	AVX[4]	10µF, 6.3V, X5R ceramic capacitor	1
C7	06033D104MAT2A	AVX[4]	0.1µF, 25V ceramic capacitor	1
C1	06033C153MAT2A	AVX[4]	15nF, 25V, ceramic capacitor	1
C6	06033C102MAT2A	AVX[4]	1nF 25V, ceramic capacitor	1
C2	06033A101KAT2A	AVX[4]	100pF, 25V, COG ceramic capacitor	1
C4	06035A821JAT2A	AVX[4]	820pF, 50V, NPO ceramic capacitor	1
C8	Not Fitted 0603 size			0
R1, R7	CRCW06031003FRT1	Vishay Dale[2]	100K (0603 size), 1%	2
R2	CRCW06031002FRT1	Vishay Dale[2]	10K (0603 size), 1%	1
R3	CRCW06037502FRT1	Vishay Dale[2]	75K (0603 size), 1%	1
R4	CRCW06032322FRT1	Vishay Dale[2]	23.2K (0603 size), 1%	1
R5	CRCW06031152FRT1	Vishay Dale[2]	11.5K (0603 size), 1%	1
R6	CRCW06031503FRT1	Vishay Dale[2]	150K (0603 size), 1%	1
R8	CRCW060322R1FRT1	Vishay Dale[2]	22.1 (0603 size), 1%	1
R9	CRCW08051R21FRT1	Vishay Dale[2]	1.21Ω (0805 size), 1%	1
R10	CRCW060349R9FRT1	Vishay Dale[2]	49.9Ω (0603 size), 1%	
U1	**MIC2267YML**	**Micrel, Inc.[5]**	**Input Current Limiting Synch' Buck Regulator (12 pin 3mm x 3mm MLF)**	**1**

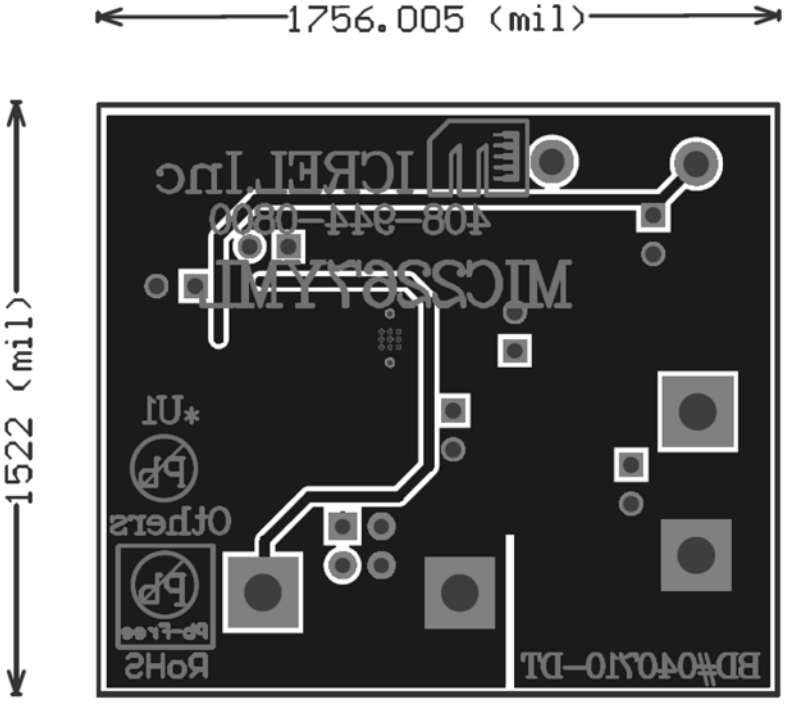
Notes:

1. TDK: www.tdk.com.
2. Vishay: www.vishay.com.
3. Murata: www.murata.com.
4. AVX: www.avx.com.
5. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

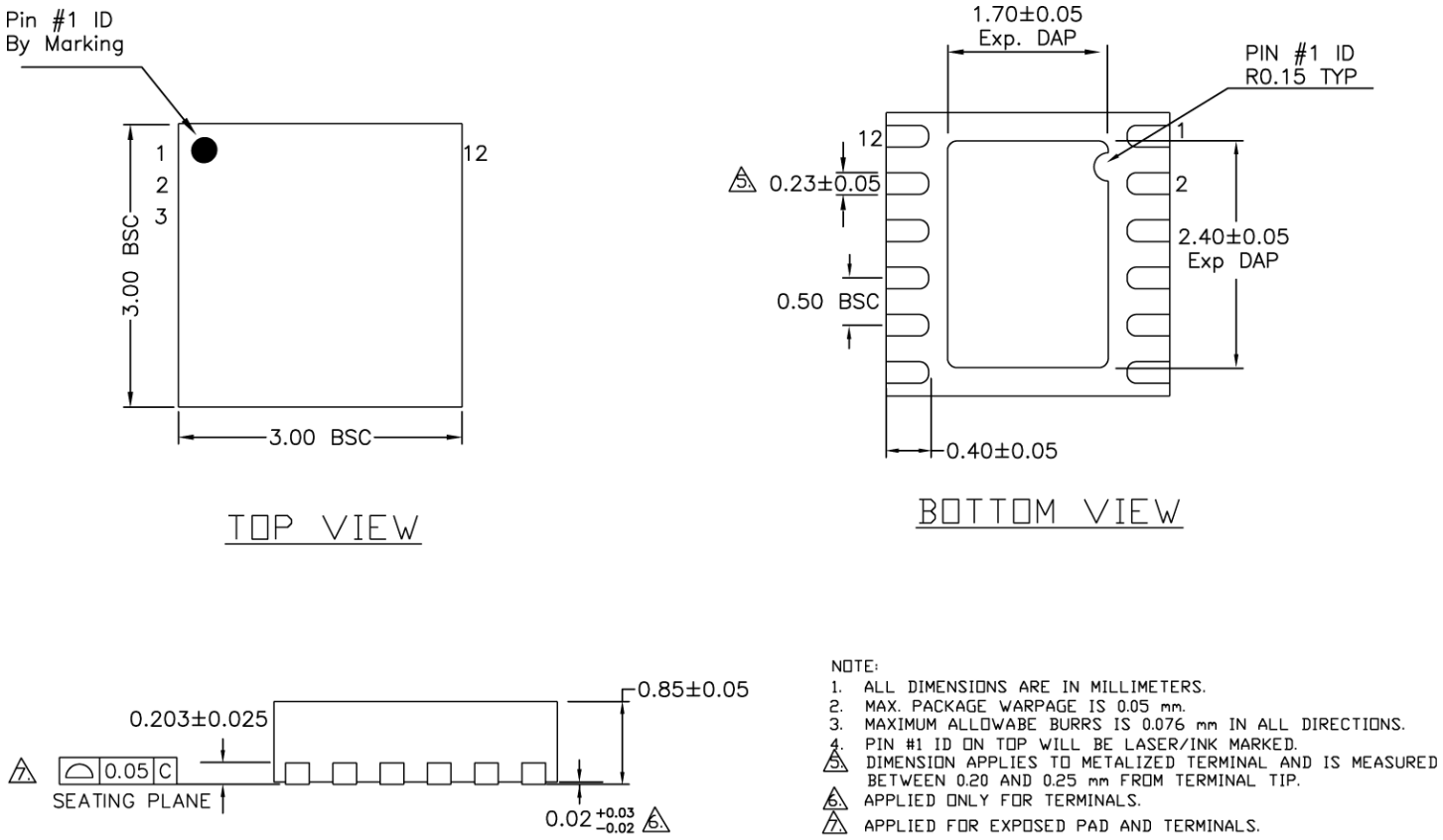


Top Layer



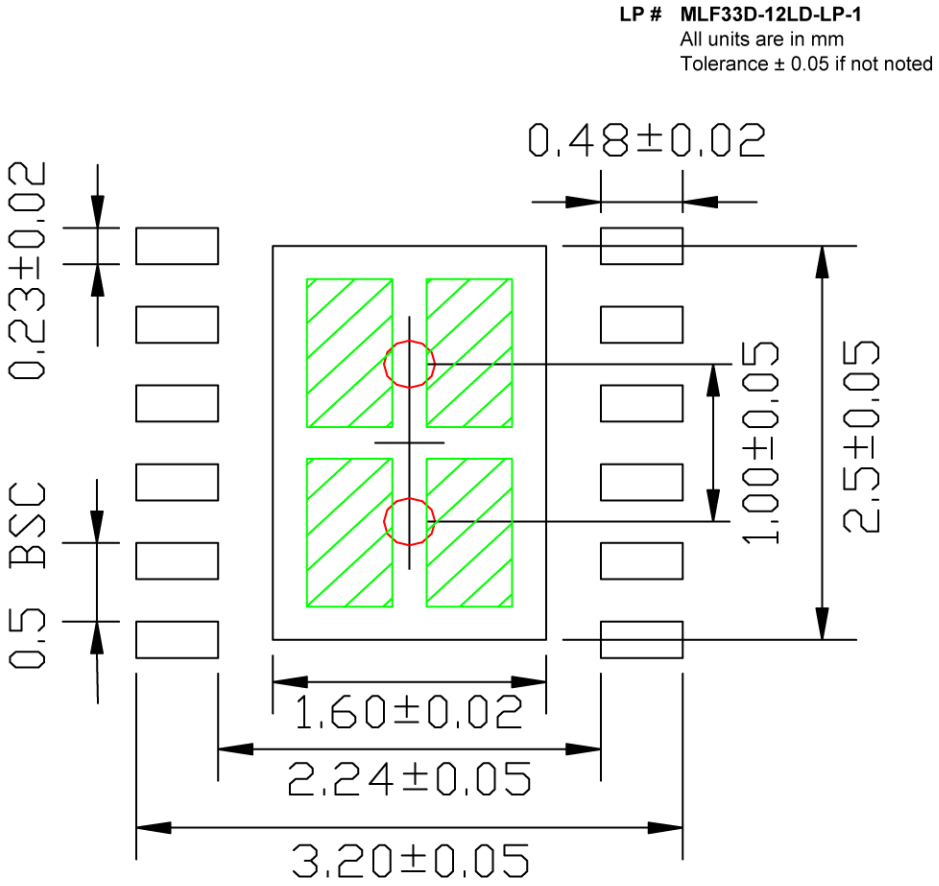
Bottom Layer

Package Information



12-Pin MLF® (YML)

Recommended Land Pattern



Red circle indicates Thermal via. Size should be 0.300mm – 0.350mm in diameter, 1.00mm pitch and should connect to GND plane for maximum thermal performance.

Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Size should be 0.50mm x 0.95mm, 1.15mm pitch.

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