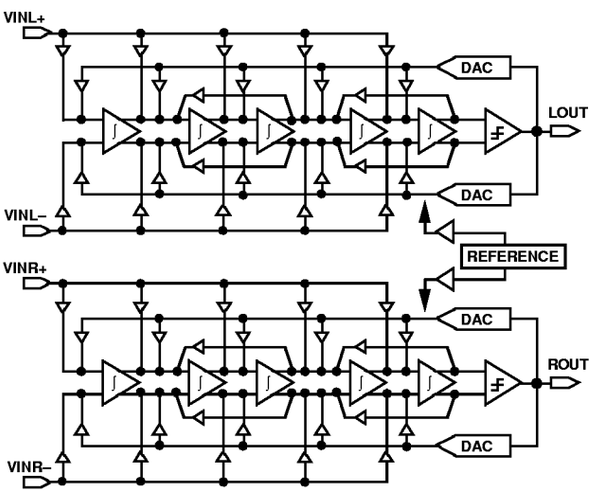
Dual-Channel ∑Δ Modulator

ADMOD79*

FEATURES
- High-Performance ∑Δ ADC Building Block
- Fifth-Order, 64 Times Oversampling Modulator with Patented Noise-Shaping
- Modulator Clock Rate to 3.57 MHz
- 103 dB Dynamic Range (for 20 kHz Input Bandwidth)
- Differential Architecture for Superior SNR and Dynamic Range
- Dual-Channel Differential Analog Inputs (±6.2 V Differential Input Voltage)
- On-Chip Voltage Reference

APPLICATIONS
- Digital Audio
- Medical Electronics
- Electronic Imaging
- Sonar Signal Processing
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT OVERVIEW

The ADMOD79 Sigma-Delta (∑Δ) modulator is a building block which can be used to build a superior analog-to-digital conversion system customized to a particular application's requirement. The ADMOD79 is a two-channel, fully differential modulator. Each channel consists of a fifth-order one-bit noise shaping modulator. An on-chip voltage reference provides a voltage source to both channels that is stable over temperature and time. There are separate single-bit digital outputs for each channel. The ADMOD79 accepts a $64 \times F_S$ input master clock (SMPCLK) that can range from 2.5 kHz to 3.57 MHz.

Input signals are sampled at $64 \times F_S$ on switched-capacitors, eliminating external sample-and-hold amplifiers and minimizing the requirements for antialias filtering at the input. With simplified antialiasing, linear phase can be preserved across the passband. The ADMOD79's proprietary fifth-order differential switched-capacitor modulator architecture shapes the one-bit comparator's quantization noise out of the passband. The high order of the modulator randomizes the modulator output, reducing idle tones in the output spectrum to very low levels. The ADMOD79's differential architecture provides increased dynamic range and excellent common-mode rejection characteristics. Because its modulator is single-bit, the ADMOD79 is inherently monotonic and has no mechanism for producing differential linearity errors. Analog and digital supply connections are separated to isolate the analog circuitry from the digital supplies.

The ADMOD79 is fabricated in a BiCMOS process and is supplied in a 0.6" wide 28-lead cerdip package. The ADMOD79 operates from ±5 V power supplies over the temperature range of –25°C to +70°C.

***Protected by U.S. Patent Numbers 5055843, 5126653, and others pending.**

REV. 0

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AD1879–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	±5	V	Input Signal	974	Hz
Ambient Temperature	25	°C		–0.5	dB Full-Scale
Input Clock (SMPCLK)	3.072	MHz	Passband	0 to 20	kHz

	Min	Typ	Max	Units
ANALOG PERFORMANCE				
Dynamic Range (0 Hz to 20 kHz, –60 dB Input)				
No A-Weight Filter	100	103		dB
With A-Weight Filter		105		
Signal to (Distortion + Noise)				
Full-Scale Input	90	96		dB
–20 dB Input		83		
Trimmed[1] Signal to (Distortion + Noise)				
Full-Scale Input	93	98		dB
–20 dB Input		83		dB
Trimmed[1] Signal to Total Harmonic Distortion				
Full-Scale Input		98		dB
–20 dB Input		100		dB
Analog Inputs				
Differential Input Range[2]	±5.89	±6.2	±6.51	V
Input Impedance at Each Input Pin		7.0		kΩ
DC Accuracy				
Gain Error			±5	%
Interchannel Gain Mismatch			±0.15	dB
Gain Drift		±200		ppm/°C
Offset Error (Referrred to Input)		±0.057	±0.343	% of FS
Offset Drift (Referred to Input)		±13		ppm/°C
Voltage Reference*	2.4	2.8	3.2	V
Crosstalk (EIAJ Method)	100			dB
Interchannel Phase Deviation		±0.001		Degrees
DIGITAL TIMING (Guaranteed over 0°C ≤ T_A ≤ 70°C, AV_{SS} = –5.0 V ± 5%, AV_{DD} = DV_{DD} = +5.0 V ± 5%)				
t_{SCP} SMPCLK Period	0.28		400	µs
t_{SCPWL} SMPCLK LO Pulse Width	140			ns
t_{SCPWH} SMPCLK HI Pulse Width	140			ns
t_{OPD} Propagation Delay, SMPCLK Falling Edge to ROUT, LOUT			100	ns
t_{RPD} Propagation Delay, SMPCLK Rising Edge to $\overline{RRESET}$, $\overline{LRESET}$			125	ns
DIGITAL I/O (Guaranteed over 0°C ≤ T_A ≤ 70°C, AV_{SS} = –5.0 V ± 5%, AV_{DD} = DV_{DD} = +5.0 V ± 5%)				
Input Voltage HI (V_{IH})	3.4			V
Input Voltage LO (V_{IL})			0.8	V
I_{IH} @ V_{IH} = 5 V			10	µA
I_{IL} @ V_{IL} = 0 V			10	µA
Output Voltage HI (V_{OH} @ I_{OH} = 360 µA)	4.0			V
Output Voltage LO (V_{OL} @ I_{OL} = 1.6 mA)			0.5	V
POWER SUPPLIES				
Current, DV_{DD}		1.0	1.5	mA
Current, $AV_{DD}1$, $AV_{SS}1$		76	95	mA
Current, $AV_{DD}2$, $AV_{SS}2$		8	12	mA
Current, $AV_{DD}1$, $AV_{SS}1$ – Power Down		14	20	mA
Dissipation				
Operation (All Supplies)		845	1078	mW
Power Down (All Supplies)		225	328	mW
Power Supply Rejection				
1 kHz 300 mV p-p Signal at Analog Supply Pins		102		dBFS
TEMPERATURE RANGE				
Specifications Guaranteed		+25		°C
Functionality Guaranteed	–25		+70	°C
Storage	–60		+100	°C

NOTES

[1]Differential gain imbalance manually trimmed to eliminate second harmonic. See "Application Issues" below.

[2]The differential input range is twice the range seen at each input pin. The input range corresponds to the full-scale digital output range.

*Guaranteed, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

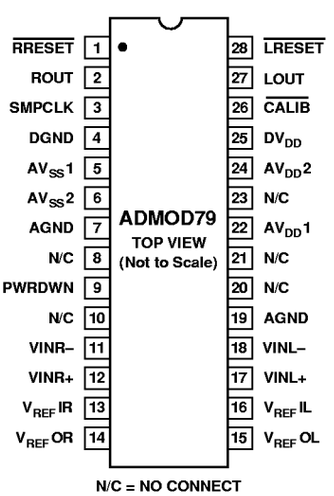
	Min	Max	Units
DVDD to DGND and $AV_{DD}1/AV_{DD}2$ to AGND	0	6	V
$AV_{SS}1/AV_{SS}2$ to AGND	–6	0	V
$AV_{SS}2$ to $AV_{SS}1$	–0.3		V
Digital Input to DGND	–0.3	DV_{DD} + 0.3	V
Analog Inputs	$AV_{SS}1$ – 0.3	$AV_{SS}1$ + 0.3	V
AGND to DGND	–0.3	0.3	V
Reference Voltage	Indefinite Short Circuit to Ground		
Soldering		+300	°C
		10	sec

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADMOD79JQ	0°C to +70°C	Cerdip	Q-28

PIN CONFIGURATIONS



N/C = NO CONNECT

PIN DESCRIPTIONS

Pin Number	Mnemonic	Input/ Output	Description
1	$\overline{\text{RRESET}}$	O	Right Modulator Reset
2	ROUT	O	Right Bitstream Modulator Output
3	SMPCLK	I	3.072 MHz (Nominal) Modulator Input Clock
4	DGND	I	Digital Ground
5	$AV_{SS}1$	I	–5 V Analog Supply
6	$AV_{SS}2$	I	–5 V Analog Logic Supply
7	AGND	I	Analog Ground
8	N/C		No Connect
9	PWRDWN	I	Power Down
10	N/C		No Connect
11	VINR–	I	Right Inverting Input
12	VINR+	I	Right Noninverting Input
13	$V_{REF}IR$	I	Right Reference Input
14	$V_{REF}OR$	O	Right Reference Output
15	$V_{REF}OL$	O	Left Reference Output
16	$V_{REF}IL$	I	Left Reference Input
17	VINL+	I	Left Noninverting Input
18	VINL–	I	Left Inverting Input
19	AGND	I	Analog Ground
20	N/C		No Connect
21	N/C		No Connect
22	$AV_{DD}1$	I	+5 V Analog Supply
23	N/C		No Connect
24	$AV_{DD}2$	I	+5 V Analog Logic Supply
25	DV_{DD}	I	+5 V Digital Supply
26	$\overline{\text{CALIB}}$	I	Calibration
27	LOUT	O	Left Bitstream Modulator Output
28	$\overline{\text{LRESET}}$	O	Left Modulator Reset Signal

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADMOD79 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS

Dynamic Range
The ratio of a full-scale output signal to the integrated output noise in the passband (0 kHz to 20 kHz with a 3.072 MHz modulator clock rate), expressed in decibels (dB). Dynamic range is measured with a –60 dB input signal and is equal to (S/[THD+N]) +60 dB.

Signal to (Distortion + Noise) (or S/[THD+N])
The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all spectral components in the passband, expressed in decibels (dB).

Signal to Total Harmonic Distortion (or S/THD)
The ratio of the rms value of the fundamental input signal to the rms sum of all harmonically related spectral components in the passband, expressed in decibels (dB).

Gain Error
With a near full-scale input, the ratio of actual output to expected output, expressed as a percentage.

Interchannel Gain Mismatch
With near full-scale inputs, the ratio of outputs of the two stereo channels, expressed in decibels.

Gain Drift
Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per °C.

Midscale Offset Error
Output response to a midscale input (i.e., zero volts dc), expressed as a percentage of full scale.

Midscale Drift
Change in midscale offset error with a change in temperature, expressed as parts-per-million (ppm) of full scale per °C.

Crosstalk
Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine-wave input on the other channel, expressed in decibels.

Interchannel Phase Deviation
Difference in input sampling times between stereo channels, expressed as a phase difference in degrees between 1 kHz inputs.

Power Supply Rejection
With analog inputs grounded, energy at the output when a 300 mV p-p signal applied to the power supply pins, expressed in decibels of full scale.

THEORY OF OPERATION

Resonators in the proprietary fifth-order ADMOD79 modulator architecture place zeros in the noise-shaping spectrum, reducing the quantization noise at lower frequencies. (See Figure 1.) The ADMOD79's fully differential architecture increases its signal-to-noise ratio performance. Completely independent right and left channels with separate references minimize crosstalk. Modulator clock rates as high as 3.57 MHz are supported.

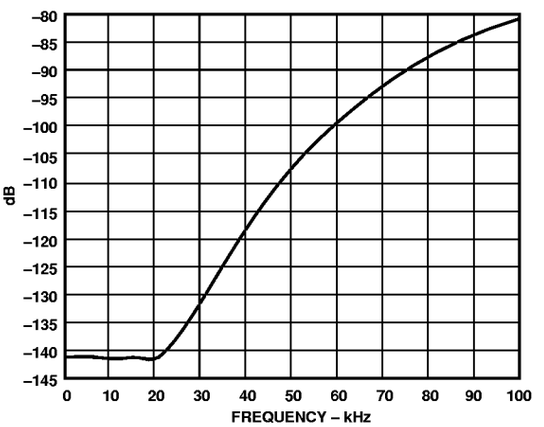


Figure 1. Noise Spectrum per 5 Hz (3.072 MHz Modulator Clock)

User-supplied digital decimation filters allow for a broad range of performance and filter functions. For standard, brick-wall digital low-pass filters with sufficient stopband attenuation, the following performance can be achieved with the ADMOD79 running at a 3.072 MHz modulator clock rate:

Filter Cut-Off Frequency	Oversampling Ratio	Signal-to-Noise Ratio
20 kHz	64	103 dB
10 kHz	128	106 dB
5 kHz	256	109 dB
2.5 kHz	512	112 dB
1.25 kHz	1024	115 dB
625 Hz	2048	118 dB

In general, since the noise is spectrally white in the passband, each halving of the input bandwidth with a constant modulator clock frequency will increase the SNR across the bandwidth by 3 dB.

Power consumption of the ADMOD79 is 1078 mW maximum. However, in power-down mode, consumption is reduced to 328 mW (with a 3.072 MHz modulator clock). Note that the ADMOD79 will still function in this mode. In the power-down mode, the ADMOD79 will operate with a slower modulator clock over a more limited bandwidth. The SNR over the band of interest is reduced relative to that possible with a full-speed modulator clock.

Typical modulator noise integrated across the passband of the modulator as shown in Figure 1 is always 103 dB, regardless of modulator clock rate. The width of that passband, however, scales down linearly with a slower clock. For example, if the modulator clock is slowed by a factor of two, noise will begin to rise at 10 kHz instead of 20 kHz. Since the same inband noise is now spread across a narrower passband, the noise per one Hz bin will also increase accordingly. Thus, the passband of Figure 1 will narrow and its floor will rise.

Modulator Clock	Modulator Passband	SNR	SNR per One Hz Bin
3.072 MHz	20 kHz	103 dB	145 dB
1.536 MHz	10 kHz	103 dB	142 dB
768 kHz	5 kHz	103 dB	139 dB
384 kHz	**2.5 kHz**	**103 dB**	**136 dB**
192 kHz	1.25 kHz	103 dB	133 dB
96 kHz	625 Hz	103 dB	130 dB

The power-down mode will support modulator clocks as fast as 384 kHz, shown above in bold.

As described above, the SNR can always be increased at a constant modulator clock rate by limiting the input bandwidth with a brick-wall digital decimation filter. This same technique can be used in the power-down mode. Thus, with a 384 kHz clock in the power-down mode, 105 dB would be achievable over a 1.25 kHz bandwidth (128 times oversampling) and 108 dB over a 625 Hz band of interest (256 times oversampling).

The ADMOD79's fifth-order modulators use a distinctive architecture of feed-forward and feed-back signal paths to achieve a high performance level. Gain is controlled by switched capacitors. Resonator loops feeding back from the third and fifth stage outputs allow the placement of zeros in the quantization-noise transfer function. These zeros have been chosen to further reduce noise in the passband. The noise floor is dominated by spectrally flat thermal circuit noise in the passband.

OPERATING FEATURES

The ADMOD79 produces a pair of noise-shaped bitstreams (LOUT and ROUT) from a pair of differential analog inputs (+VINL & –VINL and +VINR & –VINR). The analog input signal range at any given signal input pin is ±3.1 V. This implies that voltage difference across each differential pair can range ±6.2 V. The modulator clock oversamples the analog input at a rate much higher than the input bandwidth, significantly reducing the requirements on antialiasing filters. Only signals with frequency components near the very high modulator clock rate will alias into the passband. The high clock rate also eliminates the requirement for a sample-and-hold amplifier.

Holding the calibration input, $\overline{\text{CALIB}}$, LO disconnects the input from the modulators, regardless of the signal applied to the input pins. This feature allows for system calibration. Allow at least ten modulator clock cycles after asserting $\overline{\text{CALIB}}$ before reading the output bit streams.

Should an input overdrive the modulator to instability, the ADMOD79 will reset itself within 25 modulator clock cycles. Each modulator independently produces an output signal on pins $\overline{\text{LRESET}}$ and $\overline{\text{RRESET}}$, respectively, indicating the initiation of a reset sequence. These pins, normally HI, will go LO for one cycle should instability occur.

The pair of modulator outputs are TTL-compatible but are in fact driven to CMOS logic levels. Digital output data is valid on the rising edge of SMPCLK. For highest performance, the ADMOD79 modulator has been designed so that the full-scale range of the one's density is from 20% to 80% (i.e., –dc full scale = 20% one's density, +dc full scale = 80% one's density). The user's decimator should effectively gain up the modulator's output by a factor of 5/3 to produce a full-scale output corresponding to a full-scale input.

The ADMOD79 contains a pair of +2.8 V voltage references. The user has the option of using these internal references or supplying an external reference. In the former case, two external capacitors and two external resistors are required for voltage reference noise reduction. These capacitors and resistors should be connected between reference inputs (V_{REF}IL and V_{REF}IR) and analog ground as shown in Figure 2. The reference outputs (V_{REF}OL and V_{REF}OR) should be connected directly to the reference input pair. To use external reference(s), bypass the reference(s) to analog ground and connect to the reference inputs (V_{REF}IL and V_{REF}IR). The reference outputs become no connects.

The ADMOD79 requires a ±5 V analog supply and a +5 V digital supply. The analog supply should be connected to the two sets of analog supply pins, which should be decoupled from each other. (The $AV_{SS}1$ and $AV_{DD}1$ pins power the amplifiers and other active analog circuitry; the $AV_{SS}2$ and $AV_{DD}2$ pins provide voltage for the modulator's switches.) See Figure 4 for the recommended bypassing configuration.

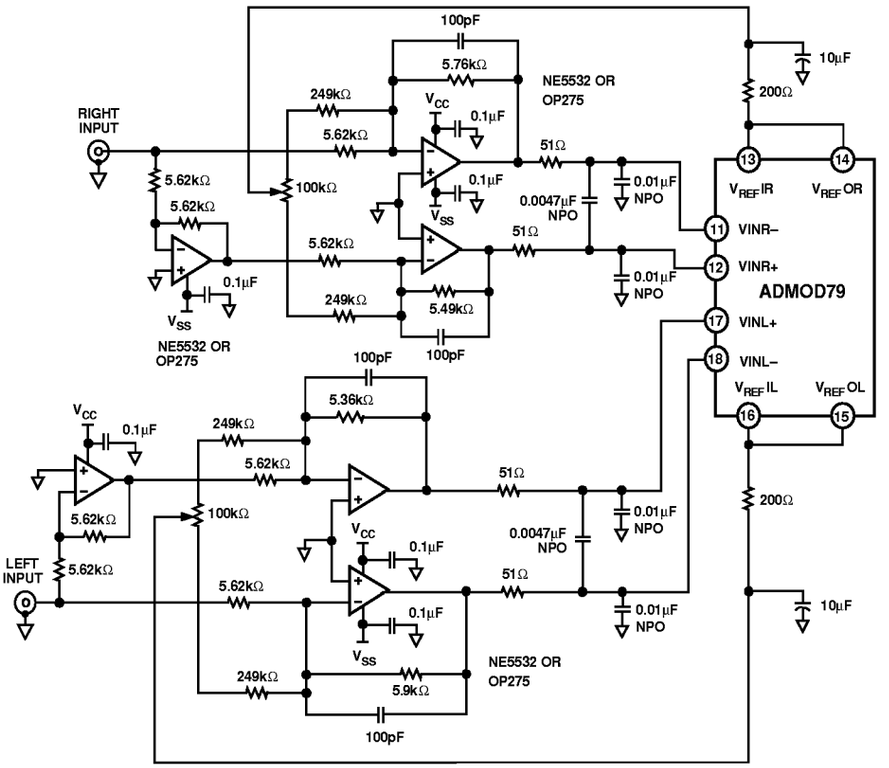


Figure 2. Recommended Input Structure

APPLICATIONS ISSUES

Recommended Input Structure

The ADMOD79 input structure is fully differential for improved common-mode rejection properties and increased dynamic range. Since each input pin sees ±3.1 V swings, each channel's input signal effectively swings ±6.2 V, i.e., across a 12.4 V range.

In most cases, a single-ended-to-differential input circuit is required. Shown in Figure 2 is the recommended circuit, based on extensive experimentation. Note that to maximize signal swing, the op amps in this circuit are powered by ±12 V or greater supplies. The ADMOD79 itself requires ±5 V supplies. If ±5 V supplies are not available in the target system, Figure 3 illustrates the recommended circuit for generating these supplies.

The trim potentiometers shown in Figure 2 connecting the minus (–) inputs of the driving op amps permit trimming out dc offset, if desired.

Note that the driving op amp feedback resistors all have slightly different values. These values produce a slight differential gain imbalance and were derived empirically to minimize second harmonic distortion on average and produce the lowest overall THD without part-by-part trimming. Replacing one of these feedback resistors in each channel with a trim potentiometer allows trimming the differential gain imbalance for part-by-part optimal performance. Analog Devices has done this in the lab by paralleling 100 kΩ trim potentiometers around the 5.49 kΩ and 5.36 kΩ input feedback resistors for the VINR+ and VINL+ signals that can be found in Figure 2. By trimming gain imbalance, second harmonic distortion can always be eliminated. In the "Specifications" section of this data sheet, a distinction is drawn between trimmed and untrimmed signal-to-(noise + distortion) and trimmed and untrimmed total harmonic distortion. The untrimmed specifications are tested with the input structure shown in Figure 2. The trimmed specifications are based on a part-by-part trim of this differential gain to eliminate the second harmonic.

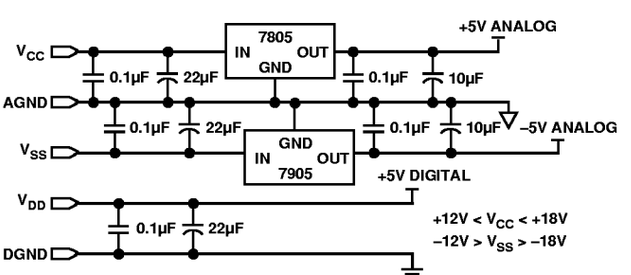


Figure 3. ADMOD79 Recommended Power Conditioning Circuit

The input circuit of Figure 2 could be implemented with a single pair of operational amplifiers per channel, one inverting and one noninverting. The recommended architecture shown in Figure 2 using three inverting op amps per channel provides isolation of the op amp inputs from charge dumped back from

the ADMOD79's input capacitors when these large capacitors switch. The performance from a two op amp per channel input structure may be adequate in many applications.

Layout and Decoupling Considerations

Obtaining the best possible performance from a state-of-the-art modulator like the ADMOD79 requires close attention to board layout. From extensive experimentation, Analog Devices has discovered principles that produce typical values of 103 dB dynamic range and 98 dB S/(THD+N) in target systems with an oversampling ratio of 64. The principles and their rationales are listed below in descending order of importance. The first two pertain to bypassing and are illustrated in Figure 4.

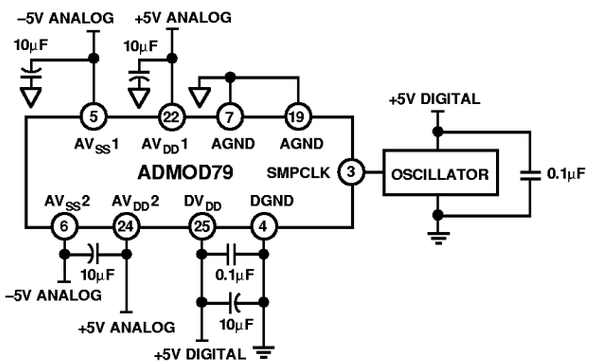


Figure 4. Recommended Bypassing and Oscillator Circuits

The digital bypassing of the ADMOD79 is a critical item on the board layout. The user should tie a bypass capacitor set (0.1 µF ceramic and 10 µF tantalum) on the DV_{DD} supply pin as close to the pin as possible. The trace between the package pin and the capacitors should be as short and as wide as possible. This will prevent digital supply current transients from being inductively transmitted to the inputs of the part.

The analog input bypassing is a second critical item. Use 0.01 µF NPO ceramic capacitors from each input pin to the analog ground plane, with a clear ground path from the bypass capacitor to the AGND pin on the same side of the package (Pins 7 and 19). The trace between this package pin and the capacitor should be as short and as wide as possible. A 0.0047 µF NPO ceramic capacitor should be placed between each set of input pins (11 to 12, and 17 to 18) to complete the input bypassing. This input bypassing minimizes the RF transmission and reception capability of the ADMOD79 inputs.

The ADMOD79 should be placed on a split ground plane as illustrated in Figure 5. The digital ground plane should be placed under the top end of the package and the analog ground plane should be placed under the bottom end of the package as shown in Figure 5. The split should be between Pins 4 and 5 and between Pins 24 and 25. The ground planes should be tied together at one spot underneath the center of the package. This ground plane technique also minimizes RF transmission and reception.

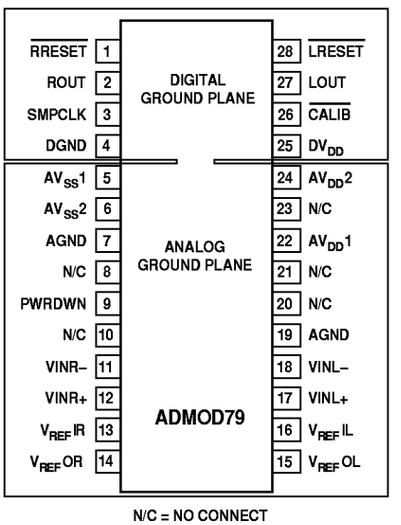


Figure 5. ADMOD79 Recommended Ground Plane

Each reference input pin (13 and 16) should be bypassed with a 200 Ω resistor and a 10 µF capacitor as shown in Figure 2. One end of the resistor should be placed as close to the package pin as possible, and the trace to it from the reference pin should be as short and as wide as possible. Keep this trace away from input pin traces! Coupling between input and reference traces will cause second harmonic distortion. The resistor is used to reduce the high-frequency coupling into the references from the board.

Wherever possible, minimize the capacitive load on digital outputs of the part. This will reduce the digital spike currents drawn from the digital supply pins.

Digital Timing

The delay from a SMPCLK falling edge to ROUT and LOUT data valid is t_{OPD}. The minimum SMPCLK LO pulse width is t_{SCPWL}, and the minimum SMPCLK HI pulse width is t_{SCPWH}. The minimum SMPCLK period is t_{SCP}. The delay from a SMPCLK rising edge to $\overline{\text{RRESET}}$ or $\overline{\text{LRESET}}$ is t_{RPD}. These timing relationships are shown in Figure 6.

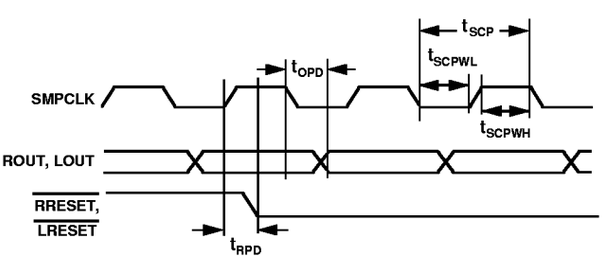
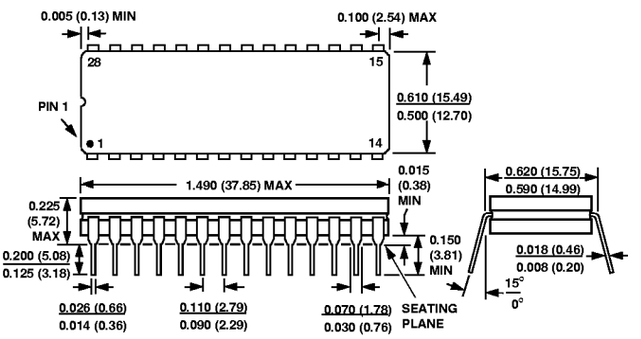


Figure 6. Digital Timing Diagram

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Q-28
28-Lead Cerdip



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