

DC Brushless Motor Driver Series for Cooling Fans

Low-voltage Single-phase Full-wave DC Brushless Fan Motor Drivers



BH6766FVM, BD6989FVM, BH6799FVM, BH6789FVM

●Description

This is the summary of models that suit for notebook PC cooling fan. They employ Bi-CMOS and Bi-CDMOS process, and realize low ON resistor, low power consumption, and quiet drive. They also incorporate lock protection and automatic restart circuit which does not require external capacitor.

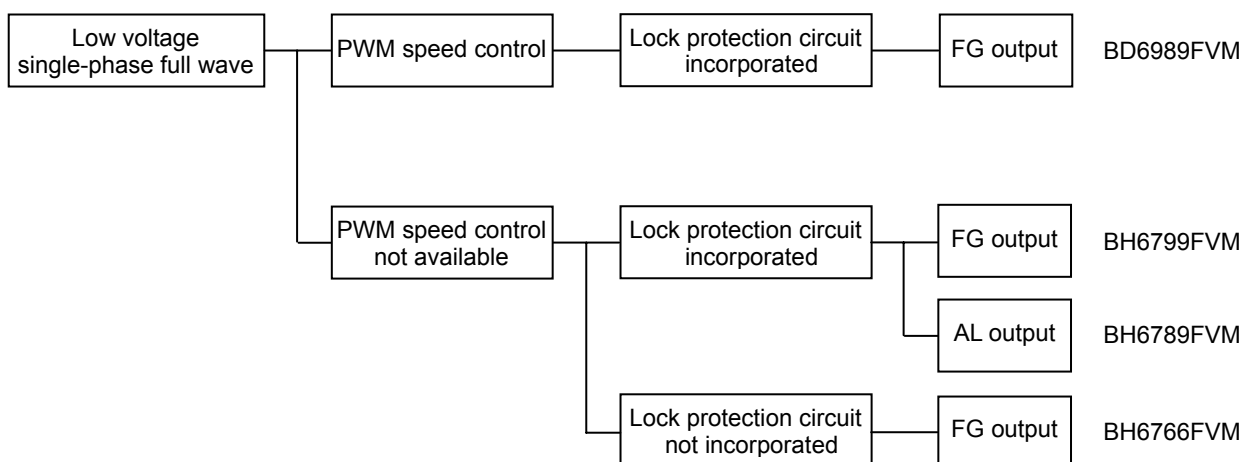
●Features

- 1) Soft switched drive
- 2) Incorporating lock protection and automatic restart circuit(BD6989FVM、BH6799FVM、BH6789FVM)
- 3) Rotating speed pulse signal (FG) output (BD6989FVM、BH6799FVM、BH6766FVM)
- 4) Lock alarm signal (AL) output (BH6789FVM)
- 5) PWM speed control (BD6989FVM)
- 6) MSOP8 compact package

●Applications

For compact 5V fan such as notebook PC cooling fan

●Lineup



● Absolute maximum ratings

◎BD6989FVM

Parameter	Symbol	Limit	Unit
Supply voltage	Vcc	10	V
Power dissipation	Pd	585 *	mW
Operating temperature	Topr	-40~+105	°C
Storage temperature	Tstg	-55~+150	°C
Output voltage	Vomax	10	V
Output current	Iomax	700 * *	mA
FG signal output current	IFG	10	mA
FG signal output voltage	VFG	10	V
Junction temperature	Tjmax	150	°C

- * Reduce by 4.68mW/°C over 25°C.
(70.0mm×70.0mm×1.6mm glass epoxy board)
- * * This value is not to exceed Pd.

◎BH6799FVM

Parameter	Symbol	Limit	Unit
Supply voltage	Vcc	7	V
Power dissipation	Pd	585 *	mW
Operating temperature	Topr	-40~+105	°C
Storage temperature	Tstg	-55~+150	°C
Output current	Iomax	1000 * *	mA
FG signal output current	IFG	5	mA
FG signal output voltage	VFG	7	V
Junction temperature	Tjmax	150	°C

- * Reduce by 4.68mW/°C over 25°C.
(70.0mm×70.0mm×1.6mm glass epoxy board)
- * * This value is not to exceed Pd.

◎BH6789FVM

Parameter	Symbol	Limit	Unit
Supply voltage	Vcc	7	V
Power dissipation	Pd	585 *	mW
Operating temperature	Topr	-40~+105	°C
Storage temperature	Tstg	-55~+150	°C
Output current	Iomax	1000 * *	mA
AL signal output current	IAL	5	mA
AL signal output voltage	VAL	7	V
Junction temperature	Tjmax	150	°C

- * Reduce by 4.68mW/°C over 25°C.
(70.0mm×70.0mm×1.6mm glass epoxy board)
- * * This value is not to exceed Pd.

◎BH6766FVM

Parameter	Symbol	Limit	Unit
Supply voltage	Vcc	7	V
Power dissipation	Pd	585 *	mW
Operating temperature	Topr	-40~+105	°C
Storage temperature	Tstg	-55~+150	°C
Output current	Iomax	600 * *	mA
FG signal output current	IFG	5	mA
FG signal output voltage	VFG	7	V
Junction temperature	Tjmax	150	°C

* Reduce by 4.68mW/°C over 25°C.
(70.0mm×70.0mm×1.6mm glass epoxy board)

* * This value is not to exceed Pd.

●OPERATING CONDITIONS

◎BD6989FVM

Parameter	Symbol	Limit	Unit
Operating supply voltage range	Vcc	2.9~8.0	V
Hall input voltage range	VH	0~Vcc-1.8	V

◎BH6799FVM, BH6789FVM

Parameter	Symbol	Limit	Unit
Operating supply voltage range	Vcc	2.0~6.0	V
Hall input voltage range	VH	0.4~Vcc-1.1	V

◎BH6766FVM

Parameter	Symbol	Limit	Unit
Operating supply voltage range	Vcc	2.0~6.0	V
Hall input voltage range	VH	0.4~Vcc-1.1	V

●ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta=25°C,Vcc=5V)

◎BD6989FVM

Parameter	Symbol	Limit			Unit	Conditions	Characteristics
		Min.	Typ.	Max.			
Circuit current	I _{cc}	-	4	6	mA		Fig.1
Input offset voltage	V _{HOFs}	-	-	±6	mV		-
PWM input H level	V _{PWMH}	2.5	-	V _{cc}	V		Fig.2
PWM input L level	V _{PWML}	0	-	0.7	V		Fig.3
Input frequency	F _{PWM}	0.02	-	50	kHz		-
Output voltage	V _O	-	0.4	0.6	V	I _o =250mA Upper and Lower total	Fig.4,5
Input-output Gain	G _{IO}	45	48	51	dB		-
FG low voltage	V _{FGL}	-	-	0.3	V	I _{FG} =3mA	Fig.6
FG leak current	I _{FGL}	-	-	20	μA	V _{FG} =10V	
Input hysteresis voltage	V _{HYS}	±5	±10	±15	mV		Fig.7
Lock detection ON time	T _{ON}	0.35	0.50	0.65	sec		Fig.8
Lock detection OFF time	T _{OFF}	3.5	5.0	6.5	sec		Fig.9

◎BH6799FVM, BH6789FVM

Parameter	Symbol	Limit			Unit	Conditions	Characteristics
		Min.	Typ.	Max.			
Circuit current	I _{cc}	-	5	8	mA		Fig.10
Input offset voltage	V _{HOFs}	-	-	±6	mV		-
Output voltage	V _O	-	0.32	0.49	V	I _o =250mA Upper and Lower total	Fig.11,12
Input-output Gain	G _{IO}	45	48	51	dB		-
FG low voltage	V _{FGL}	-	-	0.3	V	I _{FG} =3mA	Fig.13
AL low voltage	V _{ALL}	-	-	0.3	V	I _{AL} =3mA	Fig.14
Input hysteresis voltage	V _{HYS}	±5	±10	±15	mV		Fig.15
Lock detection ON time	T _{ON}	0.35	0.50	0.65	sec		Fig.16
Lock detection OFF time	T _{OFF}	3.5	5.0	6.5	sec		Fig.17
Hall bias voltage	V _{HB}	1.1	1.3	1.5	V	I _{HB} =5mA	Fig.18

◎BH6766FVM

Parameter	Symbol	Limit			Unit	Conditions	Characteristics
		Min.	Typ.	Max.			
Circuit current	I _{cc}	-	5	8	mA		Fig.19
Input offset voltage	V _{HOFs}	-	-	±6	mV		-
Output voltage	V _O	-	0.6	0.9	V	I _o =250mA Upper and Lower total	Fig.20,21
Input-output Gain	G _{IO}	45	48	51	dB		-
FG low voltage	V _{FGL}	-	-	0.3	V	I _{FG} =3mA	Fig.22
Input hysteresis voltage	V _{HYS}	±5	±10	±15	mV		Fig.23
Hall bias voltage	V _{HB}	1.1	1.3	1.5	V	I _{HB} =5mA	Fig.24

● Reference Data

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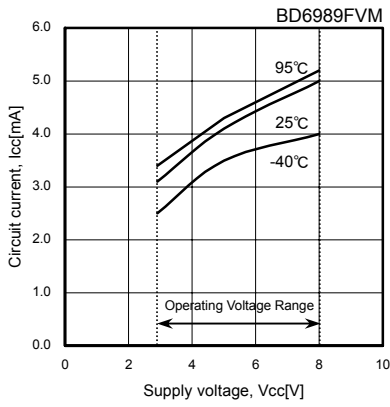


Fig.1 Circuit current

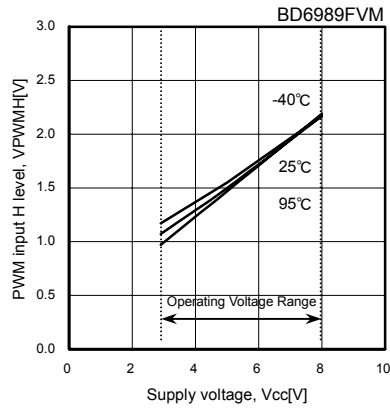


Fig.2 PWM input H level

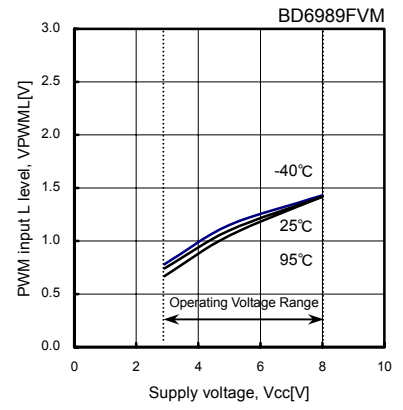


Fig.3 PWM input L level

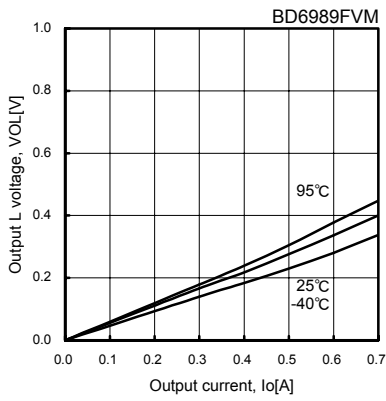


Fig.4 Output L voltage

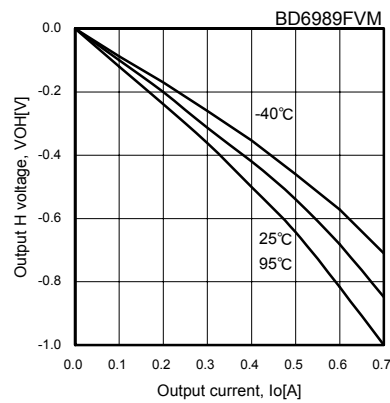


Fig.5 Output H voltage

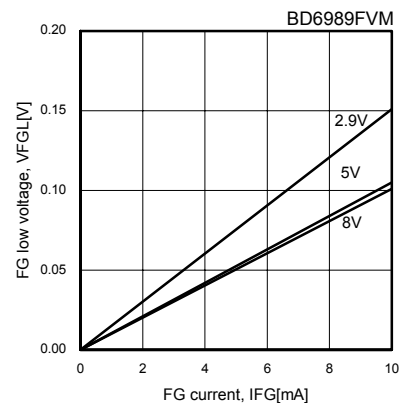


Fig.6 FG low voltage

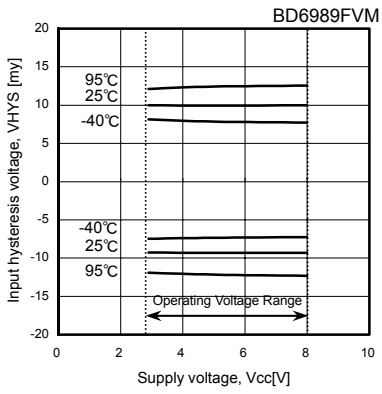


Fig.7 Input hysteresis voltage

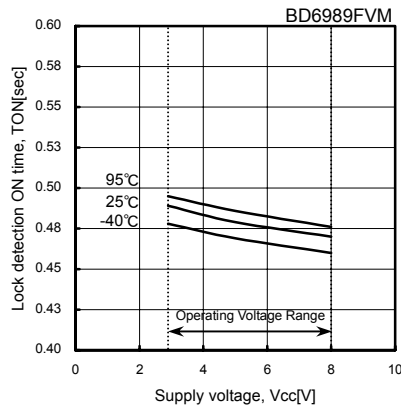


Fig.8 Lock detection ON time

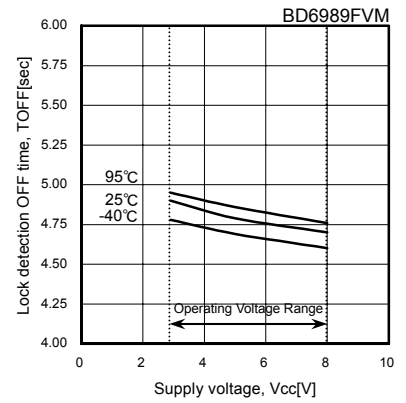


Fig.9 Lock detection OFF time

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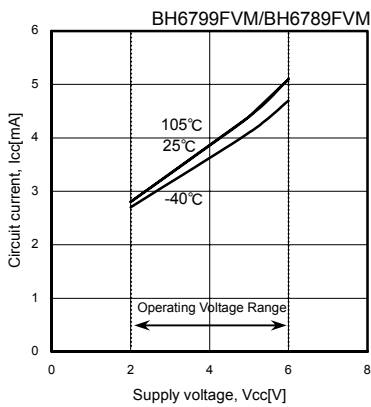


Fig.10 Circuit current

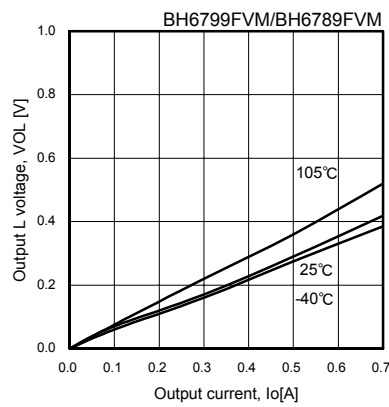


Fig.11 Output L voltage

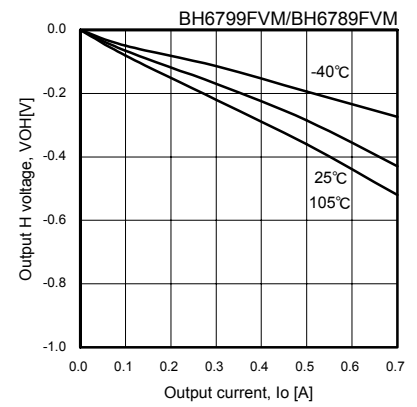


Fig.12 Output H voltage

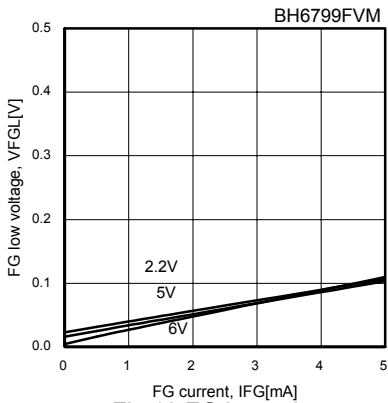


Fig.13 FG low voltage

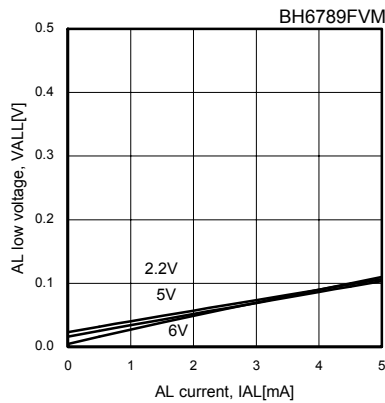


Fig.14 AL low voltage

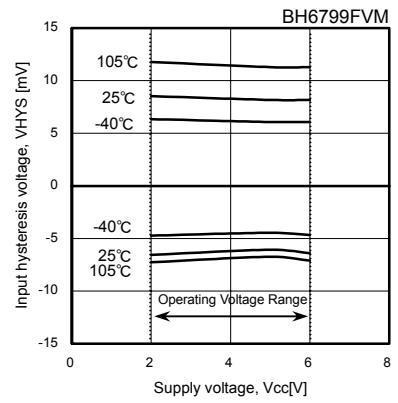


Fig.15 Input hysteresis voltage

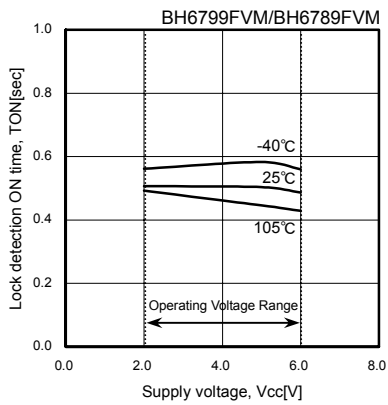


Fig.16 Lock detection ON time

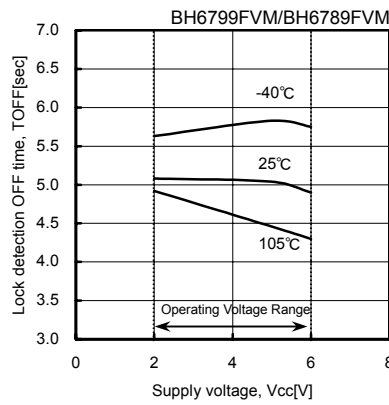


Fig.17 Lock detection OFF time

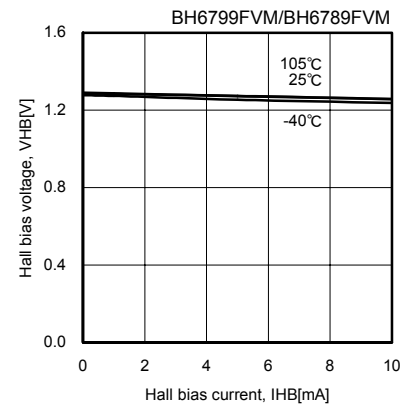


Fig.18 Hall bias voltage

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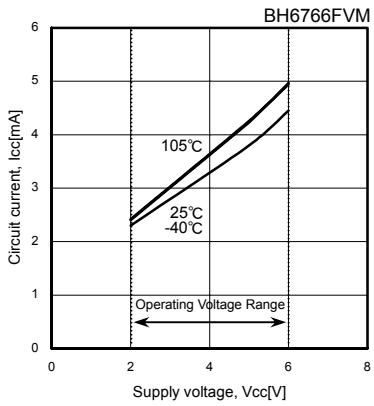


Fig.19 Circuit current

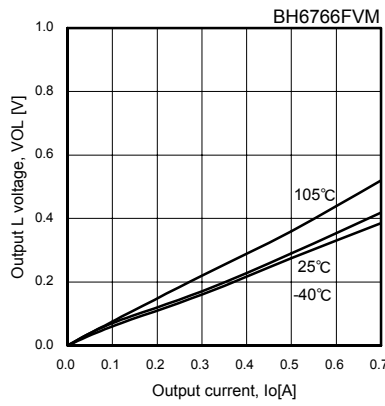


Fig.20 Output L voltage

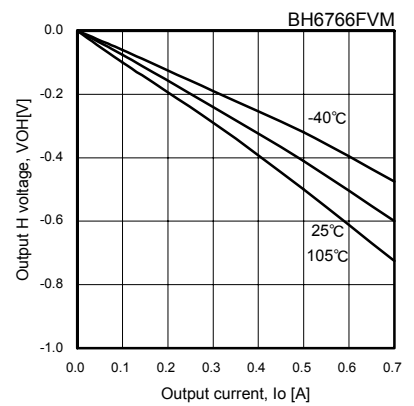


Fig.21 Output H voltage

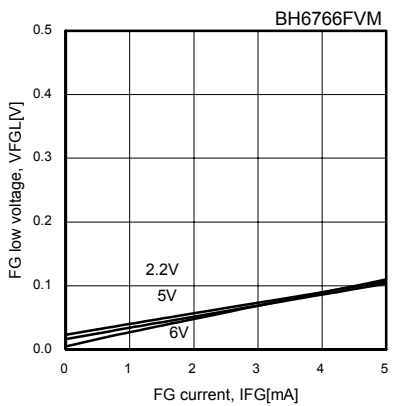


Fig.22 FG low voltage

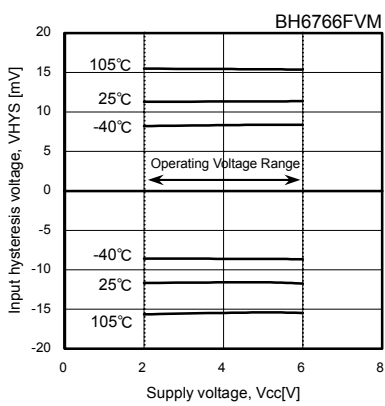


Fig.23 Input hysteresis voltage

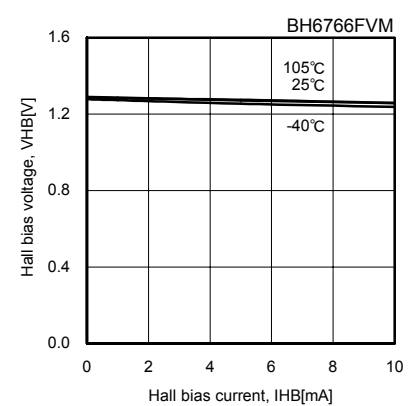
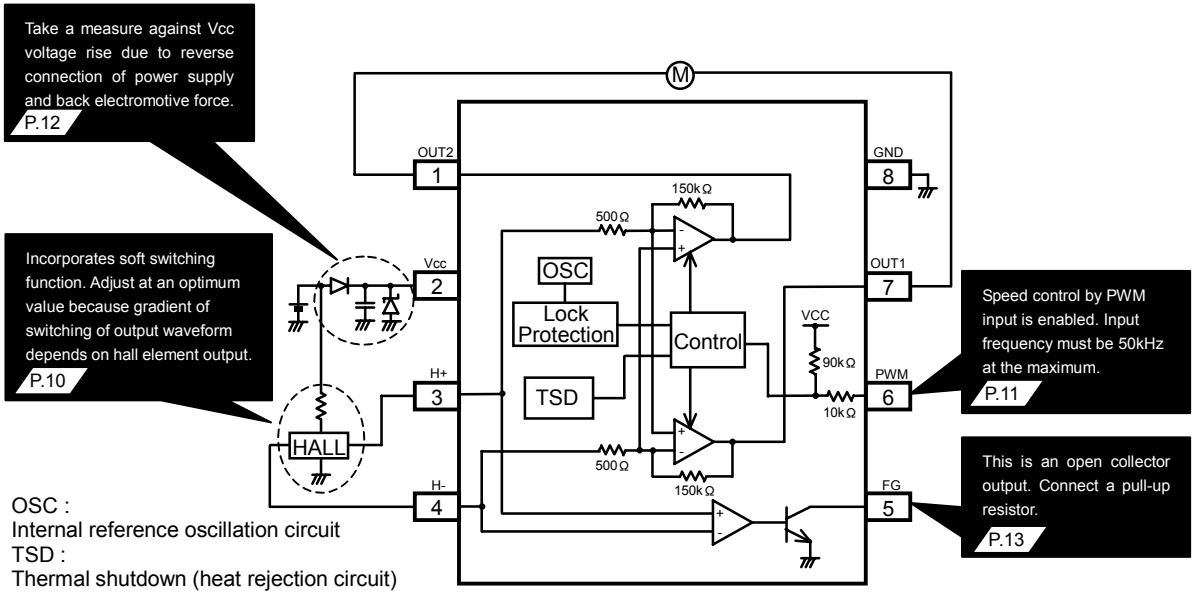


Fig.24 Hall bias voltage

●Block diagram, application circuit, and pin assignment(Constant etc are for reference)

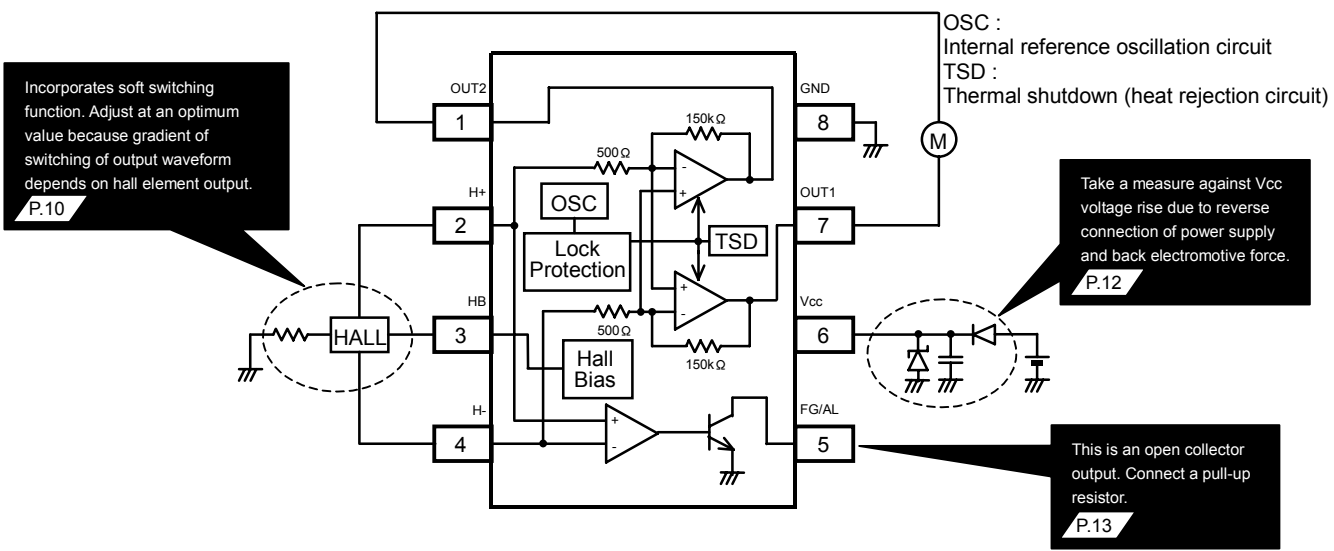
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OSC :
Internal reference oscillation circuit
TSD :
Thermal shutdown (heat rejection circuit)

PIN No.	Terminal name	Function
1	OUT2	Motor output terminal 2
2	Vcc	Power supply terminal
3	H+	Hall input terminal+
4	H-	Hall input terminal-
5	FG	FG signal output terminal
6	PWM	PWM signal input terminal
7	OUT1	Motor output terminal 1
8	GND	GND terminal

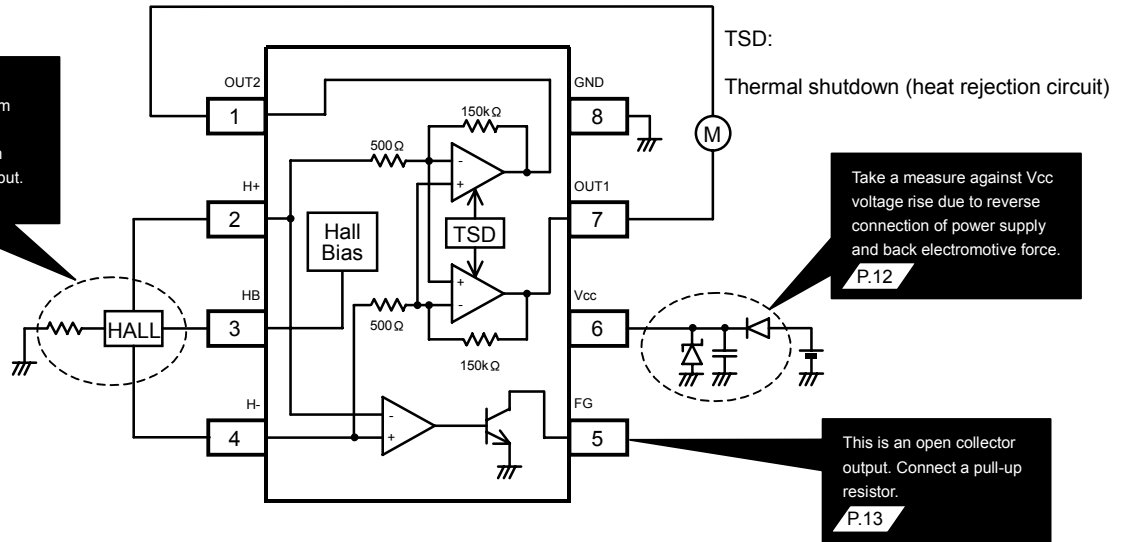
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OSC :
Internal reference oscillation circuit
TSD :
Thermal shutdown (heat rejection circuit)

PIN No.	Terminal name	Function
1	OUT2	Motor output terminal 2
2	H+	Hall input terminal+
3	HB	Hall bias terminal
4	H-	Hall input terminal-
5	FG/AL	FG/AL signal output terminal
6	Vcc	Power supply terminal
7	OUT1	Motor output terminal 1
8	GND	GND terminal

Incorporates soft switching function. Adjust at an optimum value because gradient of switching of output waveform depends on hall element output.
P.10



PIN No.	Terminal name	Function
1	OUT2	Motor output terminal 2
2	H+	Hall input terminal+
3	HB	Hall bias terminal
4	H-	Hall input terminal-
5	FG	FG signal output terminal
6	Vcc	Power supply terminal
7	OUT1	Motor output terminal 1
8	GND	GND terminal

● Truth table

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H+	H-	PWM	OUT1	OUT2	FG
H	L	H(OPEN)	H	L	L(Output Tr : ON)
L	H	H(OPEN)	L	H	H(Output Tr : OFF)
H	L	L	L	L	L(Output Tr : ON)
L	H	L	L	L	H(Output Tr : OFF)

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H+	H-	OUT1	OUT2	FG
H	L	H	L	L(Output Tr : ON)
L	H	L	H	H(Output Tr : OFF)

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H+	H-	OUT1	OUT2	FG
H	L	H	L	H(Output Tr : OFF)
L	H	L	H	L(Output Tr : ON)

●Description of operations

Function table

	BD6989FVM	BH6799FVM	BH6789FVM	BH6766FVM	Reference page
Lock protection and auto restart circuit	○	○	○		P.9
Soft switching	○	○	○	○	P.10
PWM speed control	○				P.11
FG output	○	○		○	P.13
AL output			○		P.13

1) Lock protection and automatic restart circuit <BD6989FVM, BH6799FVM, BH6789FVM>

Motor rotation is detected by hall signal, and lock detection ON time (TON) and lock detection OFF time (TOFF) are set by IC internal counter. External part (C or R) is not required. Timing chart is shown in Fig.25.

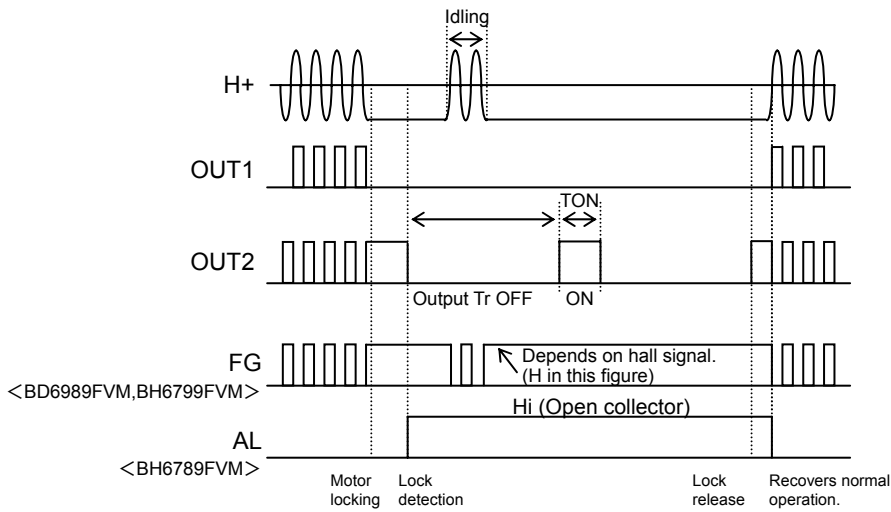


Fig.25 Lock protection timing chart

* In the case of BD6989FVM, lock protection function is turned off when the time of PWM = L has elapsed more than 66.5 ms (typ.) in order to disable lock protection function when the motor is stopped by PWM input signal.

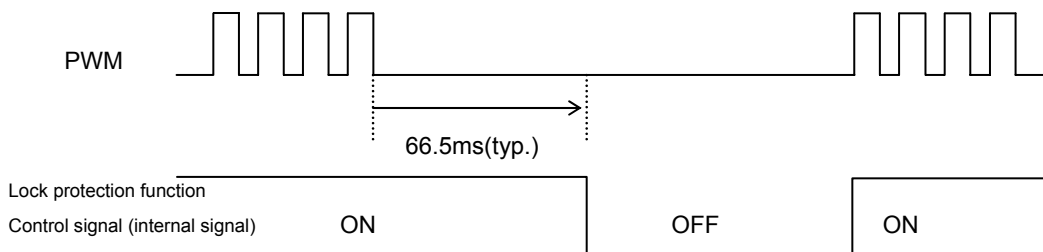


Fig.26 PWM signal and lock protection operation <BD6989FVM>

When H level duty of PWM input signal is close to 0%, lock protection function does not work at an input frequency slower than 15Hz (typ.), therefore enter a frequency faster than 20Hz.

2) Soft switching (silent drive setting)

Input signal to hall amplifier is amplified to produce an output signal.

When the hall element output signal is small, the gradient of switching of output waveform is gentle; When it is large, the gradient of switching of output waveform is steep. Gain of 300 times (typ.) is provided between input and output. Enter an appropriate hall element output to IC where output waveform swings sufficiently.

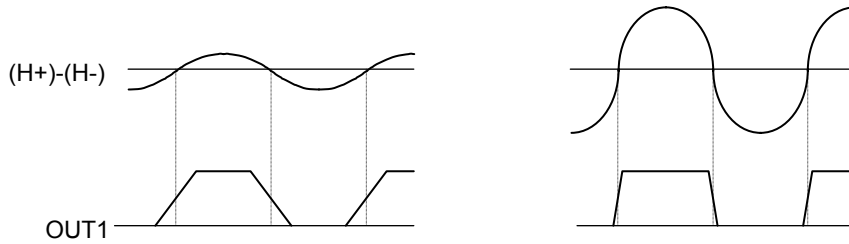


Fig.27 Relation between hall element output amplitude and output waveform

3) Hall input setting

Hall input voltage range is shown in operating conditions.

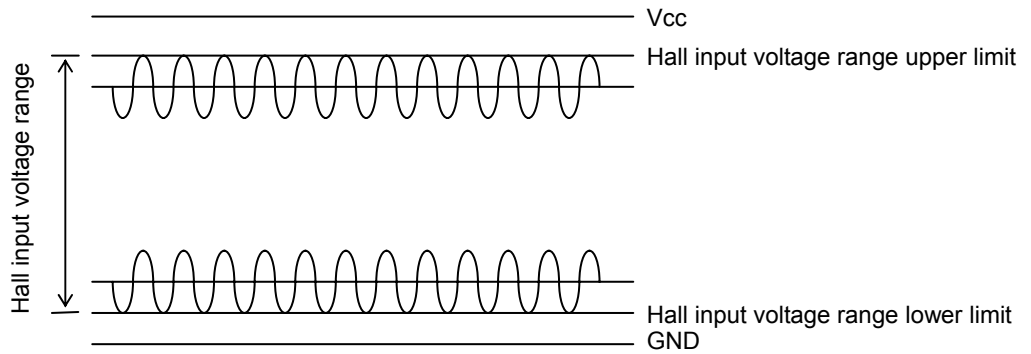
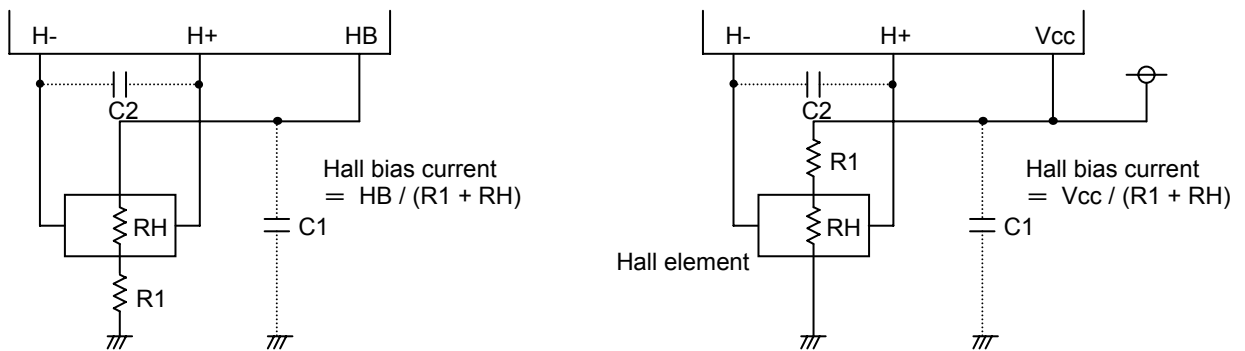


Fig.28 Hall input voltage range

Adjust the value of hall element bias resistor R1 in Fig.29 so that the input voltage of a hall amplifier is input in "hall input voltage range" including signal amplitude.

○Reducing the noise of hall signal

Hall element may be affected by Vcc noise depending on the wiring pattern of board. In this case, place a capacitor like C1 in Fig.29. In addition, when wiring from the hall element output to IC hall input is long, noise may be loaded on wiring. In this case, place a capacitor like C2 in Fig.29.



<BH6799FVM, BH6789FVM, BH6766FVM>

<BD6989FVM>

Fig.29 Application near of hall signal

4) PWM input <BD6989FVM>

Rotation speed of motor can be changed by controlling ON/OFF of the upper output depending on duty of the signal input to PWM terminal.

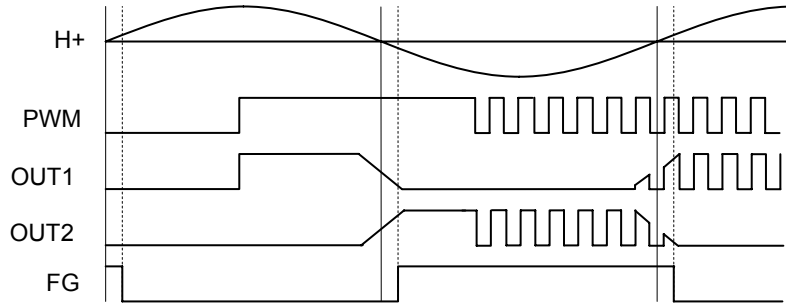


Fig.30 Timing chart in PWM control

When the voltage input to PWM terminal applies H logic : normal operation
L logic : H side output is off

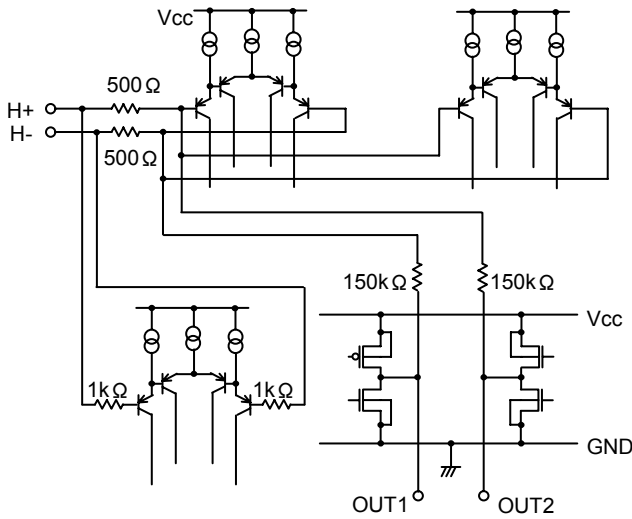
When PWM terminal is open, H logic is applied.
PWM terminal has hysteresis of 400mV (typ.).

●Equivalent circuit

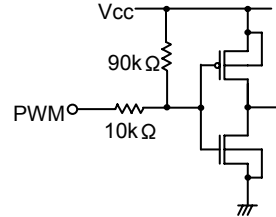
Resistance is a typical value.

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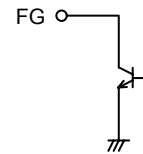
1) Hall input terminal, Motor output terminal



2) PWM signal input terminal

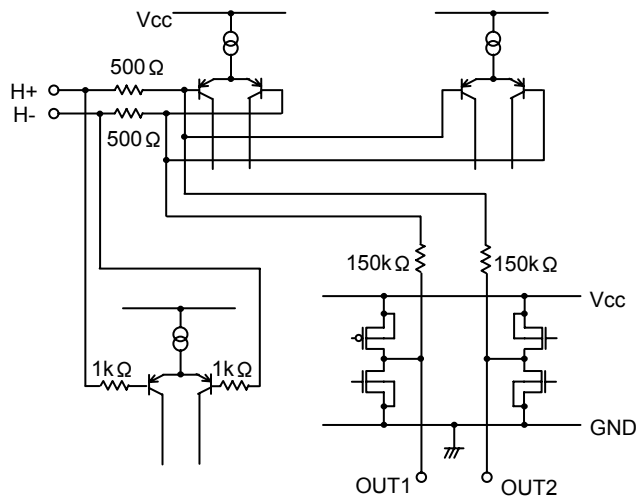


3) FG output terminal

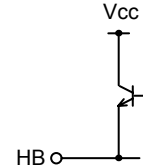


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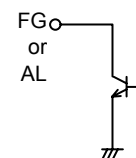
1) Hall input terminal, Motor output terminal



2) Hall bias terminal



3) FG output terminal or AL output terminal



● Safety measure

1) Reverse connection protection diode

Reverse connection of power results in IC destruction as shown in Fig.31. When reverse connection is possible, reverse connection protection diode must be added between power supply and Vcc.

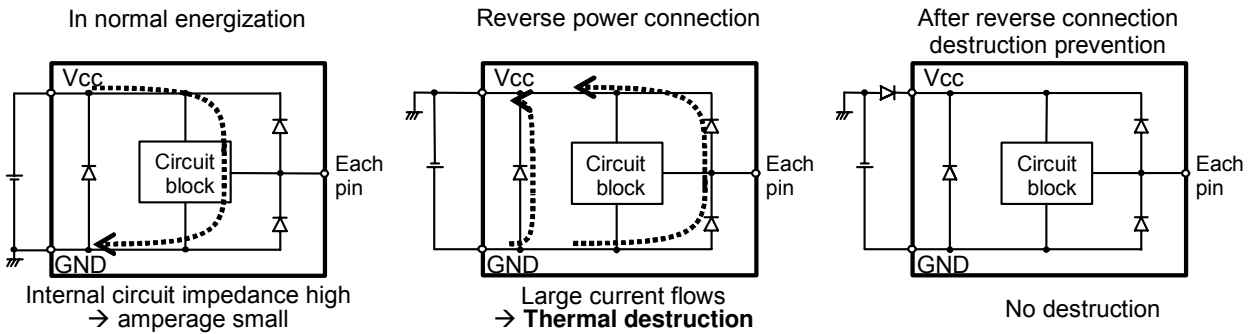


Fig.31 Flow of current when power is connected reversely

2) Measure against Vcc voltage rise by back electromotive force

Back electromotive force (Back EMF) generates regenerative current to power supply. However, when reverse connection protection diode is connected, Vcc voltage rises because the diode prevents current flow to power supply.

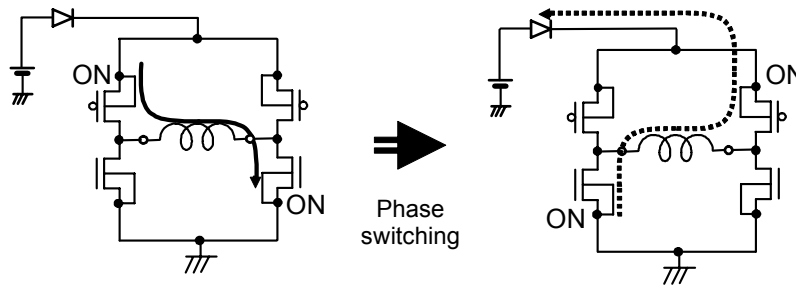


Fig.32 Vcc voltage rise by back electromotive force

When the absolute maximum rated voltage may be exceeded due to voltage rise by back electromotive force, place (A) Capacitor or (B) Zener diode between Vcc and GND. If necessary, add both (C).

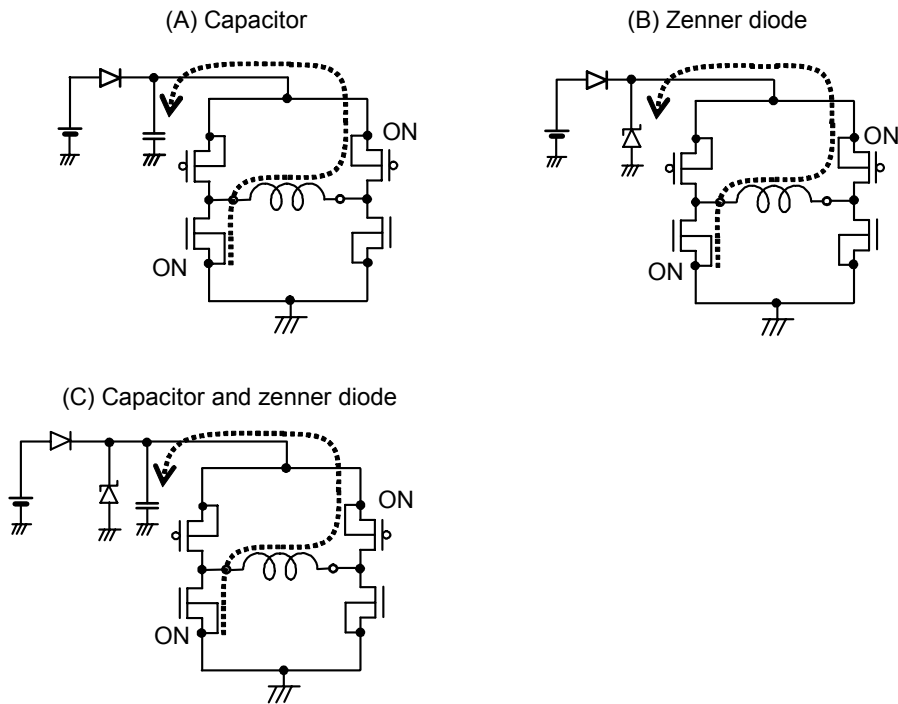


Fig.33 Measure against Vcc voltage rise

3) Problem of GND line PWM switching

Do not perform PWM switching of GND line because GND terminal potential cannot be kept to a minimum.

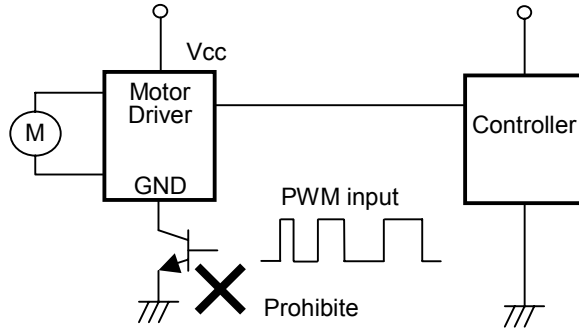


Fig.34 GND Line PWM switching prohibited

4) FG and AL output

FG and AL output is an open collector and requires pull-up resistor.

The IC can be protected by adding resistor R1. An excess of absolute maximum rating, when FG or AL output terminal is directly connected to power supply, could damage the IC.

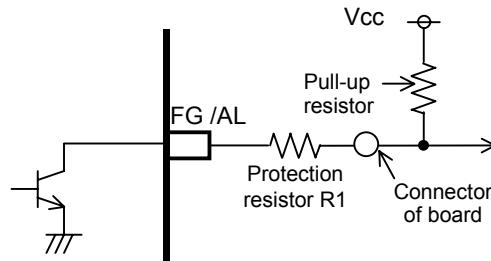


Fig.35 Protection of FG and AL terminal

● Calculation of power consumed by IC

Power consumed by this IC P_c is approximately calculated as follows:

$$P_c = P_{c1} + P_{c2} + P_{c3}$$

- P_{c1} : Power consumption by circuit current

$$P_{c1} = V_{cc} \times I_{cc}$$

- P_{c2} : Power consumption at output stage

$$P_{c2} = V_{OL} \times I_o + V_{OH} \times I_o$$

V_{OL} is L voltage of output terminal 1 and 2.

V_{OH} is H voltage of output terminal 1 and 2.

I_o is the current flowing to output terminal 1 and 2.

- P_{c3} : Power consumption at FG and AL

$$P_{c3} = V_{FG} \times I_{FG} + V_{AL} \times I_{AL}$$

V_{FG} is L voltage of FG output.

V_{AL} is L voltage of AL output.

I_{FG} and I_{AL} are the current of FG and AL.

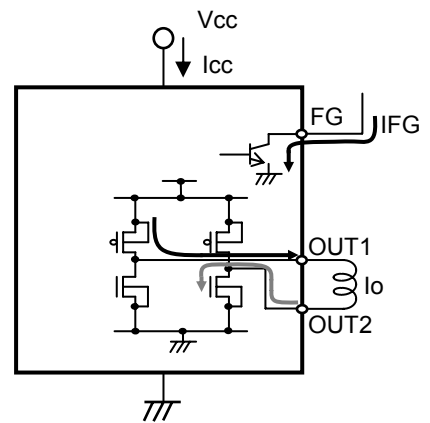


Fig.36 Calculation of power consumed by IC

Power consumption by IC greatly changes with use condition of IC such as power supply voltage and output current. Consider thermal design so that the maximum power dissipation on IC package is not exceeded.

● Thermal derating curve

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta = 25°C (normal temperature). IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, etc, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is in general equal to the maximum value in the storage temperature range.

Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called heat resistance, represented by the symbol θ_{ja} [°C/W]. The temperature of IC inside the package can be estimated by this heat resistance. Fig.37 shows the model of heat resistance of the package.

Heat resistance θ_{ja} , ambient temperature Ta, junction temperature Tj, and power consumption P can be calculated by the equation below:

$$\theta_{ja} = (T_j - T_a) / P \quad [^{\circ}\text{C}/\text{W}]$$

Thermal derating curve indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} .

Thermal resistance θ_{ja} depends on chip size, power consumption, package ambient temperature, packaging condition, wind velocity, etc., even when the same package is used. Thermal derating curve indicates a reference value measured at a specified condition. Fig.38 shows a thermal derating curve (Value when mounting FR4 glass epoxy board 70 [mm] x 70 [mm] x 1.6 [mm] (copper foil area below 3 [%]))

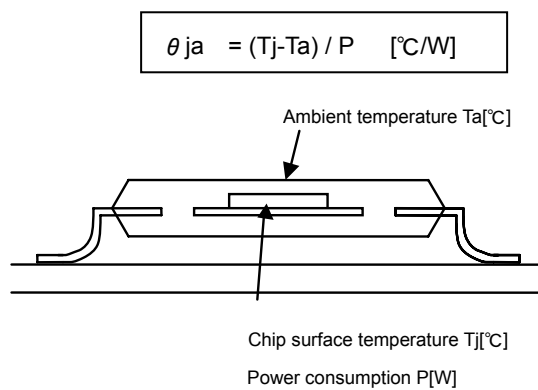


Fig.37 Thermal resistance

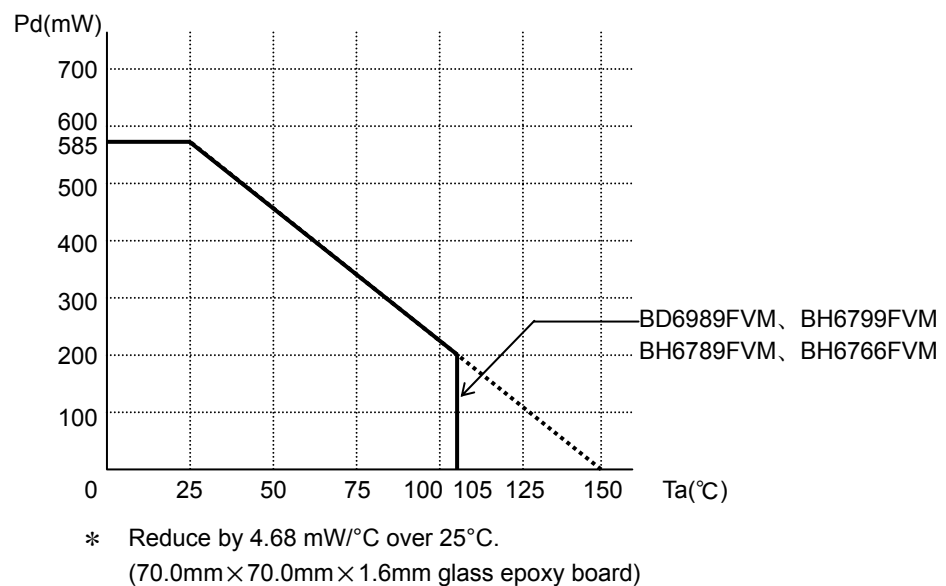


Fig.38 Thermal derating curve

●Cautions on use

1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3) Power supply line

Back electromotive force causes regenerated current to power supply line, therefore take a measure such as placing a capacitor between power supply and GND for routing regenerated current. And fully ensure that the capacitor characteristics have no problem before determine a capacitor value. (when applying electrolytic capacitors, capacitance characteristic values are reduced at low temperatures)

4) GND potential

The potential of GND pin must be minimum potential in all operating conditions. Also ensure that all terminals except GND terminal do not fall below GND voltage including transient characteristics. However, it is possible that the motor output terminal may deflect below GND because of influence by back electromotive force of motor. Malfunction may possibly occur depending on use condition, environment, and property of individual motor. Please make fully confirmation that no problem is found on operation of IC.

5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation(Pd) in actual operating conditions.

6) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9) Thermal shut down circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). Operation temperature is 175°C(typ.) and has a hysteresis width of 25°C(typ.). When IC chip temperature rises and TSD circuit works, the output terminal becomes an open state. TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operation this circuit or use the IC in an environment where the operation of this circuit is assumed.

10) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

11) GND wiring pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

12) Capacitor between output and GND

When a large capacitor is connected between output and GND, if Vcc is shorted with 0V or GND for some cause, it is possible that the current charged in the capacitor may flow into the output resulting in destruction. Keep the capacitor between output and GND below 100uF.

13) IC terminal input

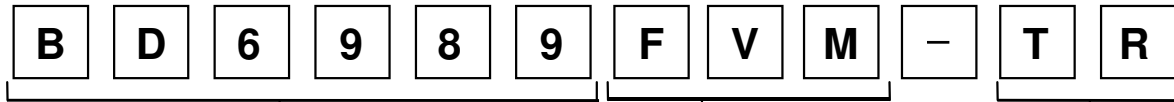
When Vcc voltage is not applied to IC, do not apply voltage to each input terminal. When voltage above Vcc or below GND is applied to the input terminal, parasitic element is actuated due to the structure of IC. Operation of parasitic element causes mutual interference between circuits, resulting in malfunction as well as destruction in the last. Do not use in a manner where parasitic element is actuated.

14) In use

We are sure that the example of application circuit is preferable, but please check the character further more in application to a part which requires high precision. In using the unit with external circuit constant changed, consider the variation of externally equipped parts and our IC including not only static character but also transient character and allow sufficient margin in determining.

● Ordering part number

· Please order by ordering part number. · Please confirm the combination of each items. · Please write the letter close to left when column is blank.



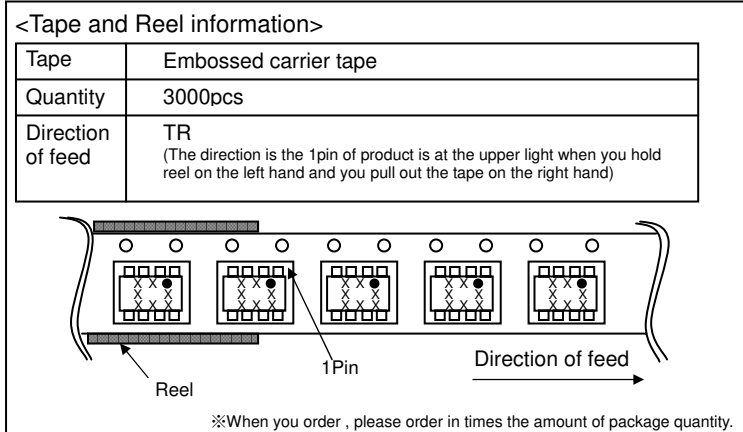
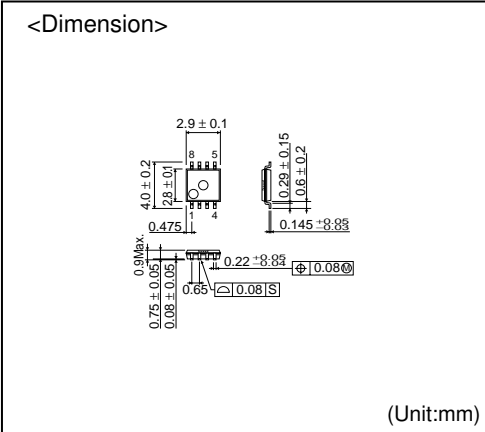
Part Number
 · BD6989 · BH6799
 · BH6789 · BH6766

Package Type
 · FVM : MSOP8

TR Emboss tape reel Pin 1 opposite draw-out side

● PHYSICAL DIMENSION

MSOP8



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ROHM CO., LTD.

21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto
 615-8585, Japan
 TEL: +81-75-311-2121 FAX: +81-75-315-0172
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