

SN5406, SN5416, SN7406, SN7416 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

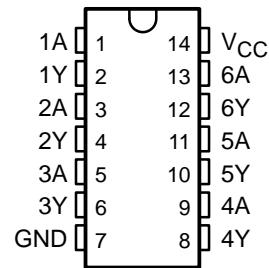
SDLS031A – DECEMBER 1983 – REVISED DECEMBER 2001

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Drivers for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

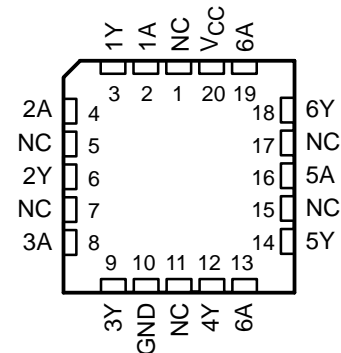
description

These TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays), and also are characterized for use as inverter buffers for driving TTL inputs. The SN5406 and SN7406 have minimum breakdown voltages of 30 V. The SN5416 and SN7416 have minimum breakdown voltages of 15 V. The maximum sink current is 30 mA for the SN5406 and SN5416, and 40 mA for the SN7406 and SN7416.

SN5406, SN5416 . . . J OR W PACKAGE
SN7406 . . . D, N, OR NS PACKAGE
SN7416 . . . D OR N PACKAGE
(TOP VIEW)



SN5406 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------------|------------------|
| 0°C to 70°C | SOIC – D | Tube | SN7406D | 7406 |
| | | Tape and reel | SN7406DR | |
| | | Tube | SN7416D | 7416 |
| | | Tape and reel | SN7416DR | |
| | PDIP – N | Tube | SN7406N | SN7406N |
| | | | | SN7416N |
| | SOP – NS | Tape and reel | SN7406NSR | SN7406 |
| –55°C to 125°C | CDIP – J | Tube | SNJ5406J | SNJ5406J |
| | | Tube | SNJ5416J | SNJ5416J |
| | CDIP – W | Tube | SNJ5406W | SNJ5406W |
| | | Tube | SNJ5416W | SNJ5416W |
| | LCCC – FK | Tube | SNJ5406FK | SNJ5406FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

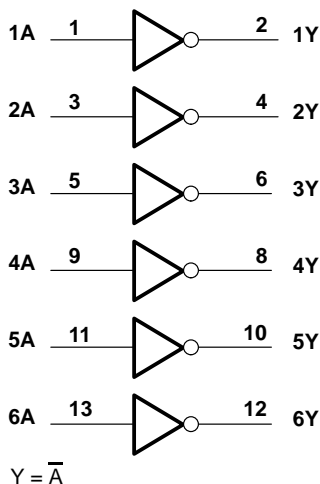
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

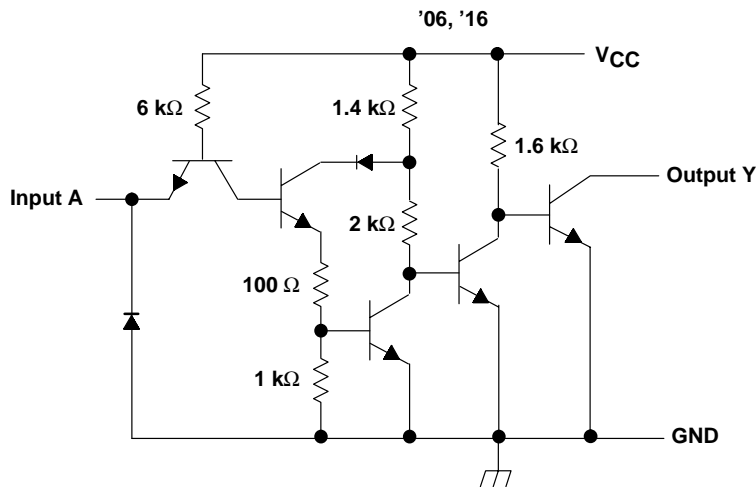
SN5406, SN5416, SN7406, SN7416
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

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logic diagram (positive logic)



schematic (each buffer/driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I (see Note 1) | 5.5 V |
| Output voltage, V_O (see Notes 1 and 2): SN5406, SN7406 | 30 V |
| SN5416, SN7416 | 15 V |
| Package thermal impedance, θ_{JA} (see Note 3): D package | 86°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
 2. This is the maximum voltage which should be applied to any output when it is in the off state.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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HEX INVERTER BUFFERS/DRIVERS
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recommended operating conditions

| | | SN5406 SN5416 | | | SN7406 SN7416 | | | UNIT | | |
|-----------------|--------------------------------|------------------|-----|-----|------------------|-----|------|------|----|----|
| | | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | | |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V | | |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V | | |
| V _{OH} | High-level output voltage | | | | 30 | | | V | | |
| | | | | | 15 | | | | | |
| I _{OL} | Low-level output current | | | | 30 | | | 40 | mA | |
| T _A | Operating free-air temperature | -55 | | | 125 | | | 0 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN5406 SN5416 | | | SN7406 SN7416 | | | UNIT | |
|------------------|---|-------------------------|------|------|------------------|------|------|------|----|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V _{IK} | V _{CC} = MIN, I _I = -12 mA | | | -1.5 | | | -1.5 | V | |
| I _{OH} | V _{CC} = MIN, V _{IL} = 0.8 V, V _{OH} = § | | | 0.25 | | | 0.25 | mA | |
| V _{OL} | V _{CC} = MIN, V _{IH} = 2 V | I _{OL} = 16 mA | | | 0.4 | | | V | |
| | | I _{OL} = ¶ | | | 0.7 | | | | |
| I _I | V _{CC} = MAX, V _I = 5.5 V | | | 1 | | | 1 | mA | |
| I _{IH} | V _{CC} = MAX, V _{IH} = 2.4 V | | | 40 | | | 40 | µA | |
| I _{IL} | V _{CC} = MAX, V _{IL} = 0.4 V | | | -1.6 | | | -1.6 | mA | |
| I _{CCH} | V _{CC} = MAX | | | 30 | | | 30 | 48 | mA |
| I _{CCL} | V _{CC} = MAX | | | 32 | | | 32 | 51 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ V_{OH} = 30 V for '06 and 15 V for '16.

¶ I_{OL} = 30 mA for SN54' and 40 mA for SN74'.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

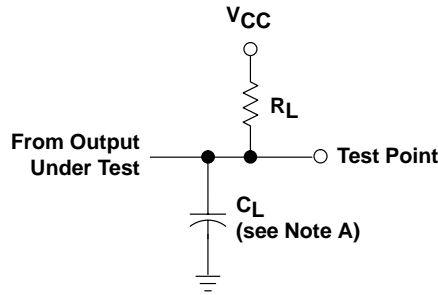
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|--|-----|-----|-----|------|
| t _{PLH} | A | Y | R _L = 110 Ω, C _L = 15 pF | | 10 | 15 | ns |
| t _{PHL} | | | | | 15 | 23 | |



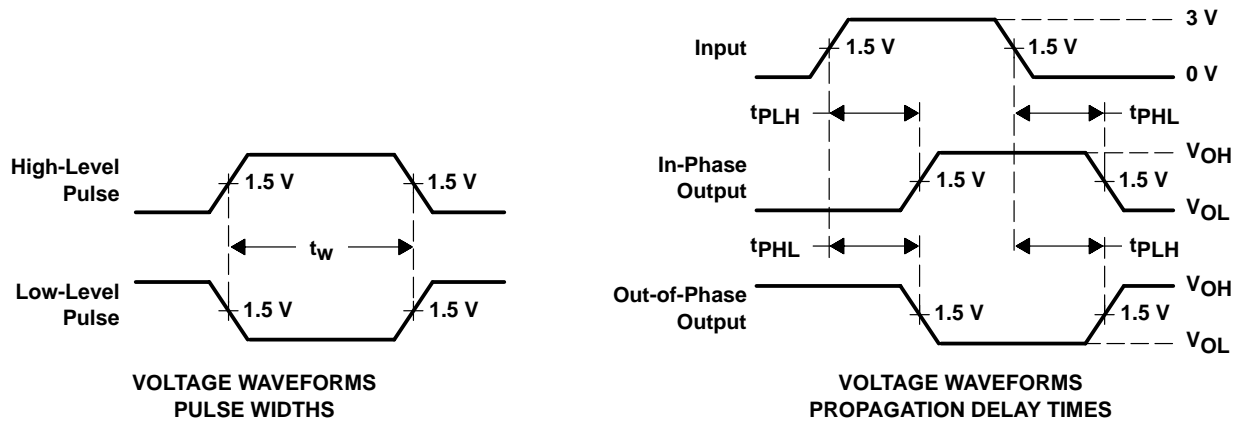
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 7$ ns, $t_f \leq 7$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/00801BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 00801BCA | Samples |
| JM38510/00801BDA | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 00801BDA | Samples |
| M38510/00801BCA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 00801BCA | Samples |
| M38510/00801BDA | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 00801BDA | Samples |
| SN5406J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN5406J | Samples |
| SN5416J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN5416J | Samples |
| SN7406D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7406 | Samples |
| SN7406DE4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7406 | Samples |
| SN7406DG4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7406 | Samples |
| SN7406DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7406 | Samples |
| SN7406DRE4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7406 | Samples |
| SN7406DRG4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7406 | Samples |
| SN7406N | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN7406N | Samples |
| SN7406NE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN7406N | Samples |
| SN7406NSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN7406 | Samples |
| SN7416D | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7416 | Samples |
| SN7416DE4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7416 | Samples |
| SN7416DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7416 | Samples |
| SN7416N | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN7416N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN7416NSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN7416 | Samples |
| SNJ5406FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ5406FK | Samples |
| SNJ5406J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ5406J | Samples |
| SNJ5406W | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ5406W | Samples |
| SNJ5416J | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ5416J | Samples |
| SNJ5416W | ACTIVE | CFP | W | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ5416W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN5406, SN5416, SN7406, SN7416 :

- Catalog : [SN7406](#), [SN7416](#)
- Military : [SN5406](#), [SN5416](#)

NOTE: Qualified Version Definitions:

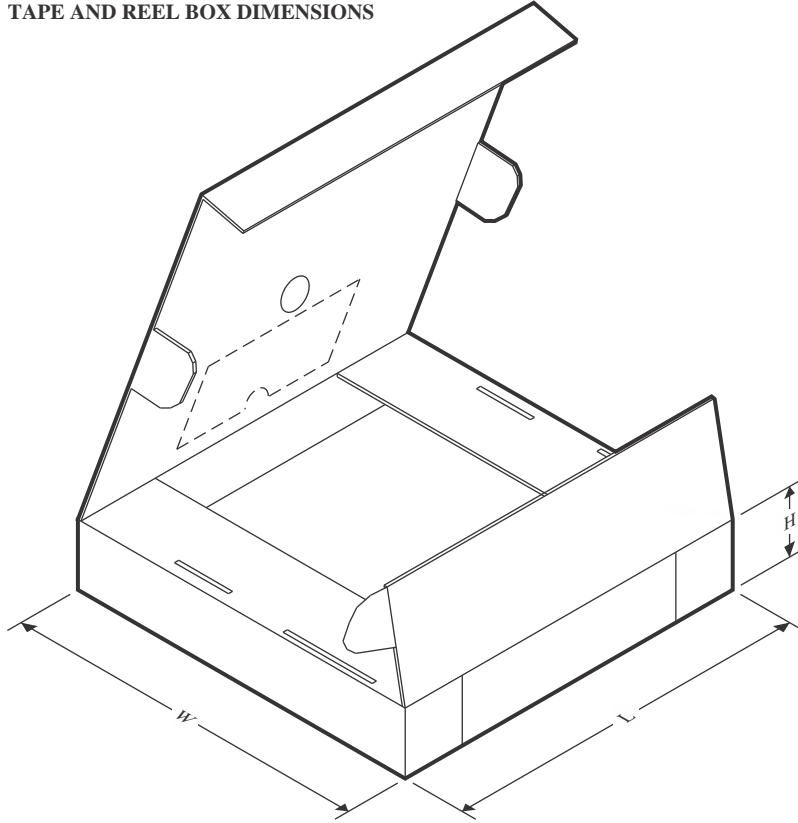
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

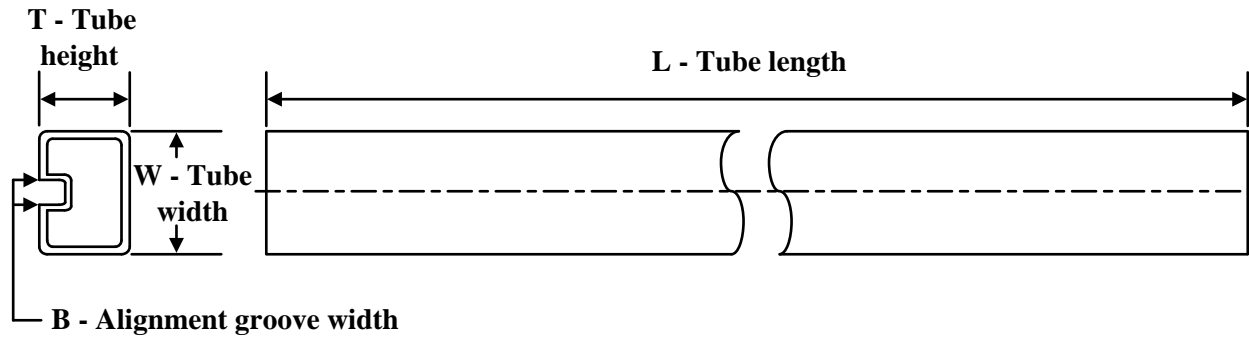

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN7406DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN7406DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN7406DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN7406NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN7416DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN7416NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN7406DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN7406DRG4 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN7406DRG4 | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN7406NSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN7416DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN7416NSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| JM38510/00801BDA | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |
| M38510/00801BDA | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN7406D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN7406DE4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN7406DG4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN7406N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN7406N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN7406NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN7406NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN7416D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN7416DE4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN7416N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN7416N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ5406FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ5406W | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |
| SNJ5416W | W | CFP | 14 | 1 | 506.98 | 26.16 | 6220 | NA |

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

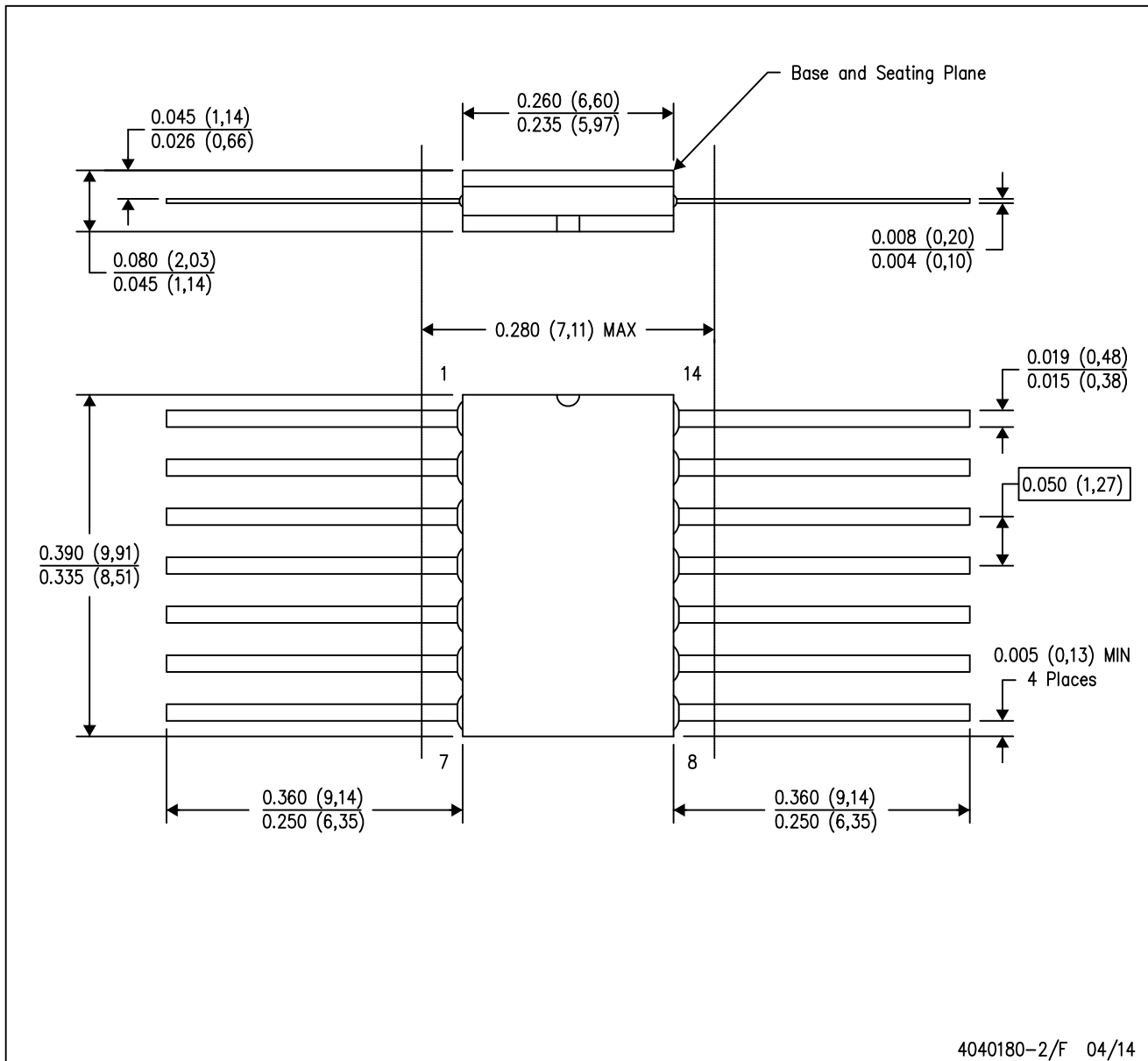
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

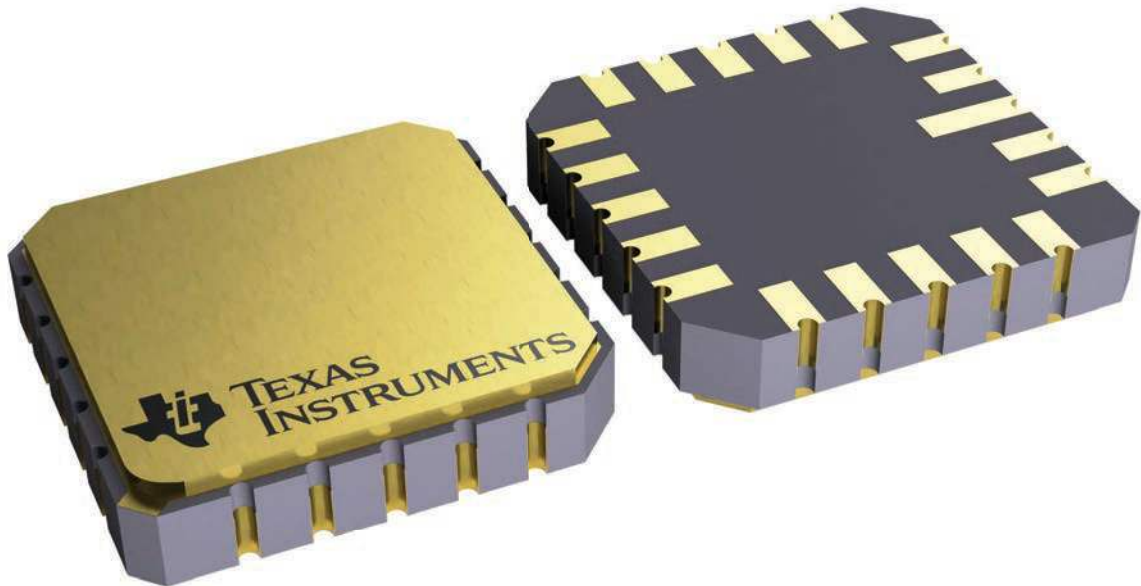
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

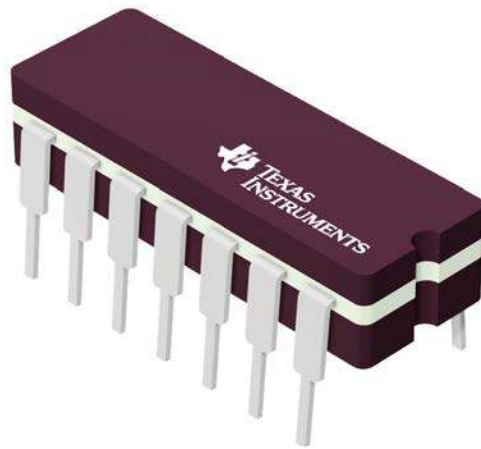
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

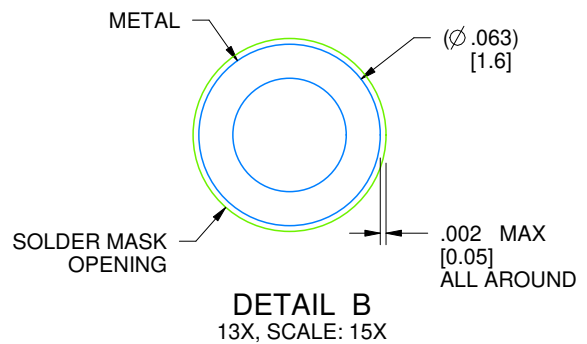
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



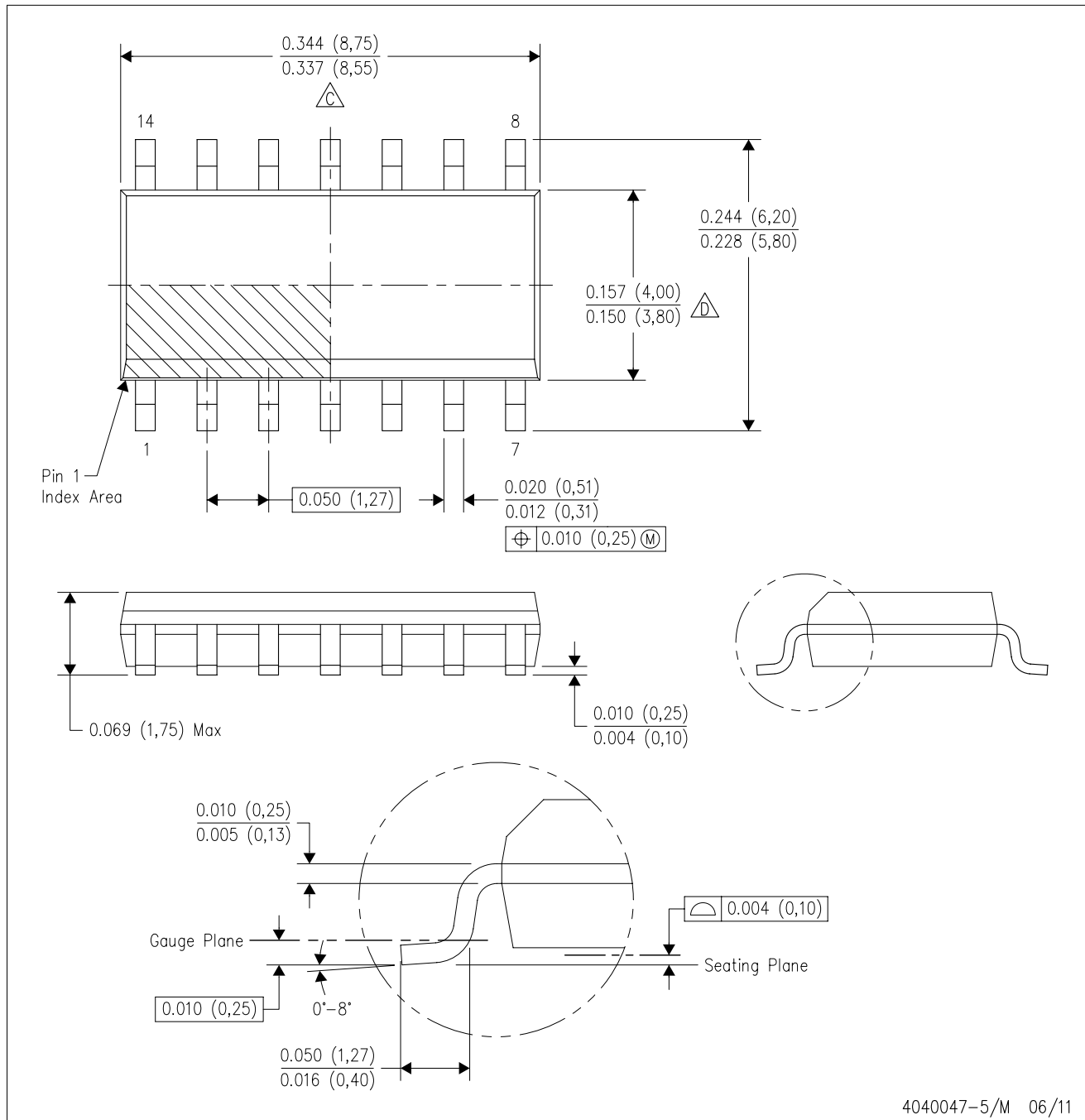
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X





4214771/A 05/2017

D (R-PDSO-G14)

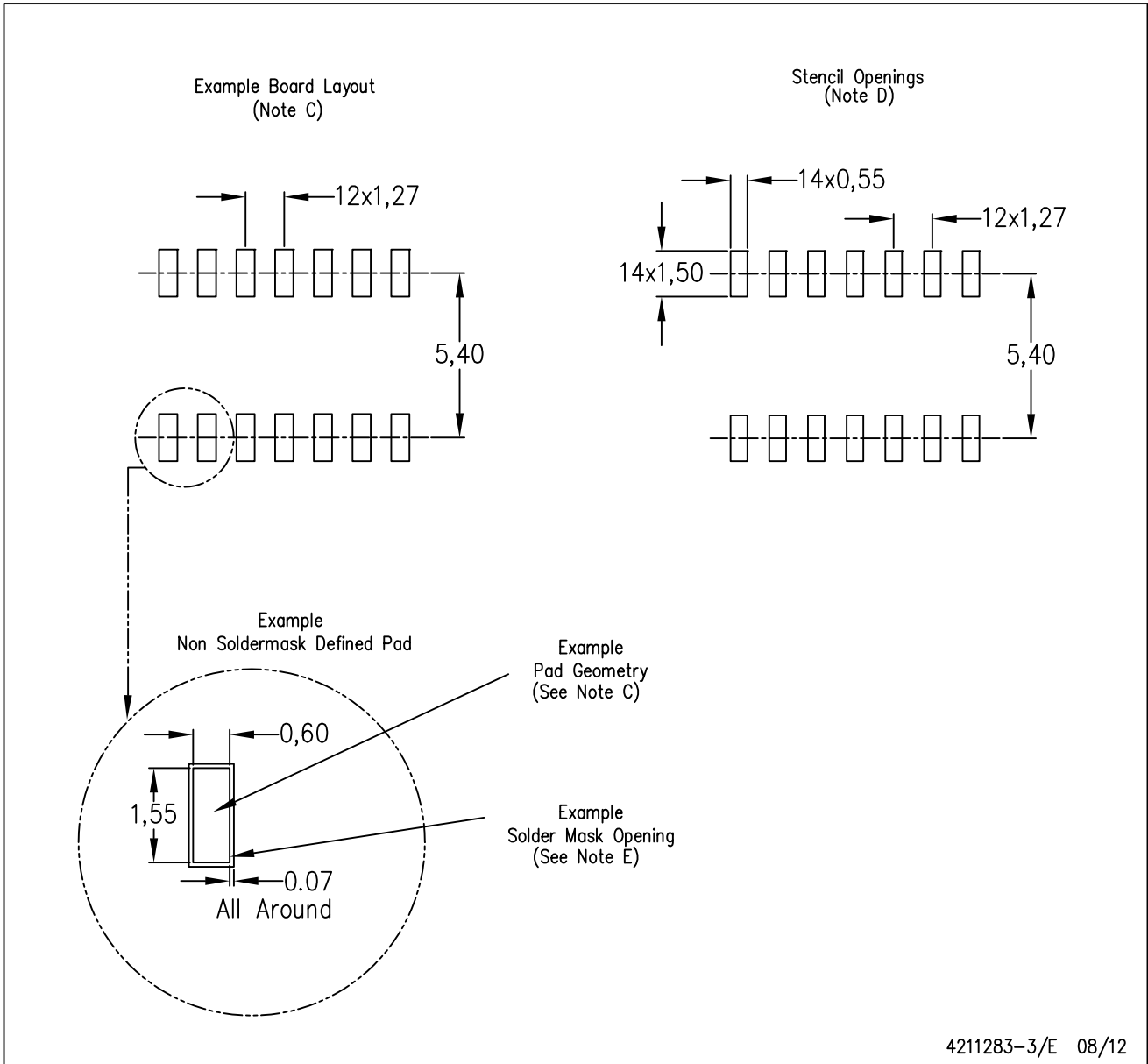
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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