MP6973

CCM/DCM Flyback Ideal Diode with Integrated 100V/14mΩ MOSFET with Slew Rate Detection

DESCRIPTION

The MP6973 is a fast turn-off, intelligent rectifier for flyback converters that integrates a 100V/14mΩ MOSFET. It can replace a diode rectifier for higher efficiency and power density. The chip regulates the forward voltage drop of the internal power switch to V_{FWD} (40mV) and turns off before the drain-source voltage reverses.

The MP6973 is optimized for low-side rectification. The internal ringing detection circuitry prevents the MP6973 from falsely turning on during discontinuous conduction mode (DCM) or quasi-resonant operations.

The MP6973 is available in an SOIC-8 package.

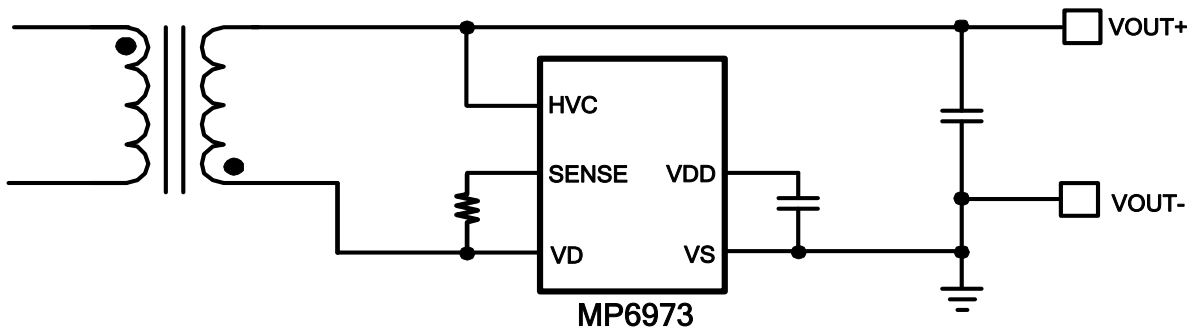
FEATURES

- Integrated 100V/14mΩ MOSFET
- Optimized Efficiency for Low-Side Rectification
- Ringing Detection Prevents False Turn-On during DCM Operations
- Compatible with Energy Star
- 110μA Quiescent Current
- Supports DCM, CCM, and Quasi-Resonant Operations
- Wide Output Range Down to 0V
- Available in an SOIC-8 Package

APPLICATIONS

- Laptop Adapters
- QC and USB PD Chargers
- High-Efficiency Flyback Converters

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6973GS*	SOIC-8	*See Below*	2

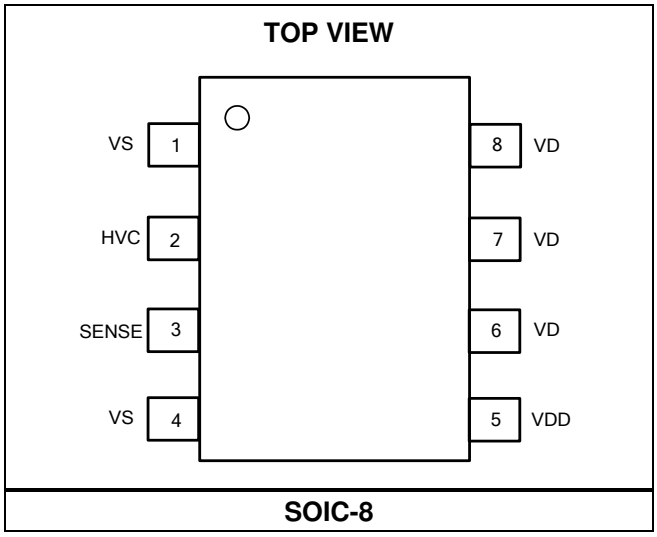
* For Tape & Reel, add suffix –Z (e.g. MP6973GS–Z).

TOP MARKING

MP6973
LLLLLLLL
MPSYWW

MP6973: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



SOIC-8

PIN FUNCTIONS

Pin #	Name	Description
1, 4	VS	**MOSFET source.** VS is also used as a reference for VDD.
2	HVC	**HV linear regulator input.**
3	SENSE	**MOSFET drain voltage sensing.**
5	VDD	**Linear regulator output.** VDD is the power supply of IC.
6, 7, 8	VD	**MOSFET drain.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD to VS .....-0.3V to +14V
VD to VS .....-1.5V to +100V
SENSE, HVC to VS .....-1V to +180V
Continuous drain current (T_C = 25°C) 14.1A
Continuous drain current (T_C = 100°C) 8.9A
Pulsed drain current (2) 50A
Maximum power dissipation (3)..... 1.8W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature ..... -55°C to +150°C

ESD Rating

Charged device model (CDM) ..... ±2000V

Recommended Operation Conditions (4)

VDD to VS .....4.5V to 13V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

SOIC-8	67	30 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Repetitive rating: Pulse width = 100µs, duty cycle limited by maximum junction temperature.
3) T_A = 25°C. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = V_{DD_HVC}, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VDD regulation voltage	V_{DD_SEN}	SENSE = 30V, HVC = 0V	4.6	5	5.4	V
	V_{DD_HVC}	SENSE = 0V, HVC = 12V	6.3	6.7	7	V
VDD UVLO rising			4.0	4.2	4.4	V
VDD UVLO hysteresis			0.1	0.24	0.38	V
VDD charging current	I_{VDD_SEN}	VDD = V_{DD_SEN} - 0.1V, SENSE = 30V, HVC = 0V, C_{DD} = 1µF	20	38	55	mA
	I_{VDD_HVC}	VDD = V_{DD_HVC} - 0.1V, SENSE = 0V, HVC = 12V, C_{DD} = 1µF	20	38	62	mA
		VDD = V_{DD_HVC} - 0.1V, SENSE = 0V, HVC = 30V, C_{DD} = 1µF	35	64	95	mA
Operating current	I_{CC}	f_{SW} = 100kHz	1.6	2.4	4	mA
Quiescent current	$I_{Q(VDD)}$	V_{DD} = 7V		110	135	µA
Control Circuitry Section						
Forward regulation voltage (VS-VD) (6)	V_{FWD}		25	40	55	mV
Turn-on threshold (VDS)			-115	-80	-57	mV
Turn-off threshold (VS-VD) (6)			-6	3	+12	mV
Turn-on delay (7)	t_{D_ON}			20		ns
Turn-off delay (6)	t_{D_OFF}			25		ns
Turn-on blanking time	t_{B-ON}		0.8	1.2	1.55	µs
Turn-off blanking threshold (VDS)	V_{B-OFF}		2	2.5	3	V
Turn-off threshold during minimum on time (VDS)			1.2	1.8	2.5	V
Turn-on slew rate detection time (7)				30		ns
Power Switch Section (8)						
Drain source breakdown voltage (6)	$V_{(BR)DSS}$		100			V
Single-pulse avalanche energy (6)	E_{AS}	V_{PS} = 50V, V_{GS} = 0V, L = 1.0mH		100		mJ
Drain-source on resistance	$R_{DS(ON)}$	I_D = 2A, V_{GS} = 6.7V		14	17.5	mΩ
Input capacitance (7)	C_{ISS}	V_{DS} = 40V, V_{GS} = 0V, f = 1MHz		1925		pF
Output capacitance (7)	C_{OSS}			307		pF
Reverse transfer capacitance (7)	C_{RSS}			20		pF

ELECTRICAL CHARACTERISTICS *(continued)*

VDD = V_{DD_HVC}, T_J = -40°C to +125°C, unless otherwise noted.

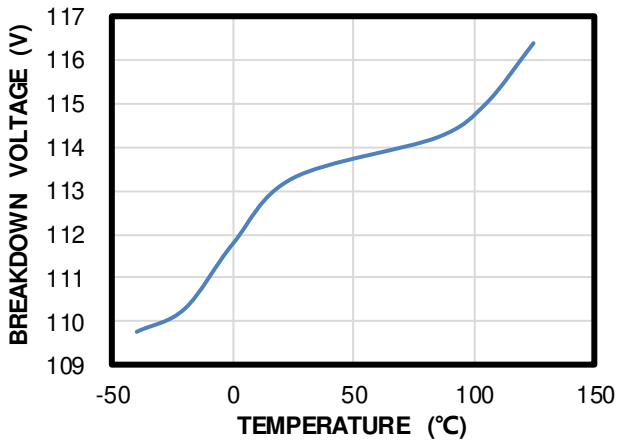
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Source-Drain Diode Characteristics						
Source-drain diode forward voltage	V_{SD}	I_S = 8A, V_{GS} = 0V		0.8	1.2	V
Reverse recovery time (7)	t_{RR}	I_F = 10A, dI/dt = 100A/μs		78		ns
Diode reverse change (7)	Q_{RR}			105		nC

Notes:

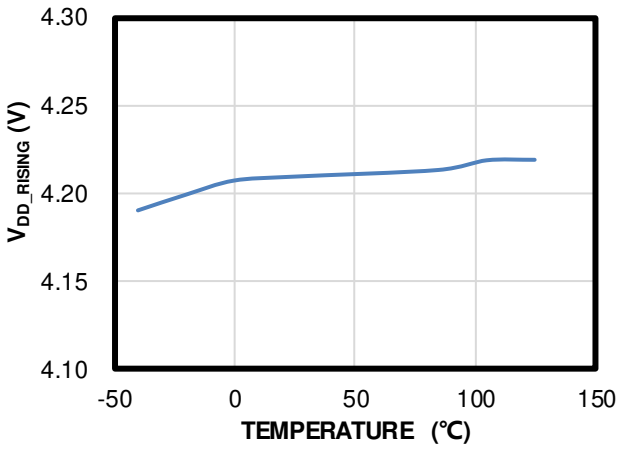
6) Guaranteed by characterization.
7) Guaranteed by design.
8) T_J = 25°C.

TYPICAL CHARACTERISTICS

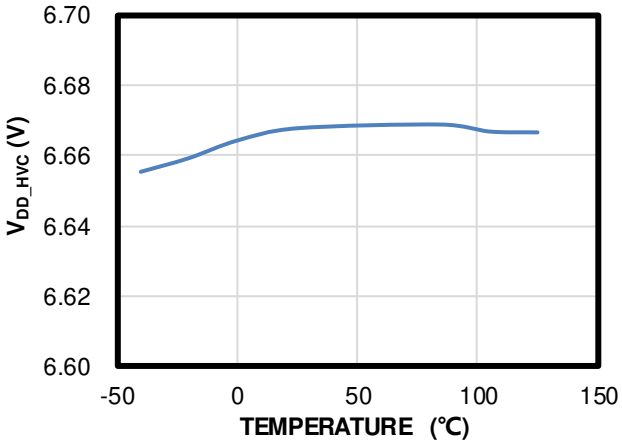
VD-VS Breakdown Voltage vs. Temperature



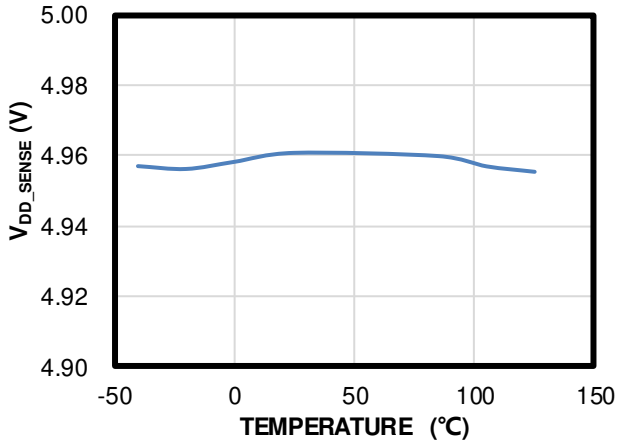
VDD Rising vs. Temperature



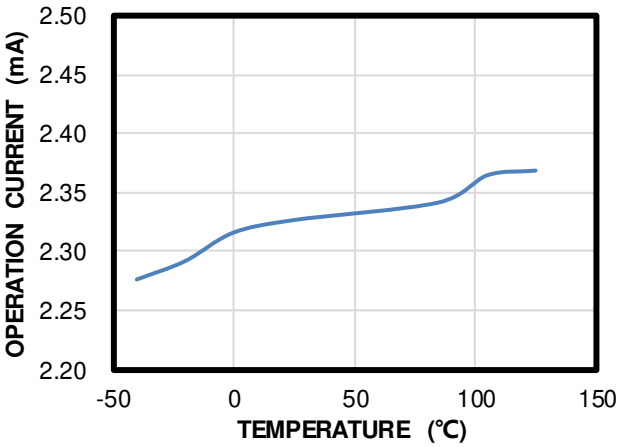
VDD Regulation Voltage vs. Temperature (HVC = 12V)



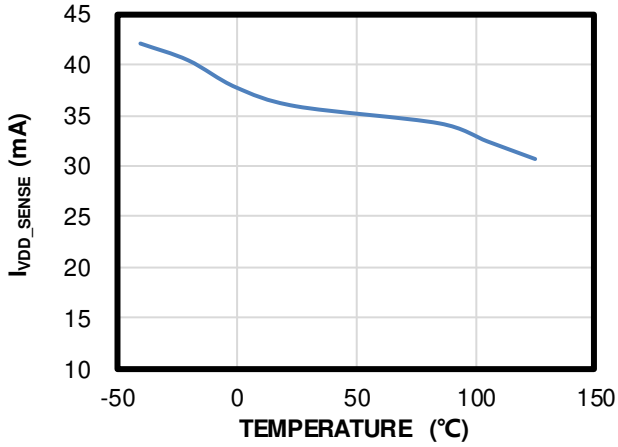
VDD Regulation Voltage vs. Temperature (SENSE = 30V)



Operation Current vs. Temperature (V_{DD} = 6.7V)

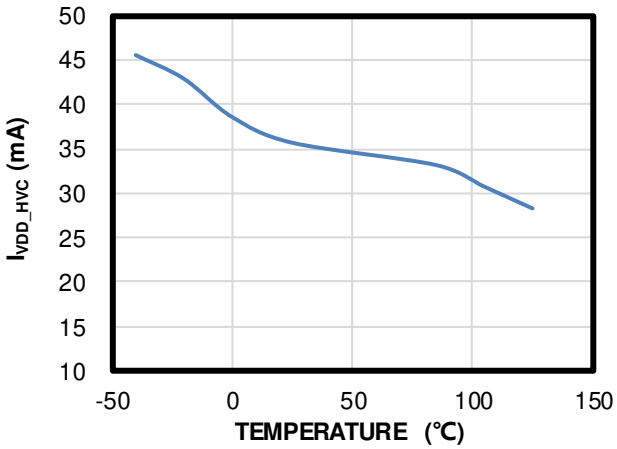


VDD Charging Current vs. Temperature (SENSE = 30V)

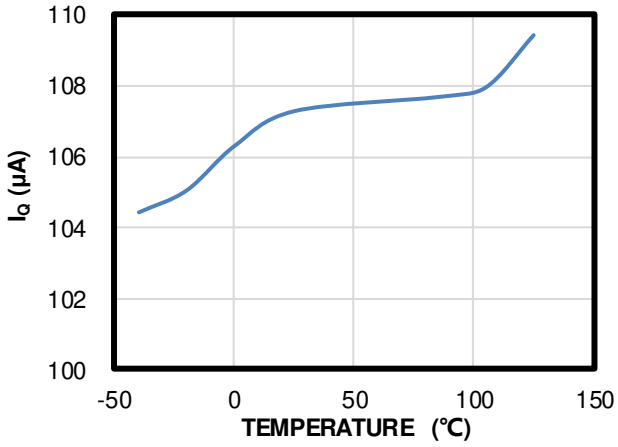


TYPICAL CHARACTERISTICS *(continued)*

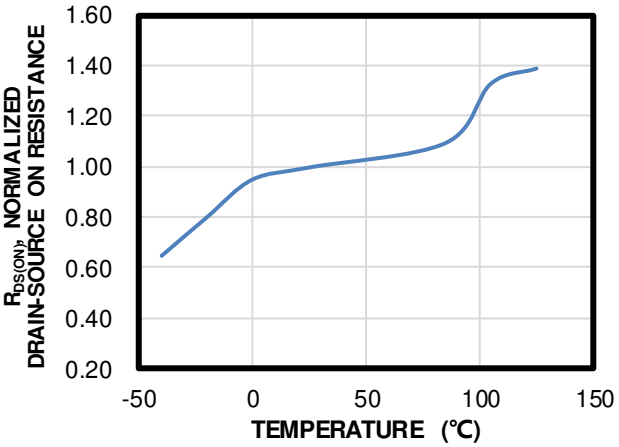
VDD Charging Current vs. Temperature (HVC = 12V)



Quiescent Current vs. Temperature (VDD = 7V)



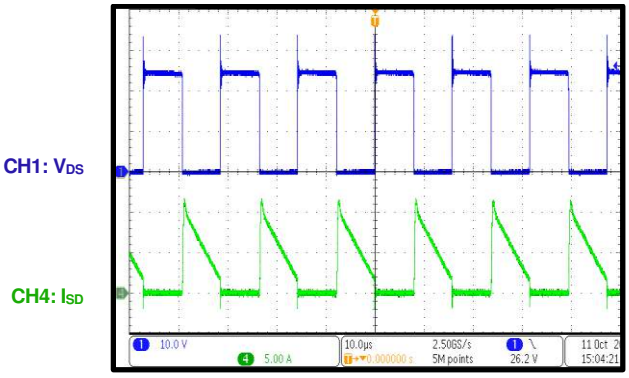
$R_{DS(ON)}$ vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

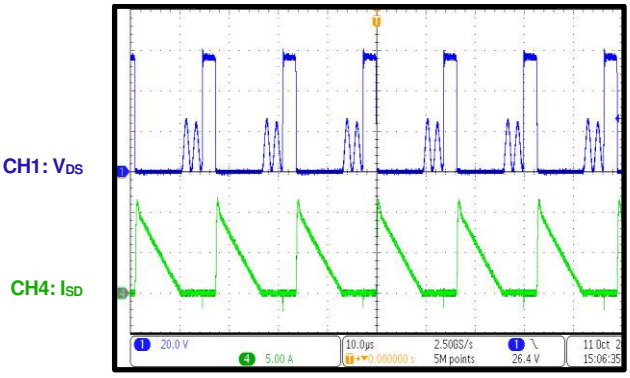
Operation in 36W Flyback Application

V_{IN} = 90V_{AC}, I_{OUT} = 3.0A



Operation in 36W Flyback Application

V_{IN} = 265V_{AC}, I_{OUT} = 3.0A



FUNCTIONAL BLOCK DIAGRAM

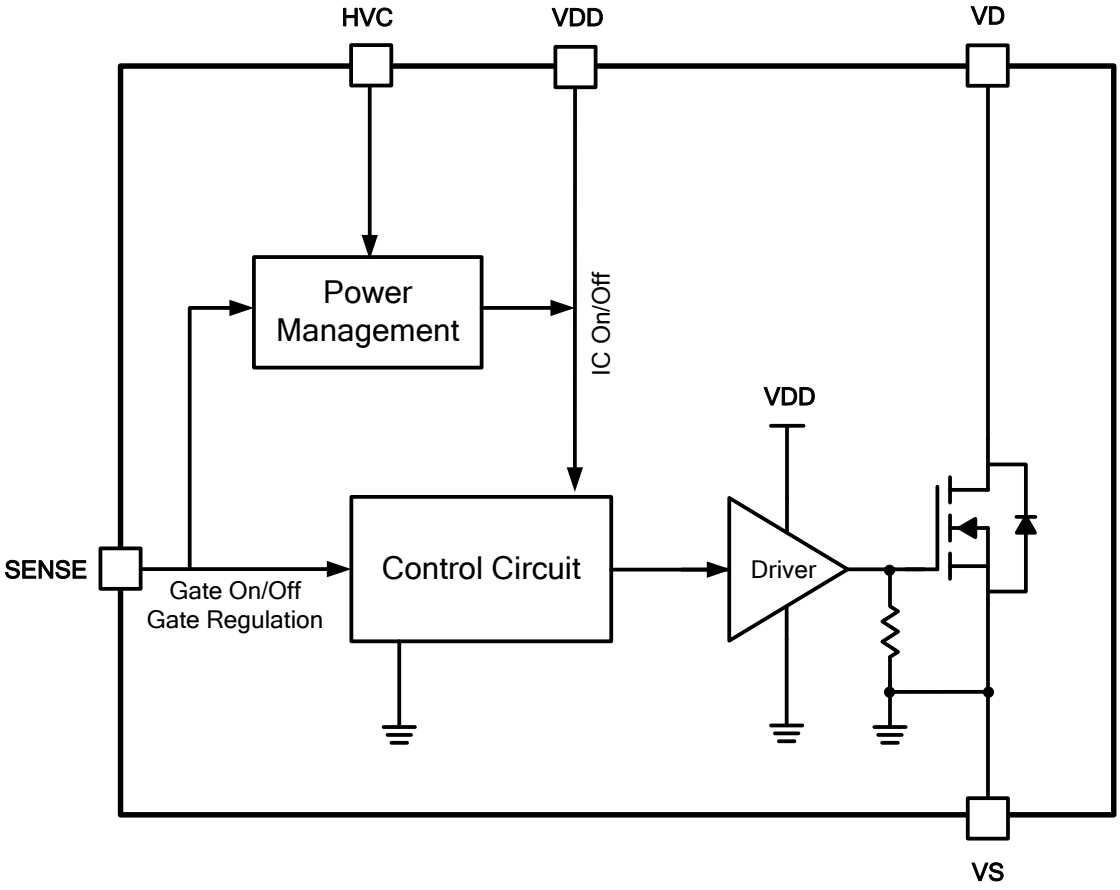


Figure 1: Functional Block Diagram

OPERATION

The MP6973 supports operation in discontinuous conduction mode (DCM) and continuous conduction mode (CCM), as well as quasi-resonant (QR) flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the synchronous rectification (SR) MOSFET current drops to zero.

VDD Generation

The external capacitor at VDD supplies power for the IC. First, SENSE charges the capacitor via a current source with I_{VDD_SEN}. When UVLO < V_{DD} < V_{DD_SENSE} (5V), both HVC and SENSE are allowed to charge VDD. But when V_{DD} exceeds V_{DD_SENSE}, HVC charges VDD alone via a current source with I_{VDD_HVC}.

If V_{HVC} < 5.7V, then VDD is regulated at V_{DD_SENSE} (5V). When 5.7V < V_{HVC} < 6.7V, VDD is regulated at V_{HVC} - 0.7V (internal current-dependent forward-diode voltage drop). When V_{HVC} > 6.7V, VDD is clamped at V_{DD_HVC} (6.7V).

Start-Up and Under-Voltage Lockout (UVLO)

When V_{DD} exceeds the VDD UVLO rising threshold (4.2V), the MP6973 exits under-voltage lockout (UVLO) and is enabled. Once V_{DD} drops below ~4.0V, the MP6973 enters sleep mode and V_{GS} is kept low.

Turn-On Phase

When V_{DS} drops to ~2V, a turn-on timer begins. If V_{DS} reaches the turn-on threshold (-80mV) from 2V within the turn-on slew rate detection time (30ns), the MOSFET turns on after a turn-on delay (t_{D_ON}), typically 20ns (see Figure 2). If V_{DS} crosses the turn-on threshold after the timer ends, the gate voltage remains off. This turn-on timer prevents the MP6973 from falsely turning on due to the ringing in DCM and quasi-resonant operations.

Turn-On Blanking

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on state lasts for a specific period of time. The turn-on blanking time ($t_{B\text{-}ON}$) is ~1.2µs to prevent an accidental turn-off due to ringing. However, if V_{DS} reaches 1.8V within the turn-on blanking time, V_{GS} is pulled low immediately.

Conduction Phase

Once V_{DS} exceeds the forward voltage drop, which is -V_{FWD} (-40mV), according to the decrease of the switching current, the MP6973 lowers the gate voltage level to enlarge the on resistance of the synchronous MOSFET.

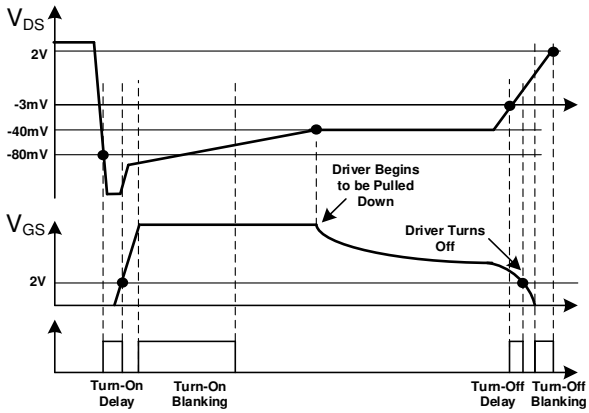


Figure 2: Turn-On/Turn-Off Timing Diagram

With this control scheme, V_{DS} is adjusted to be approximately equal to V_{FWD}, even when the current through the MOSFET is fairly low. This function keeps the driver voltage at a very low level when the synchronous MOSFET is turned off, which boosts the turn-off speed and is especially important for CCM operation.

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold (-3mV), the gate voltage is pulled to zero after a short turn-off delay (t_{D_OFF}), typically 25ns (see Figure 2).

Turn-Off Blanking

After the gate driver (V_{GS}) is pulled to zero by V_{DS} reaching the turn-off threshold (-3mV), a turn-off blanking time is applied, during which the gate driver signal is latched off. The turn-off blanking is removed when V_{DS} exceeds $V_{B\text{-}OFF}$ (2V) (see Figure 2).

APPLICATION INFORMATION

Slew Rate Detection

During DCM operation, the demagnetizing ringing may bring V_{DS} below 0V. If V_{DS} reaches the turn-on threshold during the ringing period, SR controllers without slew rate detection may turn on the MOSFET by mistake. This not only increases power loss, but may also lead to shoot-through if the primary-side MOSFET is turned on within the minimum on time of the SR controller.

The falling slew rate of the ringing is always much less than when the primary MOSFET is turned off; this false turn-on situation can be prevented by the slew rate detection function. When the slew rate is less than the threshold, the IC does not turn on the gate even when V_{DS} reaches the turn-on threshold. For more details, see the Turn-On Phase section on page 10.

External Resistor on SENSE and HVC

Over-voltage conditions may lead to the device malfunctioning or even being damaged, so the application design must be careful to guarantee safe operation, especially on the high-voltage pin.

One common over-voltage condition occurs when the body diode of the SR MOSFET is turned on, as the forward voltage drop may exceed the negative rating on the SENSE pin. In this case, it is recommended to place an external resistor between SENSE and the MOSFET drain. The resistance is typically recommended to be between 100Ω and 300Ω.

On the other hand, this resistor also cannot be too large, because it may slow down the slew rate on V_{DS} detection. In general, it is not recommended to use a resistor greater than 300Ω, but this should be checked for each case based on the condition of the slew rate.

In the applications where HVC may also suffer from negative voltage bias (e.g. in the high side setup without auxiliary winding), there should be also the same resistance be placed on HVC externally.

Typical System Implementations

Figure 3 shows the typical system IC implementation in low-side rectification. The MP6973 is directly supplied by the output.

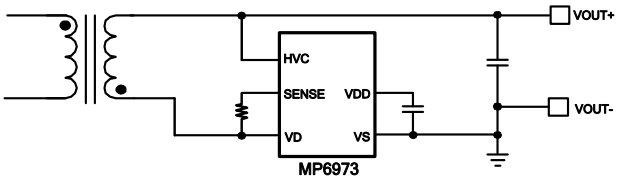


Figure 3: Low-Side Rectification

Maximum Output Current

The allowed temperature rise of the MP6973 limits the maximum output current the device can handle. The temperature rise is determined by its own power loss. Generally, the MP6973's recommended rated output current for a universal input adapter is 3A. For certain designs, the power loss of the MP6973 can be calculated, so the maximum output current can be deduced.

The MP6973's power loss can be separated into several parts, including controller consumption and integrated MOSFET conduction loss. If the MP6973 works in continuous conduction mode (CCM), reverse-recovery loss of the integrated MOSFET must also be considered. Each part of the loss can be calculated based on Equation (1), Equation (2), and Equation (3), respectively:

$$P_{LOSS\_CONTROLLER} = V_{HVC} \times I_{DD} \quad (1)$$

$$P_{LOSS\_SR\_CONDUCTION} = f_{SW} \times \int_{0}^{t_{S\_ON}} V_{SR\_SD}(t) \times I_{SR\_SD}(t)dt \quad (2)$$

$$P_{LOSS\_SR\_RR} = \frac{1}{2} \times V_{DS} \times I_{RR} \times t_{RR} \times f_{SW} \quad (3)$$

Where I_{DD} is the current of the MP6973, V_{HVC} is the voltage on HVC pin, t_{S_ON} is the SR on period, V_{SR_SD} is the voltage drop from the SR, I_{SR_SD} is the current flowing through the SR, I_{RR} is the peak reverse current, and t_{RR} is the reverse-recovery time.

The total loss of the MP6973 (P_{LOSS}) is the sum of the above losses. If an RC snubber is used, the power loss caused by this snubber must also be taken into consideration.

The junction and case temperature rises can be calculated with the junction-to-ambient thermal resistance (θ_{JA}) and junction-to-case thermal resistance (θ_{JC}). The junction temperature must be within ABS (typically 150°C). Calculate ΔT_{JA} and ΔT_{JC} with Equation (4) and Equation (5):

$$\Delta T_{JA} = P_{LOSS} \times \theta_{JA} \quad (4)$$

$$\Delta T_{JC} = P_{LOSS} \times \theta_{JC} \quad (5)$$

The thermal resistance can be reduced by laying a thicker copper layer, placing more thermal dissipation vias, and adopting a heatsink. The real maximum output current can be set by combining the real tested data.

Design Example

Figure 4 shows a layout example for a low-side application of a flyback power supply, specifically a single layer with a through-hole transformer. RSN and CSN are the RC snubber network for the internal MOSFET. The sensing loop (SENSE to the MOSFET drain) is optimized and kept separate from the power loop. The VDD decoupling capacitor (C2) is placed beside VDD.

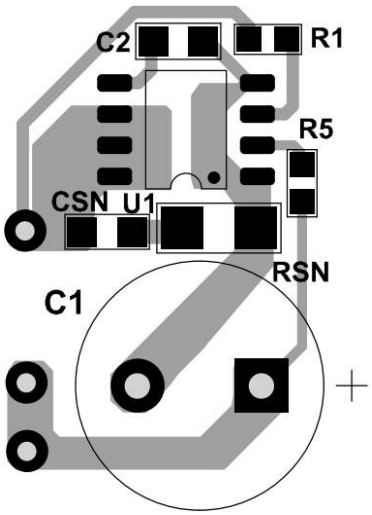


Figure 4: Layout Example in Flyback Low-Side Application

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and Figure 5, and follow the guidelines below:

Sensing for VD/SENSE

1. Connect the SENSE pin to a different position for an adjustable turn-off time during the fast transients in CCM. The further the junction point is from the VD, the earlier the SR turns off (see Figure 5).
2. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other.

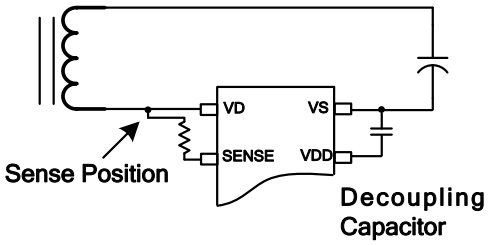
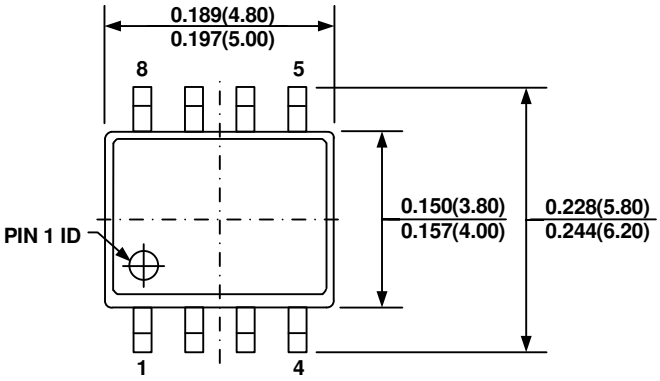


Figure 5: Voltage Sensing for VD/SENSE

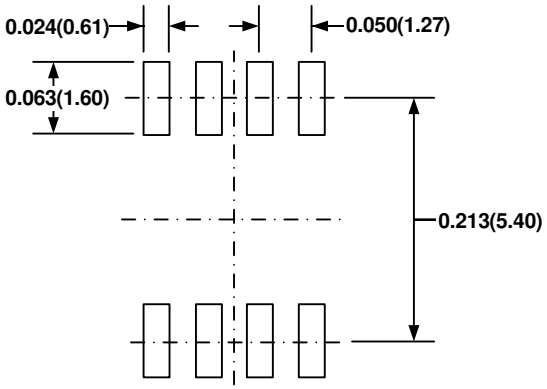
3. Place a decoupling ceramic capacitor from VDD to VS, close to the IC, for adequate filtering.

PACKAGE INFORMATION

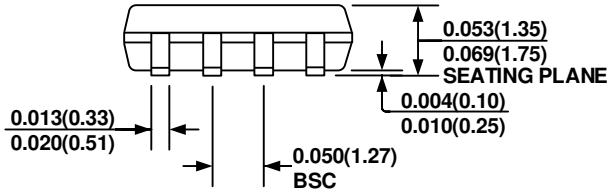
SOIC-8



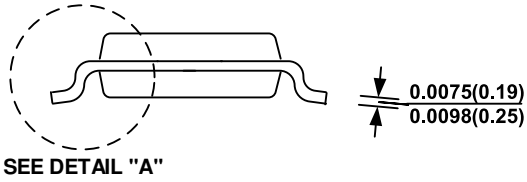
TOP VIEW



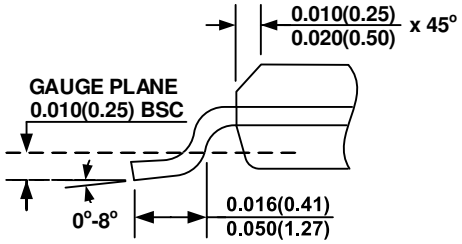
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

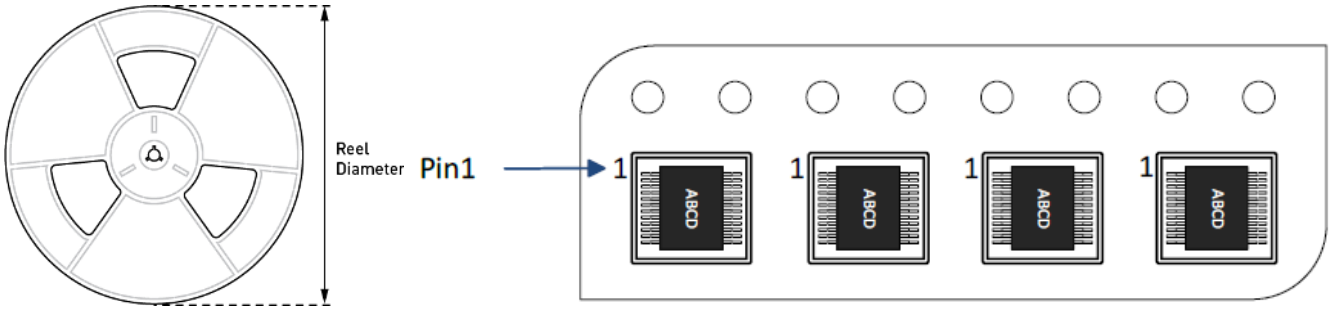


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6973GS–Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	6/17/2020	Initial Release	-