User's Guide

TPS54821 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS54821EVM-049 evaluation module (PWR049) as well as for the TPS54821 dc/dc converter. Also included are the performance specifications, the schematic, and the bill of materials for the TPS54821EVM-049.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

1.1 Background

The TPS54821 DC/DC converter is designed to provide up to a 8-A output. The TPS54821 implements split-input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 17 V whereas the control input (VIN) is rated for 4.5 V to 17 V. The TPS54821EVM-049 provides both inputs but is designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS54821 regulator. The switching frequency is externally set at a nominal 480 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54821 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54821 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54821 provides adjustable slow start, tracking, and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the TPS54821EVM-049.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54821EVM-049	VIN = 8 V to 17 V (VIN start voltage = 6.528 V)	0 A to 8 A

1.2 Performance Specification Summary

A summary of the TPS54821EVM-049 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54821EVM-049 is designed and tested for V_{IN} = 8 V to 17 V with the VIN and PVIN pins connect together with the JP1 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54821EVM-049 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range (PVIN = VIN)			8	12	17	V
V_{IN} start voltage				6.528		V
V_{IN} stop voltage				6.193		V
Output voltage setpoint				3.3		V
Output current range	V_{IN} = 8 V to 17 V		0		8	A
Line regulation	I_O = 4 A, V_{IN} = 8 V to 17 V			±0.005		%
Load regulation	V_{IN} = 12 V, I_O = 0 A to 8 A			±0.07		%
Load transient response	I_O = 2 A to 6 A	Voltage change		–130		mV
		Recovery time		80		µs
	I_O = 6 A to 2 A	Voltage change		130		mV
		Recovery time		80		µs
Loop bandwidth	V_{IN} = 12 V, I_O = 8 A			60		kHz
Phase margin	V_{IN} = 12 V , I_O = 8 A			74		°
Input ripple voltage	I_O = 8 A			900		mVPP
Output ripple voltage	I_O = 8 A			10		mVPP
Output rise time				6		ms
Operating frequency				480		kHz
Maximum efficiency	TPS54821EVM-049, V_{IN} = 8 V, I_O = 1.5 A			95.9		%

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54821. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R7 and R8. R7 is fixed at 10 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R8. Changing the value of R8 can change the output voltage above 0.6 V. The value of R8 for a specific output voltage can be calculated using Equation 1.

$$R8 = \frac{10\ k\Omega \times 0.6\ \mathrm{V}}{\mathrm{V_{OUT}} - 0.6\mathrm{V}} \tag{1}$$

Table 1-3 lists the R8 values for some common output voltages. Note that V_{IN} must be in a range so that the on-time is greater than the minimum controllable on-time (94-ns typical, 145-ns maximum), and the maximum duty cycle is less than 95%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Output Voltages Available

OUTPUT VOLTAGE (V)	R8 VALUE (kΩ)
1.8	4.99
2.5	3.16
3.3	2.21
5	1.37

1.3.2 Slow-Start Time

The slow-start time can be adjusted by changing the value of C8. Use Equation 2 to calculate the required value of C8 for a desired slow-start time.

$$\mathrm{C8(nF)} = \frac{\mathrm{Tss(ms)} \times \mathrm{Iss(\mu A)}}{\mathrm{Vref(V)}} \tag{2}$$

The EVM is set for a slow-start time of 5.7 ms using C8 = 0.022 µF.

1.3.3 Track In

The TPS54821 can track an external voltage during start-up. The J3 connector is provided to allow connection to that external voltage. Ratiometric or simultaneous tracking can be implemented using resistor divider R5 and R6. See the *TPS54821 4.5 V to 17 V Input, 8 A Synchronous Step Down Converter Data Sheet* for details.

1.3.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 6.528 V and a stop voltage of 6.193 V using R1 = 35.7 kΩ and R2 = 8.06 kΩ. Use Equation 3 and Equation 4 to calculate required resistor values for different start and stop voltages.

$$\mathrm{R1} = \frac{\mathrm{V_{START}}\left(\frac{\mathrm{V_{ENFALLING}}}{\mathrm{V_{ENRISING}}}\right) - \mathrm{V_{STOP}}}{\mathrm{I_p}\left(1 - \frac{\mathrm{V_{ENFALLING}}}{\mathrm{V_{ENRISING}}}\right) + \mathrm{I_h}} \tag{3}$$

$$\mathrm{R2} = \frac{\mathrm{R1} \times \mathrm{V_{ENFALLING}}}{\mathrm{V_{STOP}} - \mathrm{V_{ENFALLING}} + \mathrm{R1}(\mathrm{I_p} + \mathrm{I_h})} \tag{4}$$

1.3.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected using a jumper across JP1. The single input voltage is supplied at J1. If desired, these two input voltage rails may be separated by removing the jumper across JP1. Two input voltages must then be provided at both J1 and J2.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54821EVM-049 evaluation module. The section also includes test results typical for the evaluation module and covers the following:

- Efficiency
- Output voltage regulation
- Load transients
- Loop response
- Output ripple
- Input ripple
- Start-up

2.1 Input/Output Connections

The TPS54821EVM-049 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The jumper across JP1 must be in place. See Section 1.3.5 for split-input voltage rail operation. The load must be connected to J4 through a pair of 20 AWG wires. The maximum load current capability must be 8 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP10 as the ground reference.

Table 2-1. EVM Connectors and Test Points

REFERENCE DESIGNATOR	Function
J1	PVIN input voltage connector. (See Table 1-1 for V_{IN} range.)
J2	VIN input voltage connector. Not normally used.
J3	2-pin header for tracking voltage input and ground
J4	V_{OUT}, 3.3 V at 8-A maximum
J5	2-pin header for tracking output and ground
JP1	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
JP2	2-pin header for enable. Connect EN to ground to disable, open to enable.
TP1	PVIN test point at PVIN connector
TP2	GND test point at PVIN connector
TP3	VIN test point at VIN connector
TP4	GND test point at VIN connector
TP5	Test point provided to connect external voltage source for PWRGD pullup.
TP6	PWRGD test point
TP7	PH test point
TP8	Test point between voltage divider network and output. Used for loop response measurements.
TP9	Output voltage test point at VOUT connector
TP10	GND test point at VOUT connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 2 A and then decreases as the load current increases toward full load. Figure 2-1 shows the efficiency for the TPS54821EVM-049 at an ambient temperature of 25°C.

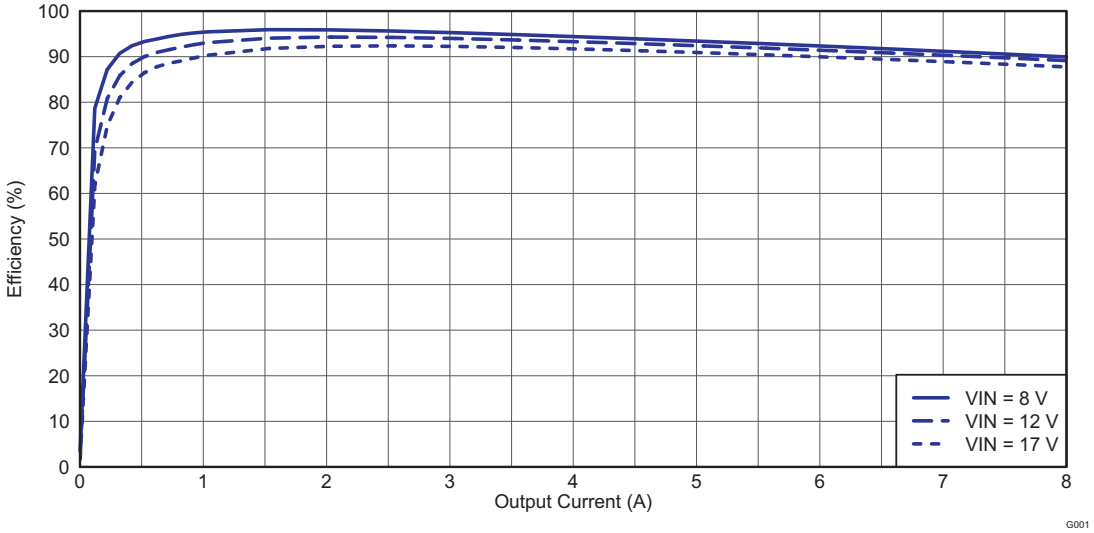

Figure 2-1. TPS54821EVM-049 Efficiency

Figure 2-2 shows the efficiency for the TPS54821EVM-049 using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

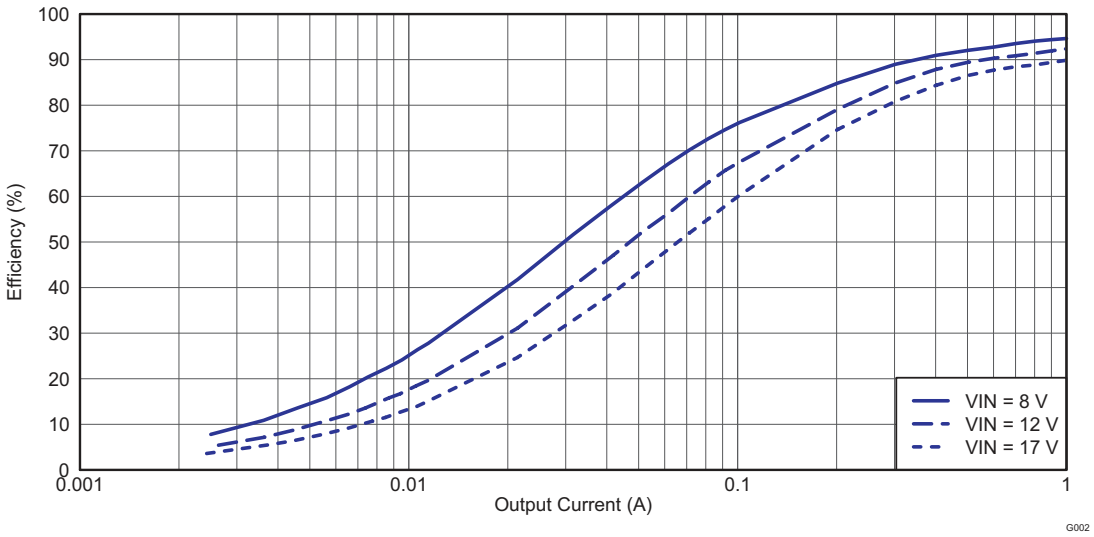

Figure 2-2. TPS54821EVM-049 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54821EVM-049.

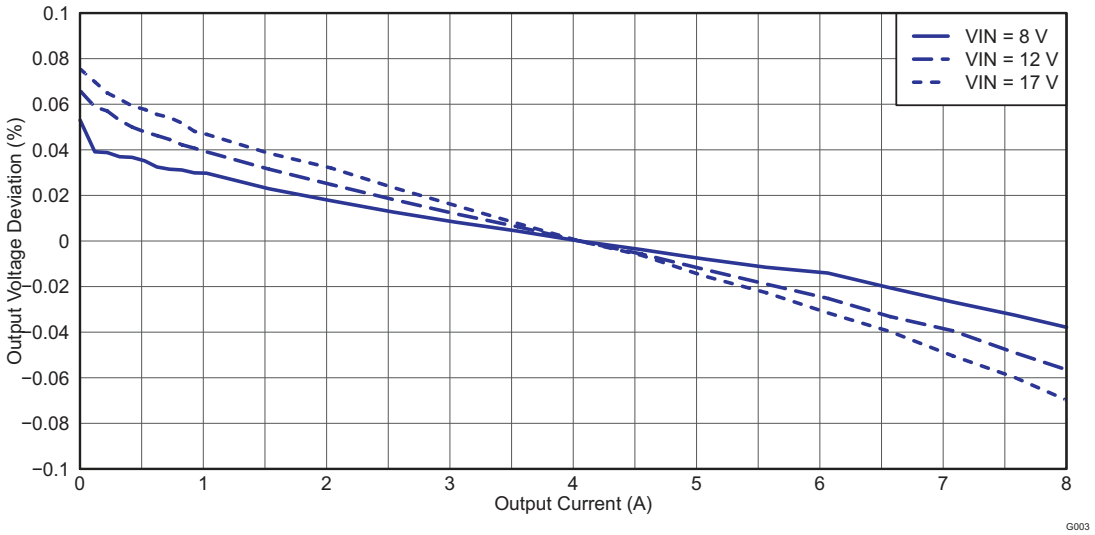

Figure 2-3. TPS54821EVM-049 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-4 shows the line regulation for the TPS54821EVM-049.

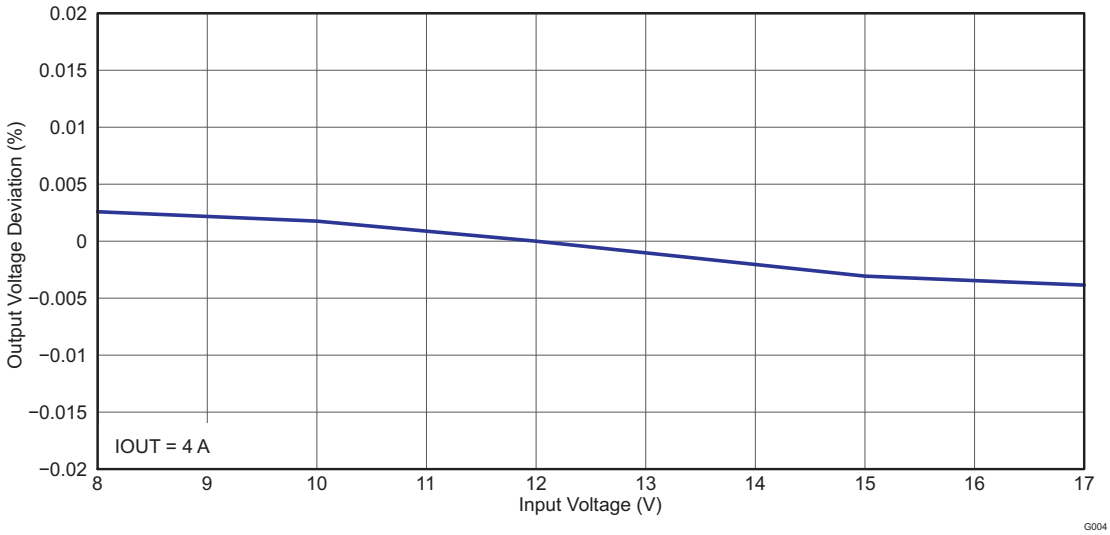

Figure 2-4. TPS54821EVM-049 Line Regulation

2.5 Load Transients

Figure 2-5 shows the TPS54821EVM-049 response to load transients. The current step is from 25% to 75% of maximum rated load at 12-V input. The current step slew rate is 1 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

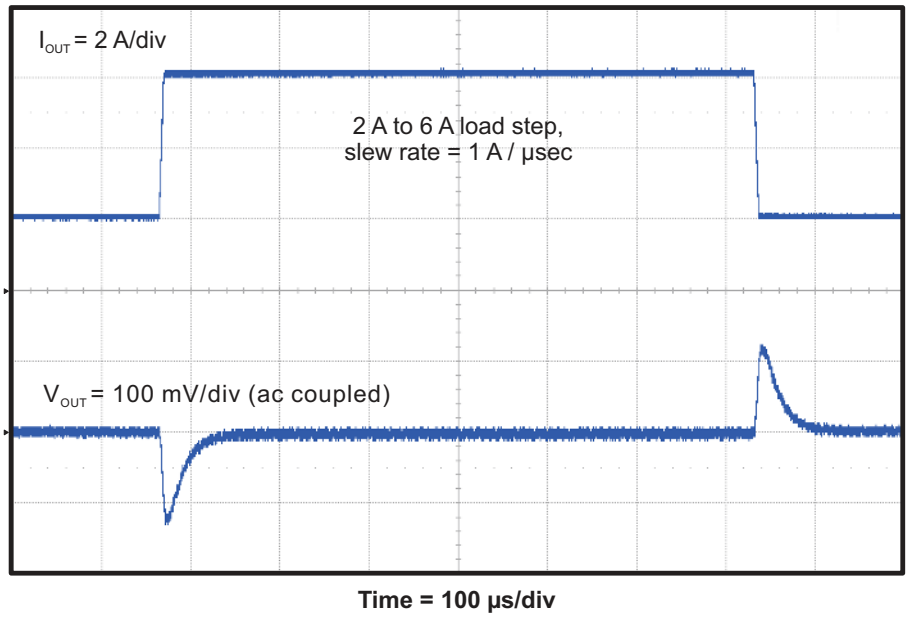

Figure 2-5. TPS54821EVM-049 Transient Response

2.6 Loop Characteristics

Figure 2-6 shows the TPS54821EVM-049 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 8 A.

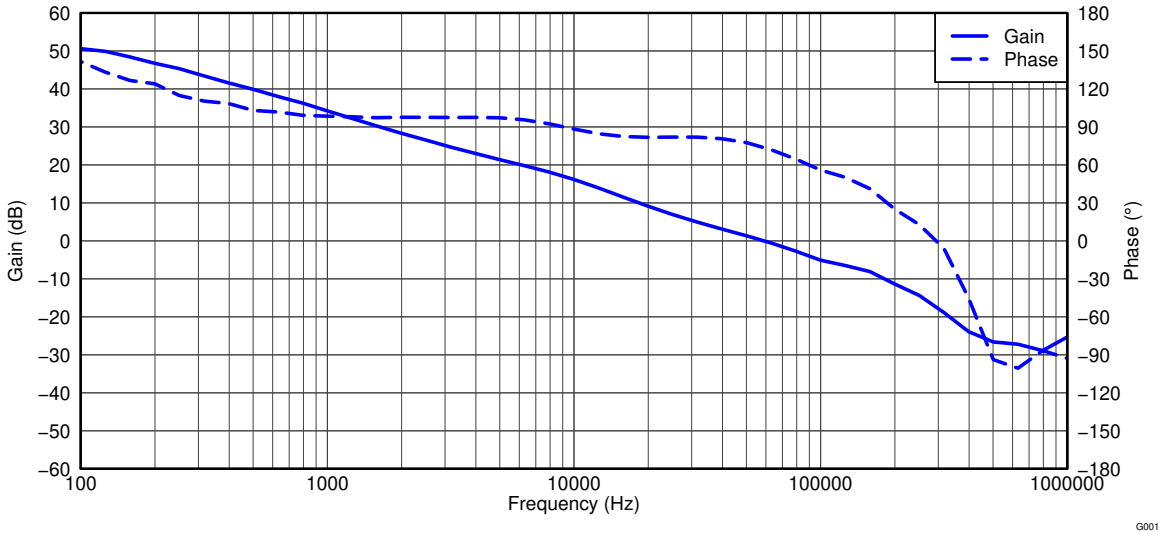

Figure 2-6. TPS54821EVM-049 Loop Response

2.7 Output Voltage Ripple

Figure 2-7 shows the TPS54821EVM-049 output voltage ripple. The output current is the rated full load of 8 A and V_{IN} = 12 V. The ripple voltage is measured directly across the output capacitors.

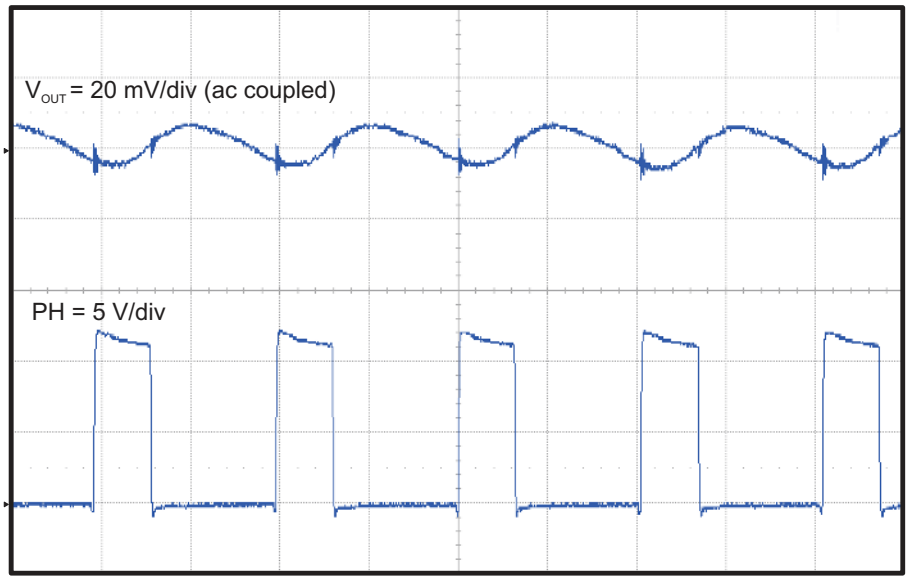

Figure 2-7. TPS54821EVM-049 Output Ripple

2.8 Input Voltage Ripple

Figure 2-8 shows the TPS54821EVM-049 input voltage. The output current is the rated full load of 8 A and V_{IN} = 12 V. The ripple voltage is measured directly across the input capacitors.

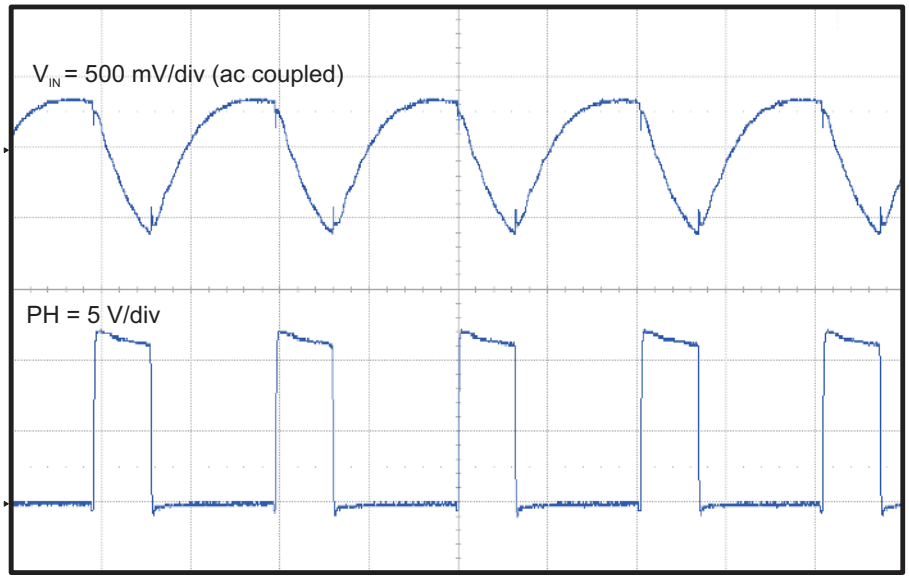

Figure 2-8. TPS54821EVM-049 Input Ripple

2.9 Powering Up

Figure 2-9 and Figure 2-10 show the start-up waveforms for the TPS54821EVM-049. In Figure 2-9, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 2-10, the input voltage is initially applied and the output is inhibited by using a jumper at JP2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 12 V and the load is 1 Ω. PWRGD is pulled up to an external 5 V supply at TP5.

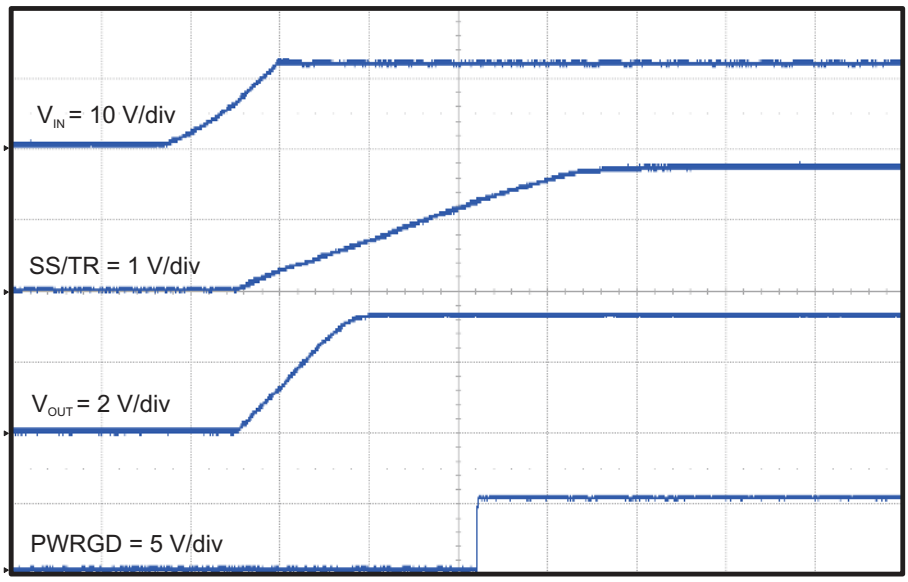

Figure 2-9. TPS54821EVM-049 Start-Up Relative to V_{IN}

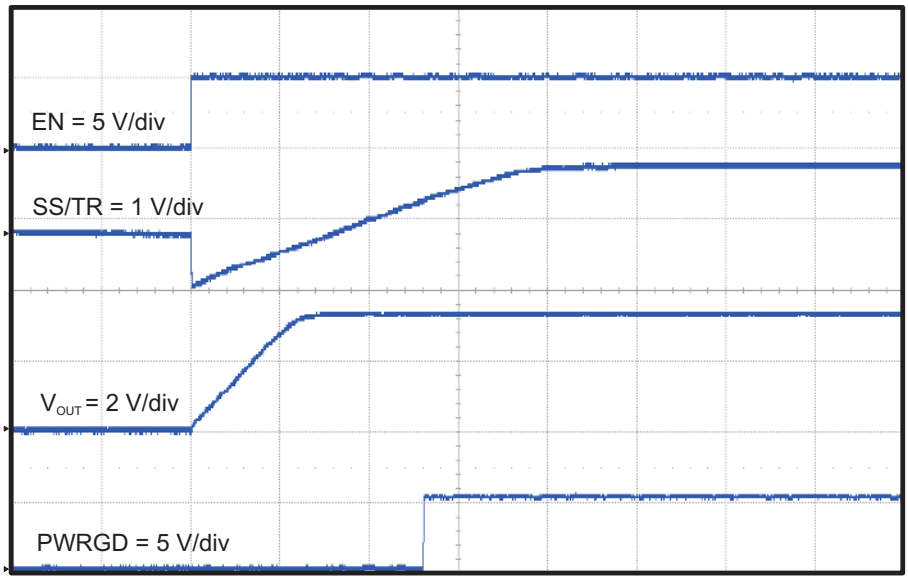

Figure 2-10. TPS54821EVM-049 Start-Up Relative to Enable

2.10 Pre-Bias Start-Up

The TPS54821 is designed to start up into a pre-biased output. The output voltage is not discharged to ground at the beginning of the slow-start sequence. Figure 2-11 shows the start-up waveform with the output voltage pre-biased to 1 V.

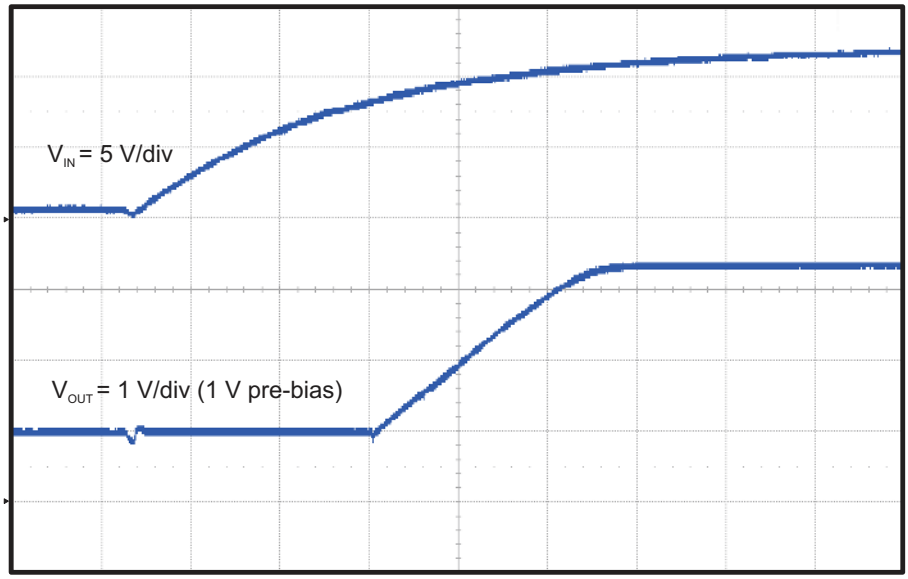

Figure 2-11. TPS54821EVM-049 Start-Up Into Pre-Bias

2.11 Hiccup-Mode Current Limit

The TPS54821 features hiccup-mode current limit. When an overcurrent event occurs, the TPS54821 shuts down and restarts. Figure 2-12 shows restart sequence in an overcurrent condition.

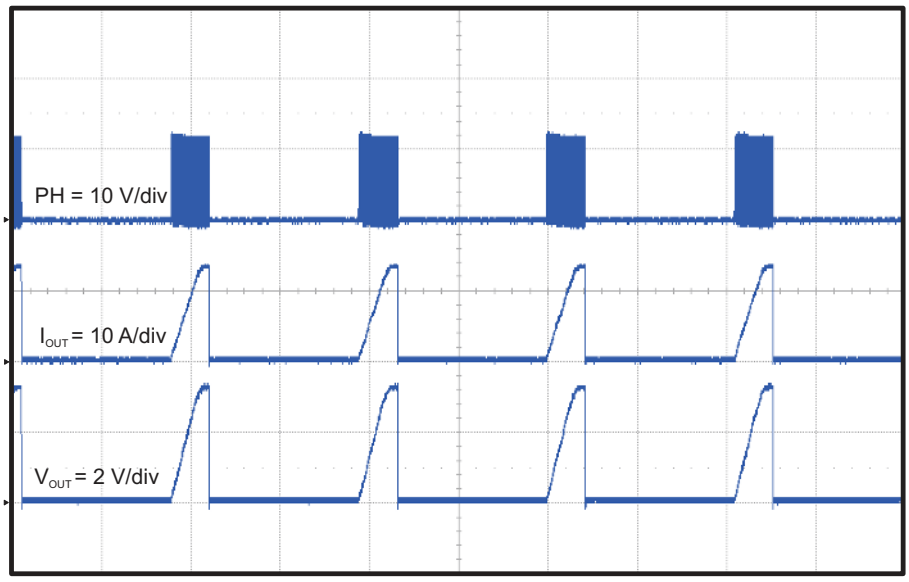

Figure 2-12. TPS54821EVM-049 Hiccup-Mode Current Limit

3 Board Layout

This section provides a description of the TPS54821EVM-049 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS54821EVM-049 is shown in Figure 3-1 through Figure 3-5. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for PVIN, VIN, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54821 and a large area filled with ground. The internal layer-2 is primarily ground with additional fill areas for PVIN, VIN, and V_{OUT}. The bottom and internal layer-2 contain ground planes only. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board including five vias directly under the TPS54821 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C2 and C4) and bootstrap capacitor (C5) are all located as close to the IC as possible. Additionally, the voltage setpoint resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the J4 output connector. For the TPS54821, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage setpoint divider, frequency set resistor, slow-start capacitor, and compensation components are terminated to ground using a wide ground trace separate from the power ground pour.

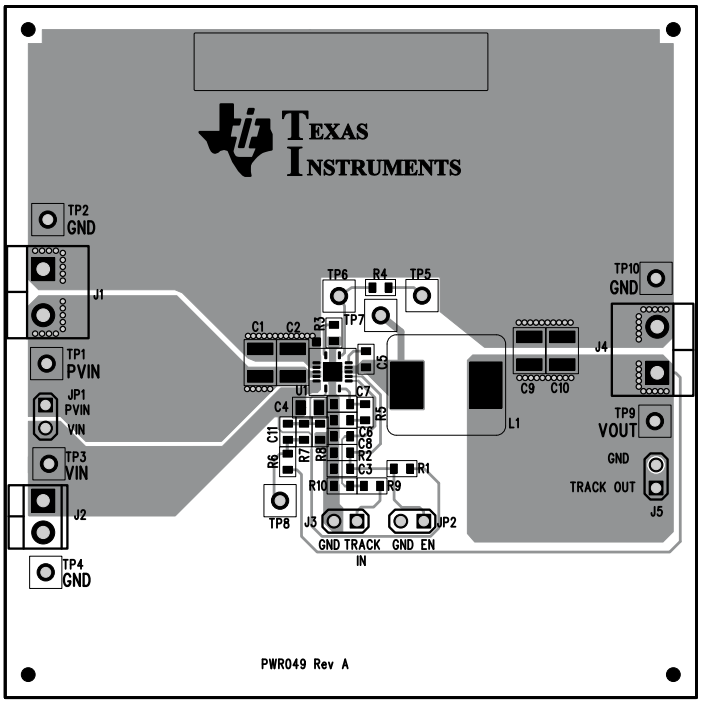

Figure 3-1. TPS54821EVM-049 Top-Side Assembly

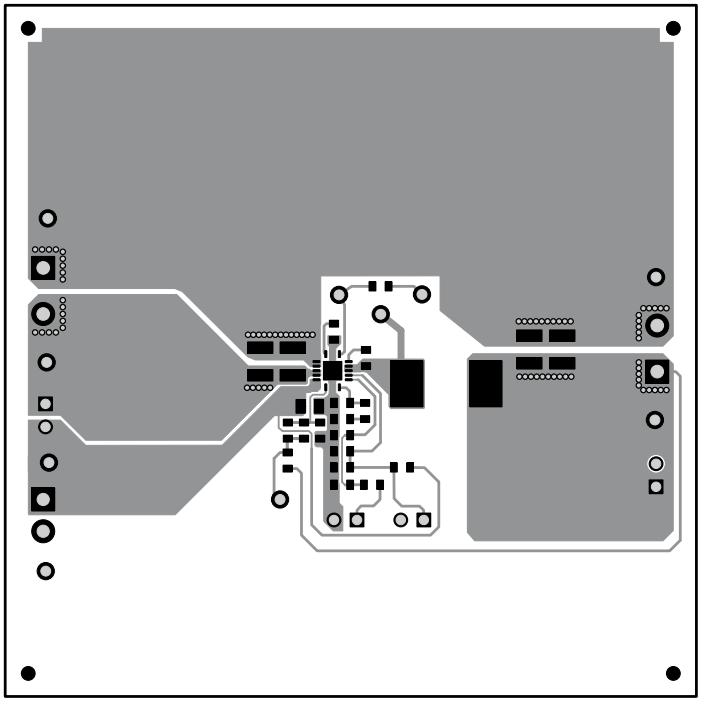

Figure 3-2. TPS54821EVM-049 Top-Side Layout

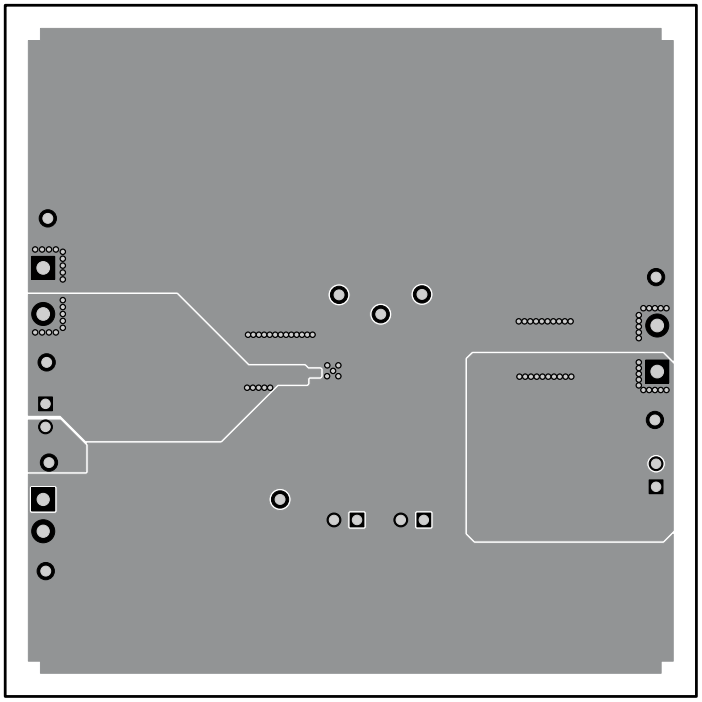

Figure 3-3. TPS54821EVM-049 Internal Layer-1 Layout

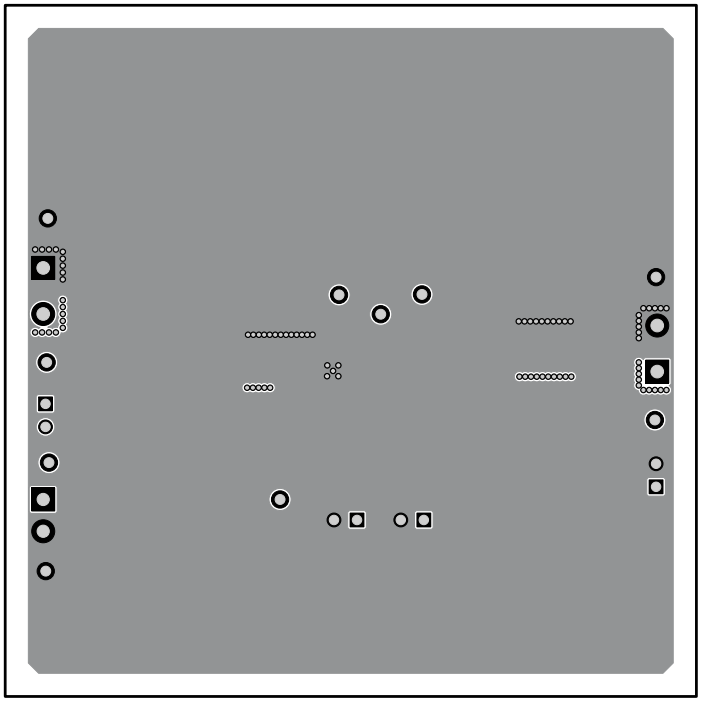

Figure 3-4. TPS54821EVM-049 Internal Layer-2 Layout

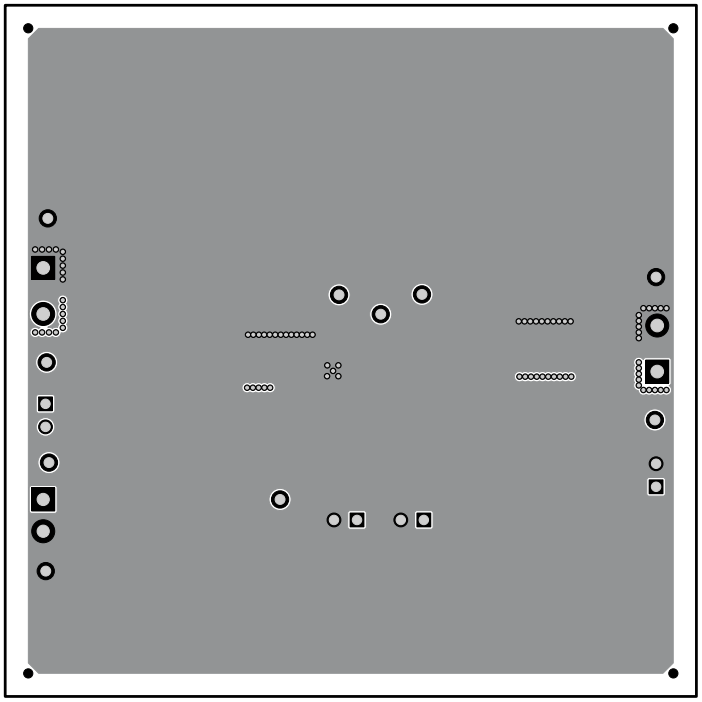

Figure 3-5. TPS54821EVM-049 Bottom-Side Layout

4 Schematic and Bill of Materials

This section presents the TPS54821EVM-049 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54821EVM-049.

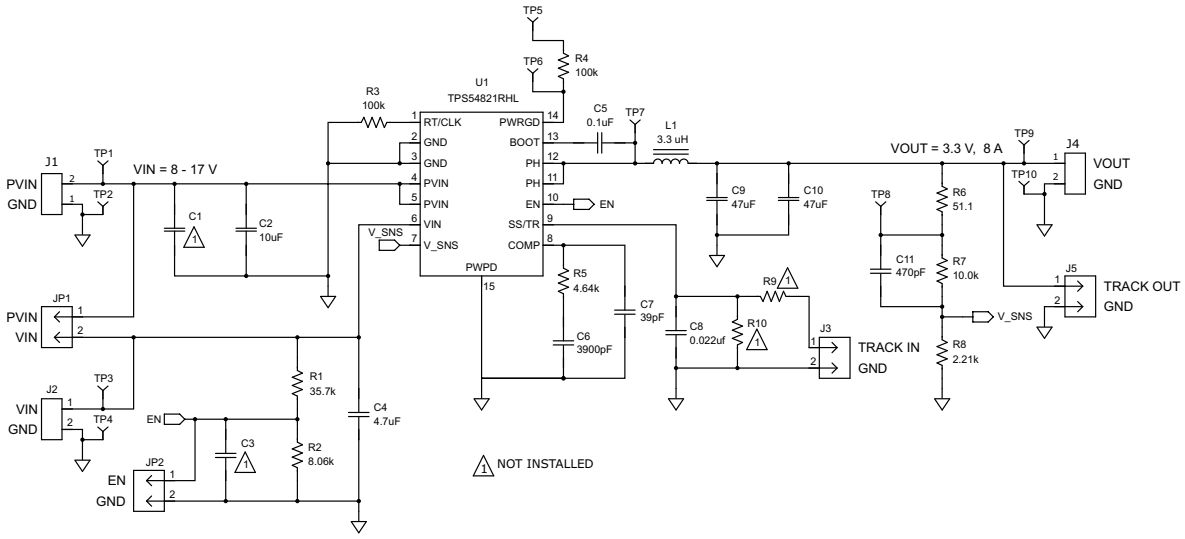

Figure 4-1. TPS54821EVM-049 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54821EVM-049.

Table 4-1. TPS54821EVM-049 Bill of Materials

COUNT	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
0	C1	Open	Capacitor, Ceramic	1210	Std	Std
1	C2	10 µF	Capacitor, Ceramic, 25 V, X5R, 20%	1210	Std	Std
0	C3		Capacitor, Ceramic	0603	Std	Std
1	C4	4.7 µF	Capacitor, Ceramic, 25 V, X5R, 10%	0805	Std	Std
1	C5	0.1 µF	Capacitor, Ceramic, 25 V, X5R, 10%	0603	Std	Std
1	C6	3900 pF	Capacitor, Ceramic, 50 V, X7R, 10%	0603	Std	Std
1	C7	39 pF	Capacitor, Ceramic, 50 V, COG, 10%	0603	Std	Std
1	C8	0.022 µF	Capacitor, Ceramic, 25 V, X7R, 10%	0603	Std	Std
2	C9, C10	47 µF	Capacitor, Ceramic, 10 V, X5R, 10%	1210	Std	Std
0	C11	470 pF	Capacitor, Ceramic, 50 V, X7R, 10%	0603	Std	Std
1	J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5 mm	0.27 × 0.25 inch	ED555/2DS	OST
2	J1, J4	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1 mm	0.40 × 0.35 inch	ED120/2DS	OST
4	JP1, JP2,J3, J5	PEC02SAAN	Header, Male 2-pin, 100 mil spacing	0.100 inch × 2	PEC02SAAN	Sullins
1	L1	3.3 µH	Inductor, SMT, 10-A, 13.7 milliΩ	0.400 × 0.453 inch	IHLP4040DZER3R3M01	Vishay
1	R1	35.7 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	8.06 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R4	100 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	4.64 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	51.1	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	10.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	2.21 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R9, R10	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	TP1, TP3, TP7, TP9	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
6	TP2, TP4, TP5, TP6, TP8, TP10	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
1	U1	TPS54821RHL	IC, 1.6V-17V Synchronous Buck PWM Converter with Integrated MOSFET	3.5mm × 3.5mm QFN14	TPS54821RHL	TI
2	—		Shunt, 100-mil, Black	0.100	929950-00	3M
1	—		Label (see note 5)	1.25 × 0.25 inch	THT-13-457-10	Brady
1	—		PCB, 2.5” × 2.5” × 0.062”		PWR049	Any

Notes

1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk (‘**’) cannot be substituted. All other components can be substituted with equivalent MFG's components.
5. Install label in silkscreened box after final wash. Text shall be 8 pt font

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2011) to Revision A (August 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2

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