

MAX98314

Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

General Description

The MAX98314 mono 3.2W Class D amplifier provides Class AB audio performance with Class D efficiency. This device offers five selectable gain settings (0dB, 3dB, 6dB, 9dB, and 12dB) set by a single gain-select input (GAIN).

Active emissions limiting (AEL) edge rate and overshoot control circuitry and a filterless spread-spectrum modulation (SSM) scheme greatly reduce EMI and eliminate the need for output filtering found in traditional Class D devices.

The IC's low 0.95mA at 3.7V, 1.2mA at 5.0V quiescent current extends battery life in portable applications.

Highly linear, integrated input coupling capacitors (C_{IN}) reduce solution size and provide excellent THD+N, PSRR, and CMRR performance at low frequencies vs. standard Class D amplifiers using external input capacitors.

The IC is available in a small 9-bump, 0.3mm pitch WLP (1.0mm x 1.0mm x 0.80mm) package and is specified over the -40°C to +85°C extended temperature range.

Applications

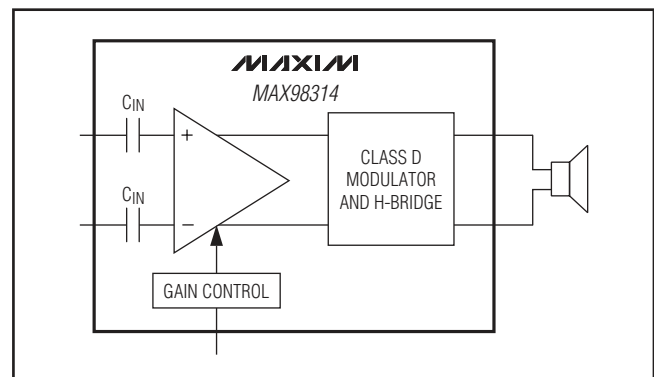
Mobile Phones
Portable Audio
Notebook Computers
MP3 Players
Netbook Computers
VoIP Phones

Ordering Information appears at end of data sheet.

Features

- ◆ **Integrated Input Coupling Capacitors with Excellent Linearity**
 - ◇ $f_C = 100\text{Hz}$ (6dB)
 - ◇ $f_C = 200\text{Hz}$ (12dB)
- ◆ **Low Quiescent Current**
 - ◇ 0.95mA at 3.7V
 - ◇ 1.2mA at 5.0V
- ◆ **Delivers High Output Power at 10% THD+N**
 - ◇ 3.2W into 4Ω, $V_{PVDD} = 5V$
 - ◇ 960mW into 8Ω, $V_{PVDD} = 3.7V$
- ◆ **Ultra-Low Noise: 19μV**
- ◆ **Eliminates Output Filtering Requirement**
 - ◇ Spread Spectrum and Active Emissions Limiting
- ◆ **Click-and-Pop Suppression**
- ◆ **Thermal and Overcurrent Protection**
- ◆ **Low Current Shutdown Mode**
- ◆ **Small, Space-Saving Package**

Simplified Block Diagram

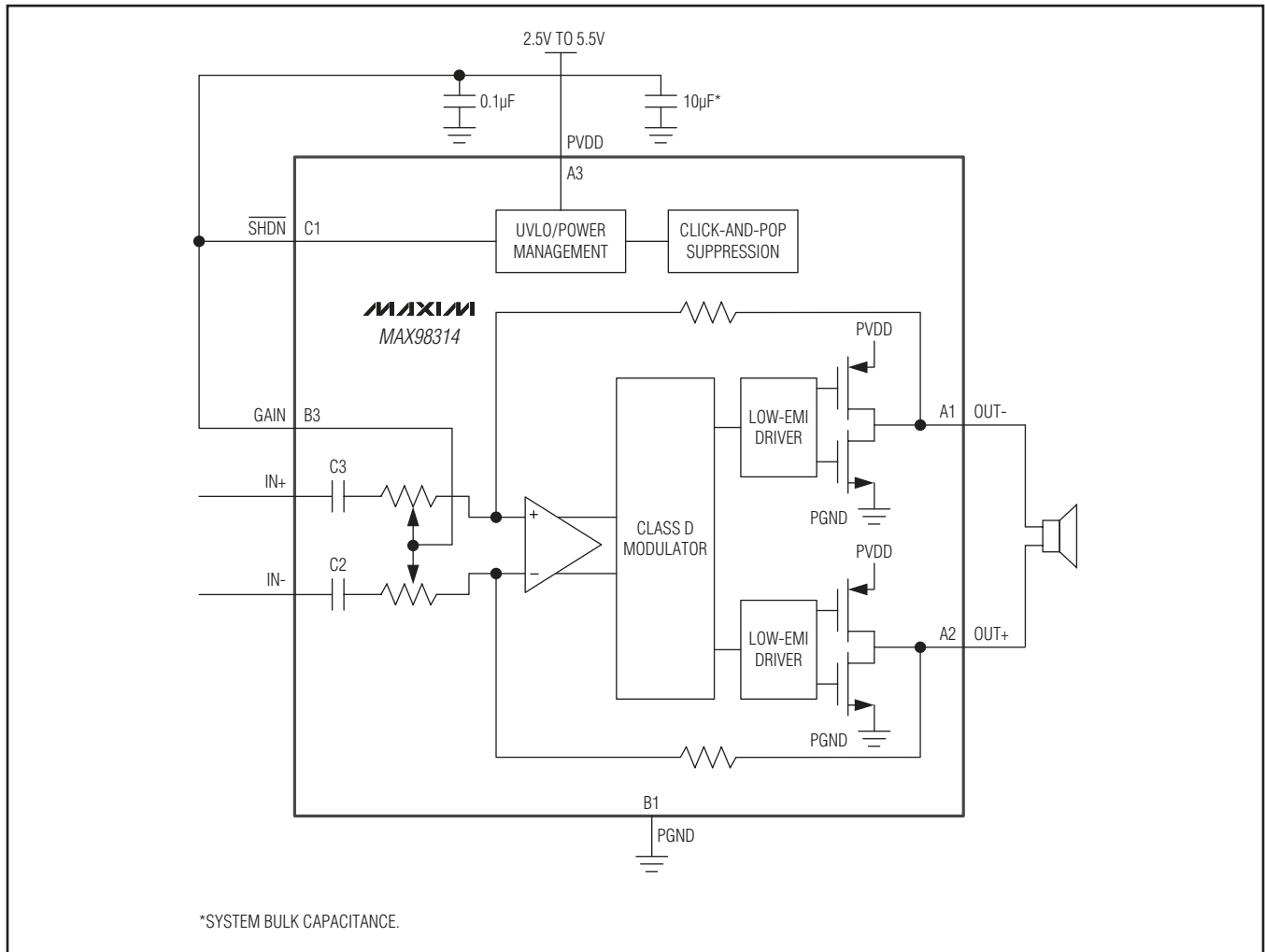


For related parts and recommended products to use with this part, refer to: www.maxim-ic.com/MAX98314.related

MAX98314

Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

Functional Diagram/Typical Application Circuit



Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

ABSOLUTE MAXIMUM RATINGS

PVDD, IN+, IN-, $\overline{\text{SHDN}}$, GAIN to PGND.....	0.3V to +6V	Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) for Multilayer Board
OUT+, OUT- to PGND.....	0.3V to ($V_{\text{PVDD}} + 0.3\text{V}$)	WLP (derate 10.64mW/°C above +70°C).....
Continuous Current In/Out of PVDD, PGND, OUT_.....	750mA	Junction Temperature
Continuous Input Current (all other pins).....	$\pm 20\text{mA}$	Operating Temperature Range.....
Duration of Short Circuit Between		Storage Temperature Range.....
OUT_ to PVDD, PGND	Continuous	Soldering Temperature (reflow)
Between OUT+ and OUT- Pins	Continuous	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP

Junction-to-Ambient Thermal Resistance (θ_{JA})	102°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	47°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{\text{PVDD}} = V_{\overline{\text{SHDN}}} = V_{\text{GAIN}} = 5\text{V}$, $V_{\text{PGND}} = 0\text{V}$, $A_V = 6\text{dB}$ ($\text{GAIN} = \text{PVDD}$), $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = T_{\text{MIN}}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Note 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AMPLIFIER CHARACTERISTICS							
Supply Voltage Range	V_{PVDD}	Guaranteed by PSRR test		2.5		5.5	V
Undervoltage Lockout	UVLO	PVDD falling			1.8	2.2	V
Quiescent Current	I_{PVDD}	$V_{\text{PVDD}} = 5\text{V}$			1.2	1.8	mA
		$V_{\text{PVDD}} = 3.7\text{V}$			0.95		
Shutdown Supply Current	$I_{\overline{\text{SHDN}}}$	$V_{\overline{\text{SHDN}}} = 0\text{V}$, $T_A = +25^\circ\text{C}$			< 0.1	10	μA
Turn-On Time	t_{ON}				3.7	10	ms
Bias Voltage	V_{BIAS}			$V_{\text{PVDD}}/2$			V
Voltage Gain	A_V	$f = 1\text{kHz}$	GAIN connected to PGND	11.75	12	12.25	dB
			GAIN connected to PGND through 100k Ω $\pm 5\%$ resistor	8.75	9	9.25	
			GAIN connected to PVDD	5.75	6	6.25	
			GAIN connected to PVDD through 100k Ω $\pm 5\%$ resistor	2.75	3	3.25	
			GAIN unconnected	-0.25	0	+0.25	
Input Capacitance	C_{IN}	All gains		0.011			μF
Highpass Corner Frequency	f_C	-3dB down	$A_V = 12\text{dB}$	199			Hz
			$A_V = 9\text{dB}$	139			
			$A_V = 6\text{dB}$	63	100	189	
			$A_V = 3\text{dB}$	70			
			$A_V = 0\text{dB}$	50			

Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

ELECTRICAL CHARACTERISTICS (continued)

($V_{PVDD} = V_{SHDN} = V_{GAIN} = 5V$, $V_{PGND} = 0V$, $A_V = 6dB$ (GAIN = PVDD), $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Common-Mode Rejection Ratio	CMRR	$f_{IN} = 1kHz$, input referred		67		dB	
Output Offset Voltage	V_{OS}	$T_A = +25^\circ C$ (Note 4)		± 1	± 3	mV	
Click-and-Pop Level	K_{CP}	$R_L = 8\Omega + 68\mu H$, peak voltage, $T_A = +25^\circ C$, A-weighted, 32 samples per second, $T_A = +25^\circ C$ (Notes 4, 5)	Into shutdown	-59		dBV	
			Out of shutdown	-82			
Power-Supply Rejection Ratio (Note 4)	PSRR	$V_{PVDD} = 2.5V$ to $5.5V$, $T_A = +25^\circ C$ $V_{RIPPLE} = 200mV_{P-P}$	$f = 217Hz$	70	90	dB	
			$f = 1kHz$	74			
			$f = 20kHz$	72	49		
Output Power	P_{OUT}	THD+N = 10% $f = 1kHz$ $R_L = 4\Omega + 33\mu H$	$V_{PVDD} = 5.0V$	3.2		W	
			$V_{PVDD} = 4.2V$	2.2			
			$V_{PVDD} = 3.7V$	1.7			
			THD+N = 1%	$V_{PVDD} = 5.0V$	2.6		
			$V_{PVDD} = 4.2V$	1.8			
			$V_{PVDD} = 3.7V$	1.4			
			THD+N = 10%	$V_{PVDD} = 5.0V$	1.8		
			$V_{PVDD} = 4.2V$	1.2			
Total Harmonic Distortion Plus Noise	THD+N	$f_{IN} = 1kHz$	$R_L = 4\Omega$, $P_{OUT} = 1W$	0.03	0.1	%	
			$R_L = 8\Omega$ $P_{OUT} = 0.725W$	0.03			
Output Noise	V_N	A-weighted (Note 4)	$A_V = 12dB$	31		μV_{RMS}	
			$A_V = 9dB$	26			
			$A_V = 6dB$	23			
			$A_V = 3dB$	21			
			$A_V = 0dB$	19			
Efficiency	η	$R_L = 8\Omega$, $P_{OUT} = 1.8W$, $f = 1kHz$		93		%	
Oscillator Frequency	f_{OSC}			300		kHz	
Spread-Spectrum Bandwidth				20		kHz	
Current Limit				2.8		A	
Thermal Shutdown Level				155		$^\circ C$	

Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

ELECTRICAL CHARACTERISTICS (continued)

($V_{PVDD} = V_{SHDN} = V_{GAIN} = 5V$, $V_{PGND} = 0V$, $A_V = 6dB$ (GAIN = PVDD), $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Hysteresis				15		$^\circ C$
DIGITAL INPUT (\overline{SHDN})						
Input Voltage High	V_{INH}	$V_{PVDD} = 2.5V$ to $5.5V$	1.4			V
Input Voltage Low	V_{INL}	$V_{PVDD} = 2.5V$ to $5.5V$			0.4	V
Input Leakage Current		$T_A = +25^\circ C$			± 1	μA

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Specifications over temperature limits are guaranteed by design.

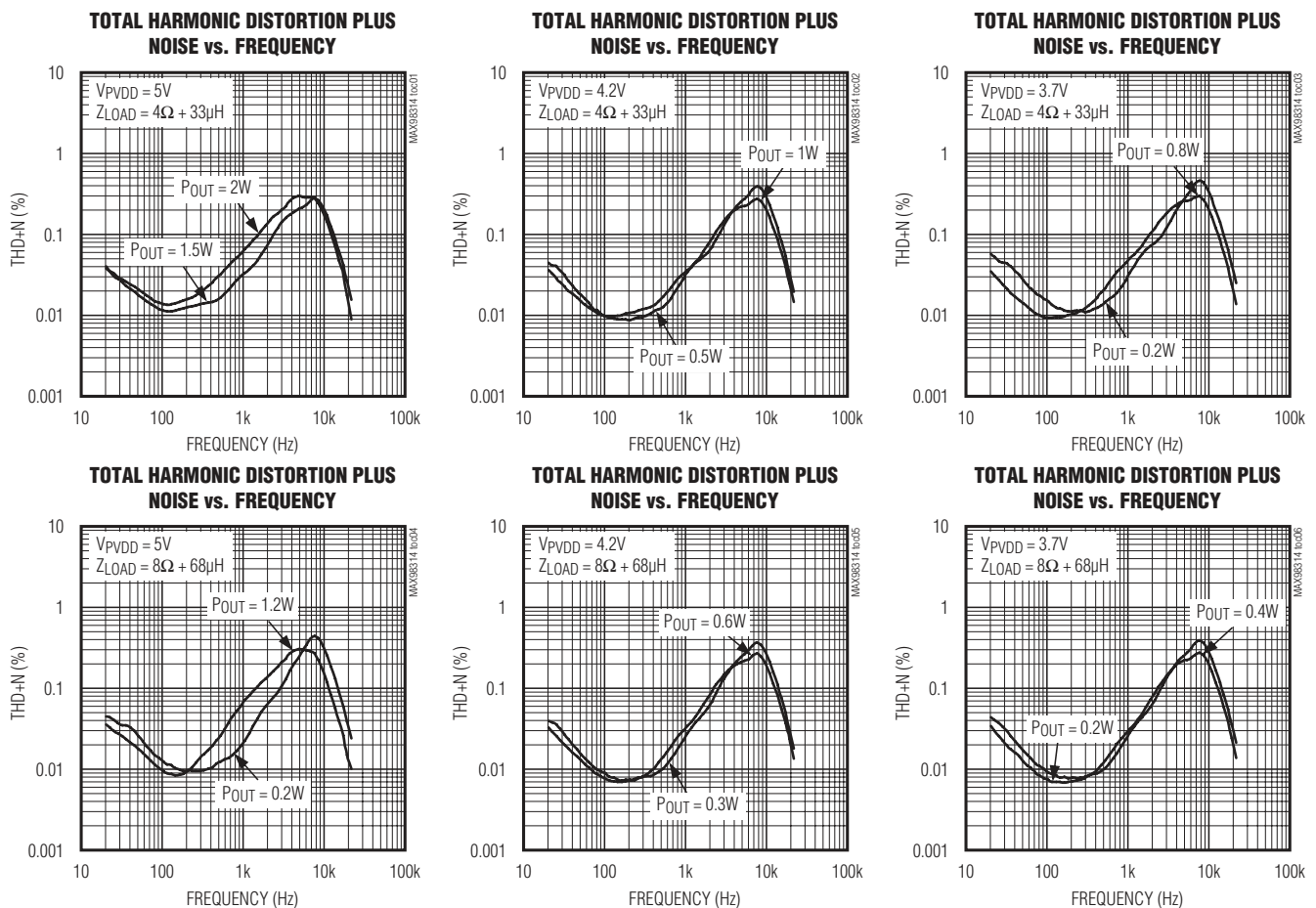
Note 3: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For $R_L = 4\Omega$, $L = 33\mu H$. For $R_L = 8\Omega$, $L = 68\mu H$.

Note 4: Amplifier inputs AC-coupled to ground.

Note 5: Mode transitions controlled by \overline{SHDN} control pin.

Typical Operating Characteristics

($V_{PVDD} = V_{SHDN} = 5.0V$, $V_{PGND} = 0V$, $A_V = 6dB$, $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = +25^\circ C$, unless otherwise noted.)

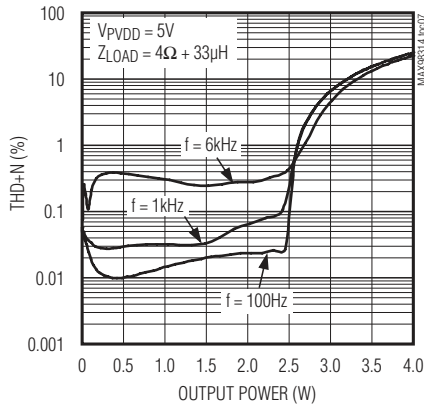


Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

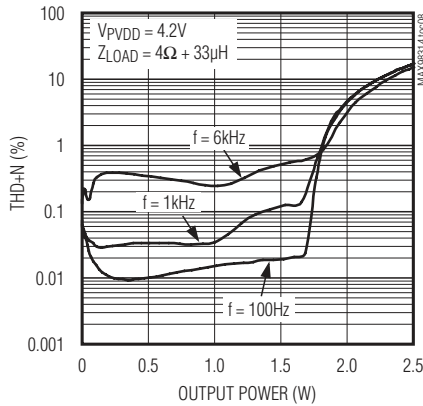
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{SHDN} = 5.0V$, $V_{PGND} = 0V$, $A_V = 6dB$, $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = +25^\circ C$, unless otherwise noted.)

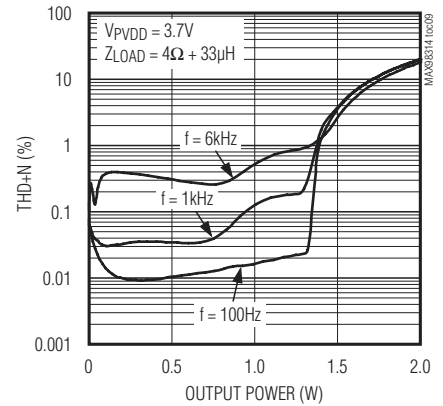
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



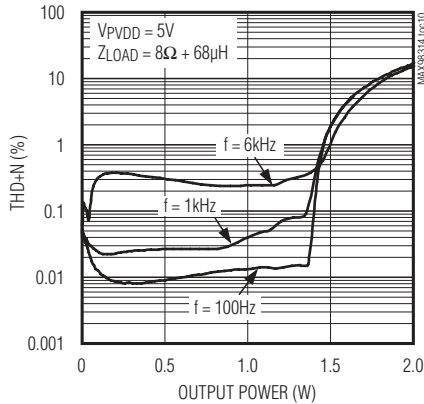
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



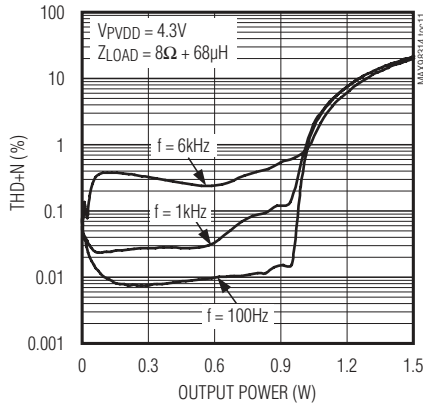
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



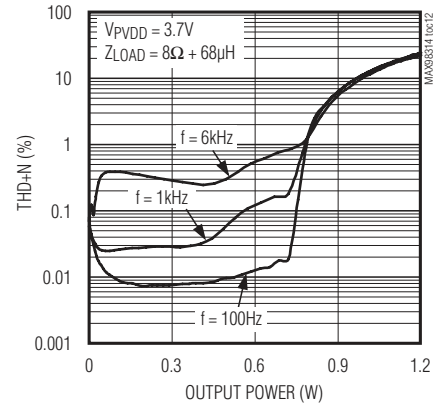
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



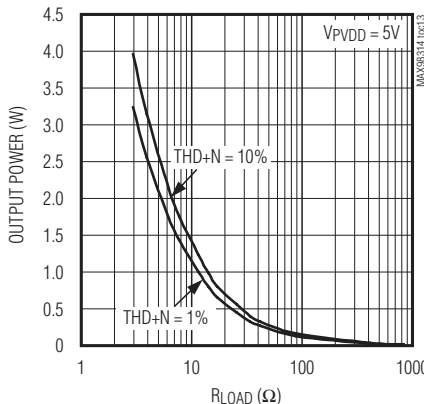
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



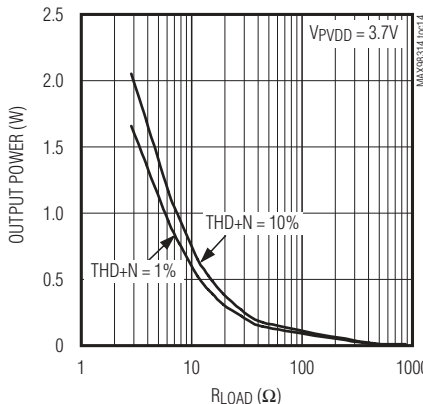
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



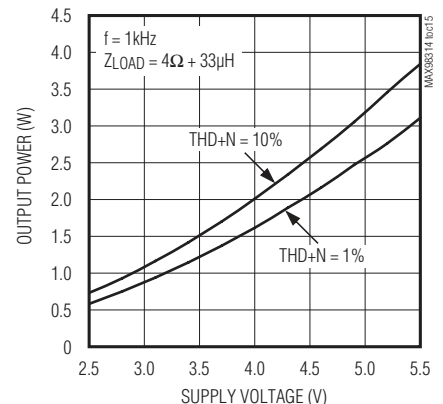
OUTPUT POWER vs. LOAD RESISTANCE



OUTPUT POWER vs. LOAD RESISTANCE



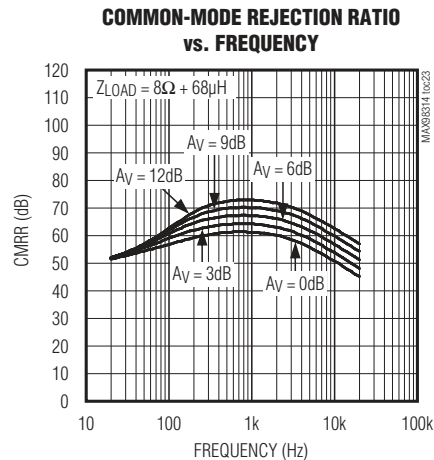
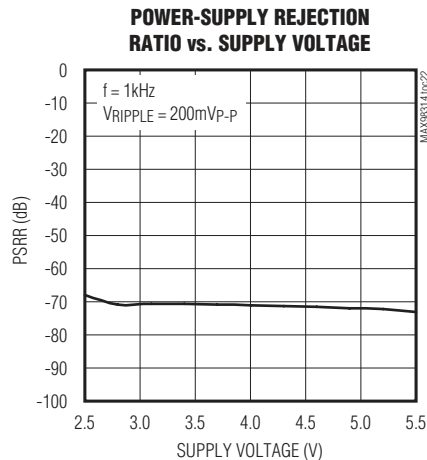
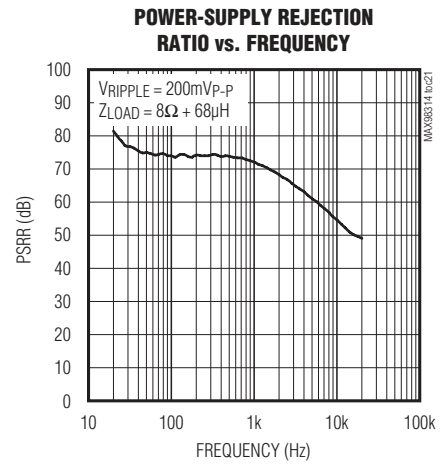
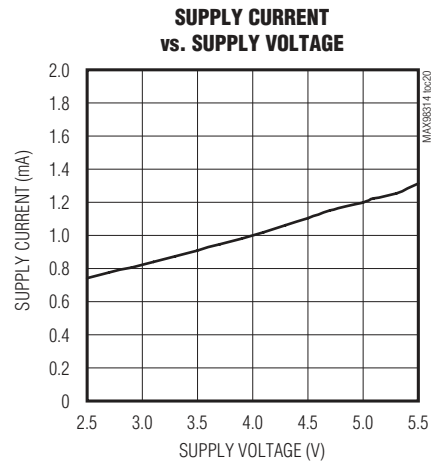
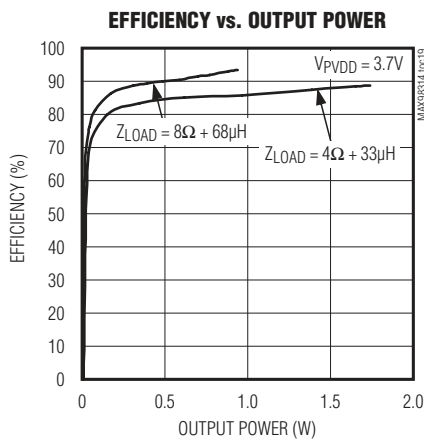
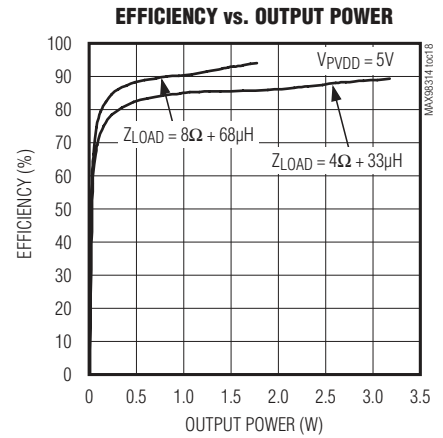
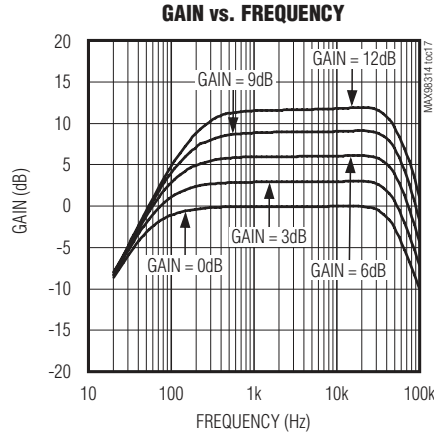
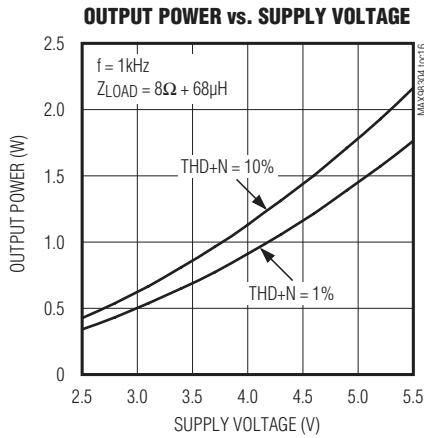
OUTPUT POWER vs. SUPPLY VOLTAGE



Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

Typical Operating Characteristics (continued)

($V_{PVDD} = V_{SHDN} = 5.0V$, $V_{PGND} = 0V$, $A_V = 6dB$, $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = +25^\circ C$, unless otherwise noted.)



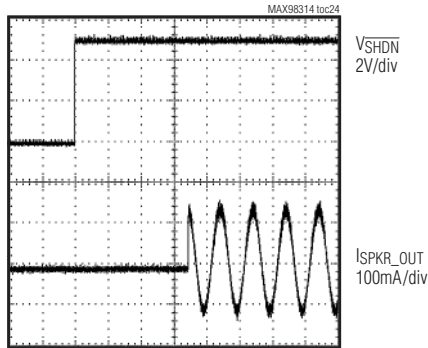
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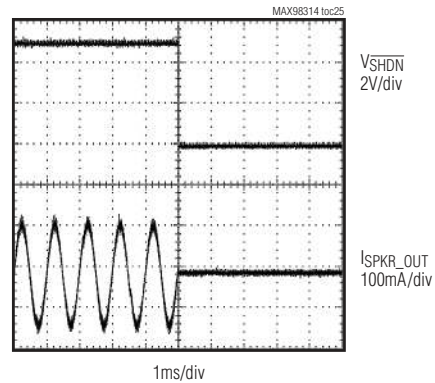
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{SHDN} = 5.0V$, $V_{PGND} = 0V$, $A_V = 6dB$, $R_L = \infty$, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = +25^\circ C$, unless otherwise noted.)

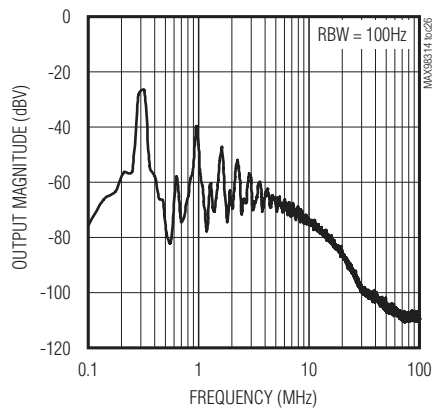
STARTUP RESPONSE



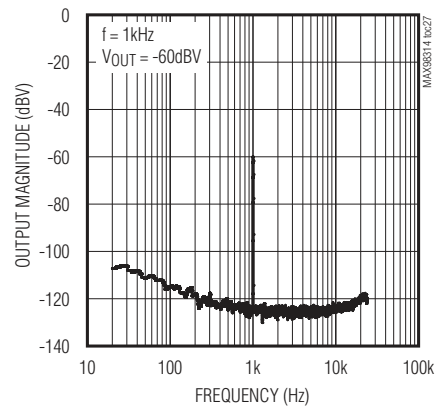
SHUTDOWN RESPONSE



WIDEBAND vs. FREQUENCY



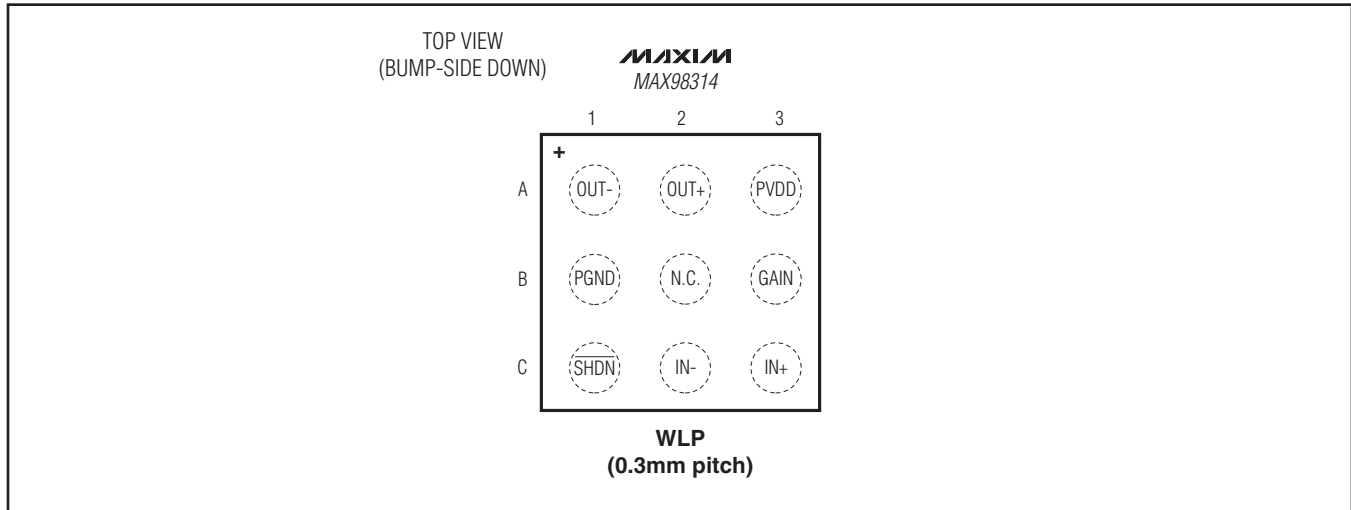
NARROWBAND vs. FREQUENCY



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Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

Pin Configuration



Pin Description

BUMP	NAME	FUNCTION
A1	OUT-	Negative Speaker Output
A2	OUT+	Positive Speaker Output
A3	PVDD	Power Supply. Bypass PVDD with a 0.1 μ F and 10 μ F capacitor to PGND.
B1	PGND	Power Ground
B2	N.C.	No Connection. Can be left unconnected or connected to PGND.
B3	GAIN	Gain Select. See Table 1 for GAIN settings.
C1	SHDN	Active-Low Shutdown Input. Drive SHDN low to place the device in shutdown.
C2	IN-	Inverting Audio Input
C3	IN+	Noninverting Audio Input

Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

Detailed Description

The MAX98314 features low quiescent current, a low-power shutdown mode, comprehensive click-and-pop suppression, and excellent RF immunity.

The IC offers Class AB audio performance with Class D efficiency in a minimal board-space solution. The Class D amplifier features spread-spectrum modulation, edge-rate, and overshoot control circuitry that offers significant improvements to switch-mode amplifier radiated emissions.

The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier additionally includes thermal overload and short-circuit protection.

Highly linear, integrated input coupling capacitors (C_{IN}) reduce solution size and provide excellent THD+N, PSRR, and CMRR performance at low frequencies vs. standard Class D amplifiers using external input capacitors.

Class D Speaker Amplifier

The IC's filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent switching current overhead.

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet electromagnetic interference (EMI) regulation standards. Maxim's patented active emissions limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions, while maintaining up to 93% efficiency.

The spread-spectrum modulation mode flattens wide-band spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The IC's spread-spectrum modulator randomly varies the switching frequency by $\pm 20\text{kHz}$ around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 1).

Amplifier Current Limit

If the output current of the speaker amplifier exceeds the current limit (2.8A typ), the IC disables the outputs for approximately 100 μs . At the end of 100 μs , the outputs are reenabled. If the fault condition still exists, the IC continues to disable and reenables the outputs until the fault condition is removed.

Selectable Amplifier Gain

The IC offers five programmable gain settings, selectable by a single gain input (GAIN).

Table 1. GAIN Selection

GAIN PIN	MAXIMUM GAIN (dB)
Connect to PGND	12
Connect to PGND through 100k Ω $\pm 5\%$	9
Connect to PVDD	6
Connect to PVDD through 100k Ω $\pm 5\%$	3
Unconnected	0

Integrated Input Coupling Capacitors (C_{IN})

The IC integrates two 0.011 μF input coupling capacitors, C_{IN} . The input coupling capacitors, in conjunction with the amplifier's internal input resistance (R_{IN}), form a first-order highpass filter that removes the DC bias from the incoming signal. These capacitors allow the amplifier to bias the signal to an optimum DC level.

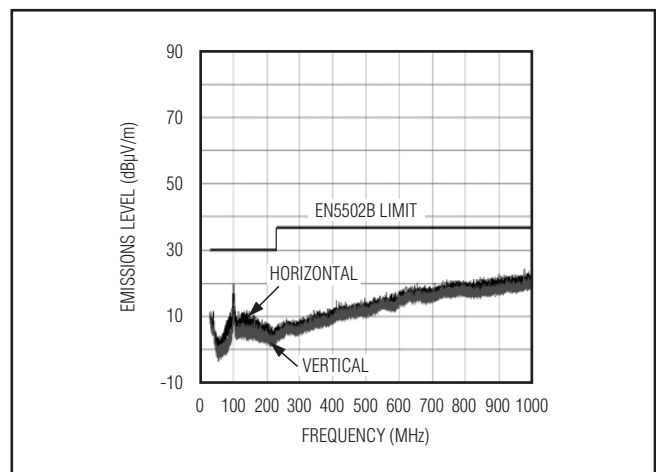


Figure 1. EMI Performance with 60cm of Speaker Cable, No Output Filter

Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

Assuming zero source impedance, the -3dB corner frequency, f_{-3dB} , is:

$$f_{-3dB} = 1/2\pi R_{IN}C_{IN} \text{ [Hz]}$$

The 100ppm/V voltage coefficient of the integrated input coupling capacitor results in excellent low-frequency THD+N performance. Figure 2 illustrates the superior linearity of the IC's integrated input coupling capacitors compared to a similar amplifier with external 0.01 μ F X7R and X5R 0402 input coupling capacitors.

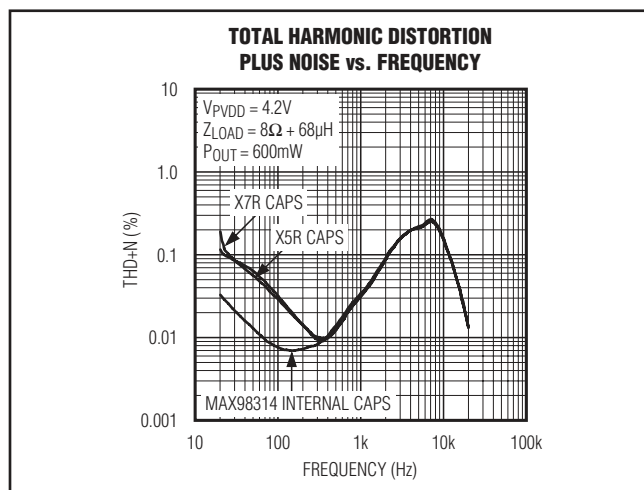


Figure 2. Low-Frequency THD+N Performance

Shutdown

The IC features a low-power shutdown mode, drawing < 0.1 μ A (typ) of supply current. Drive $\overline{\text{SHDN}}$ low to put the IC into shutdown.

Click-and-Pop Suppression

The speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device. When entering shutdown, the differential speaker outputs ramp down to PGND quickly and simultaneously.

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter. The filter adds cost and size, and decreases efficiency and THD+N performance. The IC's filterless modulation scheme does not require an output filter.

Because the switching frequency of the IC is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10 μ H. Typical 8 Ω speakers exhibit series inductances in the 20 μ H to 100 μ H range.

Speaker Amplifier Power-Supply Input (PVDD)

PVDD powers the speaker amplifier and ranges from 2.5V to 5.5V. Bypass PVDD with a 0.1 μ F and 10 μ F capacitor to PGND. Apply additional bulk capacitance at the device if long input traces between PVDD and the power source are used.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As the load impedance decreases, the current drawn from the device increases. At higher current, the resistance of the output traces decrease the power delivered to the load. For example, if 2W is delivered from the device output to a 4 Ω load through 100m Ω of total speaker trace, 1.904W is delivered to the speaker. If power is delivered through 10m Ω of total speaker trace, 1.99W is delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB layers.

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Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to [Application Note 1891: Wafer-Level Packaging \(WLP\) and Its Applications](#). Figure 3 shows the dimensions of the WLP balls used on the IC.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX98314EWL+	-40°C to +85°C	9 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

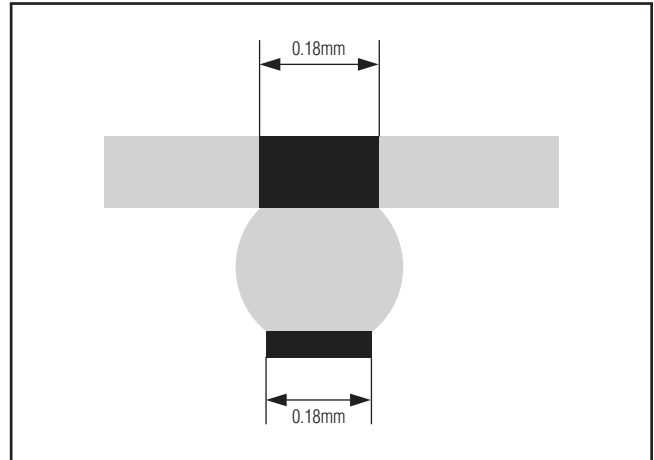


Figure 3. WLP Ball Dimensions

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Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP (0.3mm pitch)	W90A0+1	21-0539	Refer to Application Note 1891

TOP VIEW

SIDE VIEW

COMMON DIMENSIONS	
A	0.75 ±0.05
A1	0.16 ±0.03
A2	0.59 REF
A3	0.040 BASIC
b	∅0.21 ±0.03
D1	0.60 BASIC
E1	0.60 BASIC
e	0.30 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W90A0+1	0.95	0.98	0.95	0.98	NONE

BOTTOM VIEW

NOTES:

- Terminal pitch is defined by terminal center to center value.
- Outer dimension is defined by center lines between scribe lines.
- All dimensions in millimeter.
- Marking shown is for package orientation reference only.
- Tolerance is ± 0.02 unless specified otherwise.
- All dimensions apply to PbFree (+) package codes only.
- Front - side finish can be either Black or Clear.

TITLE			
Package Outline 9 bumps, WLP Pkg. 0.3MM Pitch			
APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0539	B	

-DRAWING NOT TO SCALE-

MAX98314

Mono 3.2W Class D Amplifier with Integrated Input Coupling Capacitors

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/11	Initial release	—

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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