STEREO DIGITAL AMPLIFIER POWER STAGE

FEATURES

- **2×20 W at 10% THD+N Into 8-Ω BTL**
- **2×25 W at 10% THD+N Into 6-Ω BTL**
- **>100-dB SNR (A-Weighted)**
- **<0.1% THD+N at 1 W**
- **Thermally Enhanced Package:**
  - **DDV (44-pin HTSSOP)**
- **High-Efficiency Power Stage (>90%) With 140-mΩ Output MOSFETs**
- **Power-On Reset for Protection on Power Up Without Any Power-Supply Sequencing**
- **Integrated Self-Protection Circuits Including Undervoltage, Overtemperature, Overload, Short Circuit**
- **PWM Activity Detector to detect stopped PWM inputs and protect the system**
- **Error Reporting**
- **EMI Compliant When Used With Recommended System Design**
- **Intelligent Gate Drive**
- **Pin Compatible With the TAS5142DDV**

APPLICATIONS

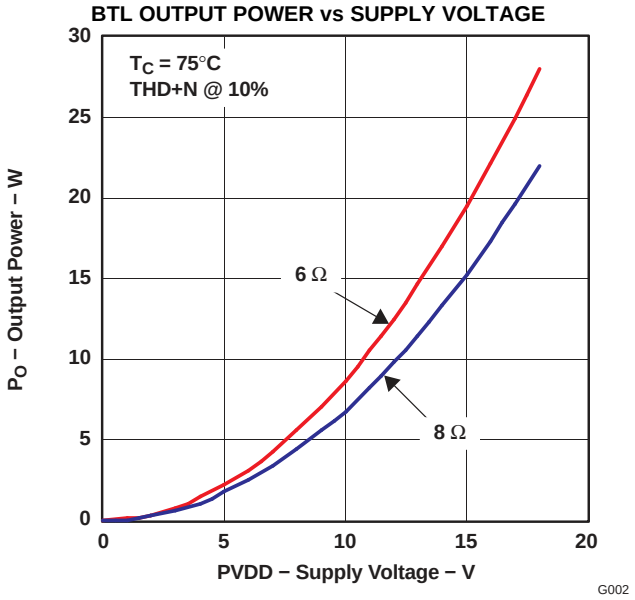
- **Televisions**
- **Mini/Micro Audio Systems**
- **DVD Receivers**
- **Home Theaters**

DESCRIPTION

The TAS5132 is an integrated stereo digital amplifier power stage with an advanced protection system. The TAS5132 is capable of driving a 6-Ω bridge-tied load (BTL) at up to 25 W per channel with low integrated noise at the output, low THD+N performance, and low idle power dissipation.

A low-cost, high-fidelity audio system can be built using a TI chipset, comprising a modulator (e.g., TAS5086) and the TAS5132. This system only requires a simple passive LC demodulation filter to deliver high-quality, high-efficiency audio amplification with proven EMI compliance. This device requires two power supplies, at 12 V for GVDD and VDD, and at 18 V for PVDD. The TAS5132 does not require power-up sequencing due to internal power-on reset. The efficiency of this digital amplifier is greater than 90% into 8 Ω, which enables the use of smaller power supplies and heatsinks.

The TAS5132 has an innovative protection system integrated on chip, safeguarding the device against a wide range of fault conditions that could damage the system. These safeguards are short-circuit protection, overcurrent protection, undervoltage protection, and overtemperature protection. The TAS5132 has a new proprietary current-limiting circuit that reduces the possibility of device shutdown during high-level music transients.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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GENERAL INFORMATION

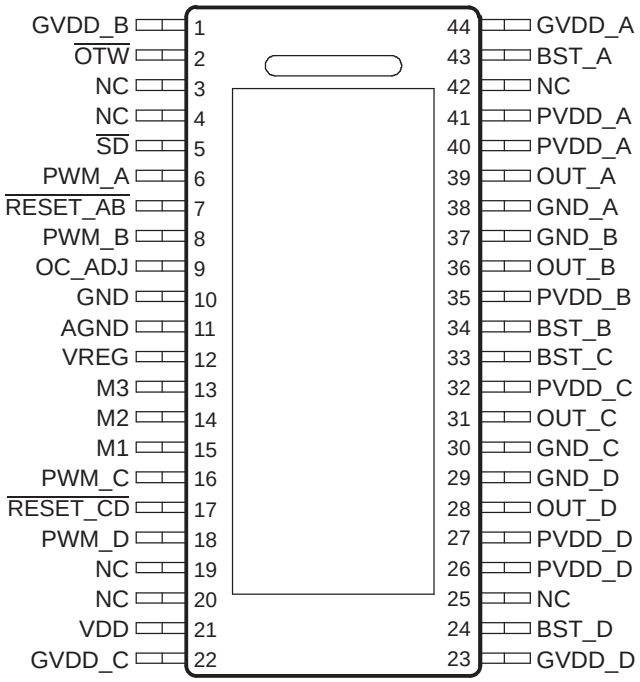
Terminal Assignment

The TAS5132 is available in a thermally enhanced package:

- 44-pin HTSSOP PowerPAD™ package (DDV)

This package type contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heatsink.

DDV PACKAGE
(TOP VIEW)



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GENERAL INFORMATION (continued)

MODE Selection Pins

MODE PINS			PWM INPUT	OUTPUT CONFIGURATION	PROTECTION SCHEME
M3	M2	M1			
0	0	0	2N (1) AD/BD modulation	2 channels BTL output	BTL mode (2)
0	0	1	Reserved		
0	1	0	1N (1) AD modulation	2 channels BTL output	BTL mode (2)
0	1	1	1N (1) AD modulation	1 channel PBTL output	PBTL mode. Only PWM_A input is used.
1	0	0	1N (1) AD modulation	4 channels SE output	Protection works similarly to BTL mode (2). Only difference in SE mode is that OUT_X is Hi-Z instead of a pulldown through internal pulldown resistor.
1	0	1	2N (1) AD/BD modulation	2 channels BTL output	Protection system work similarly to BTL mode (2) (0, 0, 0); however the PWM input protection is disabled. Also, overcurrent detection will be more sensitive and will latch if an error occurs.
1	1	0	Reserved		
1	1	1			

(1) The 1N and 2N naming convention is used to indicate the required number of PWM lines to the power stage per channel in a specific mode.
(2) An overload protection (OLP) occurring on A or B causes both channels to shut down. An OLP on C or D works similarly. Global errors like overtemperature error (OTE), undervoltage protection (UVP), and power-on reset (POR) affect all channels.

Package Heat Dissipation Ratings(1)

PARAMETER	TAS5132DDV
$R_{\theta JC}$ (°C/W)—2 BTL or 4 SE channels (8 transistors)	1.4
$R_{\theta JC}$ (°C/W)—1 BTL or 2 SE channel(s) (4 transistors)	2.6
$R_{\theta JC}$ (°C/W)—(1 transistor)	8.7
Pad area(2)	15 mm^2

(1) JC is junction-to-case, CH is case-to-heatsink.
(2) $R_{\theta CH}$ is an important consideration. Assume a 2-mil thickness of typical thermal grease between the pad area and the heatsink. The $R_{\theta CH}$ with this condition is 2.5°C/W for the DDV package.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

VDD to AGND	–0.3 V to 13.2 V
GVDD_X to AGND	–0.3 V to 13.2 V
PVDD_X to GND_X (2)	–0.3 V to 30 V
OUT_X to GND_X (2)	–0.3 V to 30 V
BST_X to GND_X (2)	–0.3 V to 43.2 V
VREG to AGND	–0.3 V to 4.2 V
GND_X to GND	–0.3 V to 0.3 V
GND_X to AGND	–0.3 V to 0.3 V
GND to AGND	–0.3 V to 0.3 V
PWM_X, OC_ADJ, M1, M2, M3 to AGND	–0.3 V to 4.2 V
$\overline{\text{RESET\_X}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$ to AGND	–0.3 V to 7 V
Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW}}$)	9 mA
Maximum operating junction temperature range, T_J	0°C to 150°C
Storage temperature range	–40°C to 125°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Minimum pulse duration, low	50 ns

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

ORDERING INFORMATION

T_A	PACKAGE	DESCRIPTION
0°C to 70°C	TAS5132DDV	44-pin HTSSOP

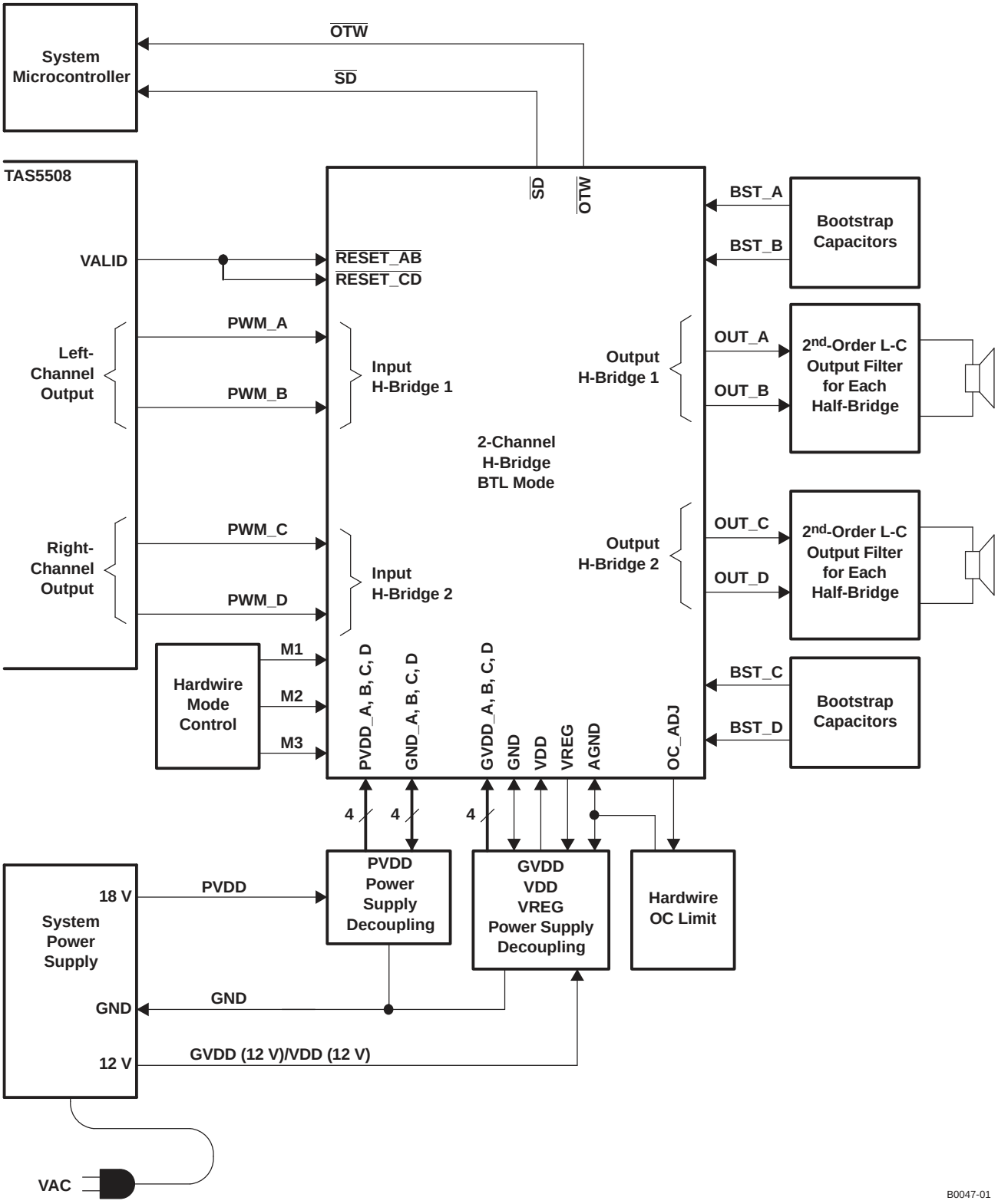
For the most current specification and package information, see the TI Web site at www.ti.com.

Terminal Functions

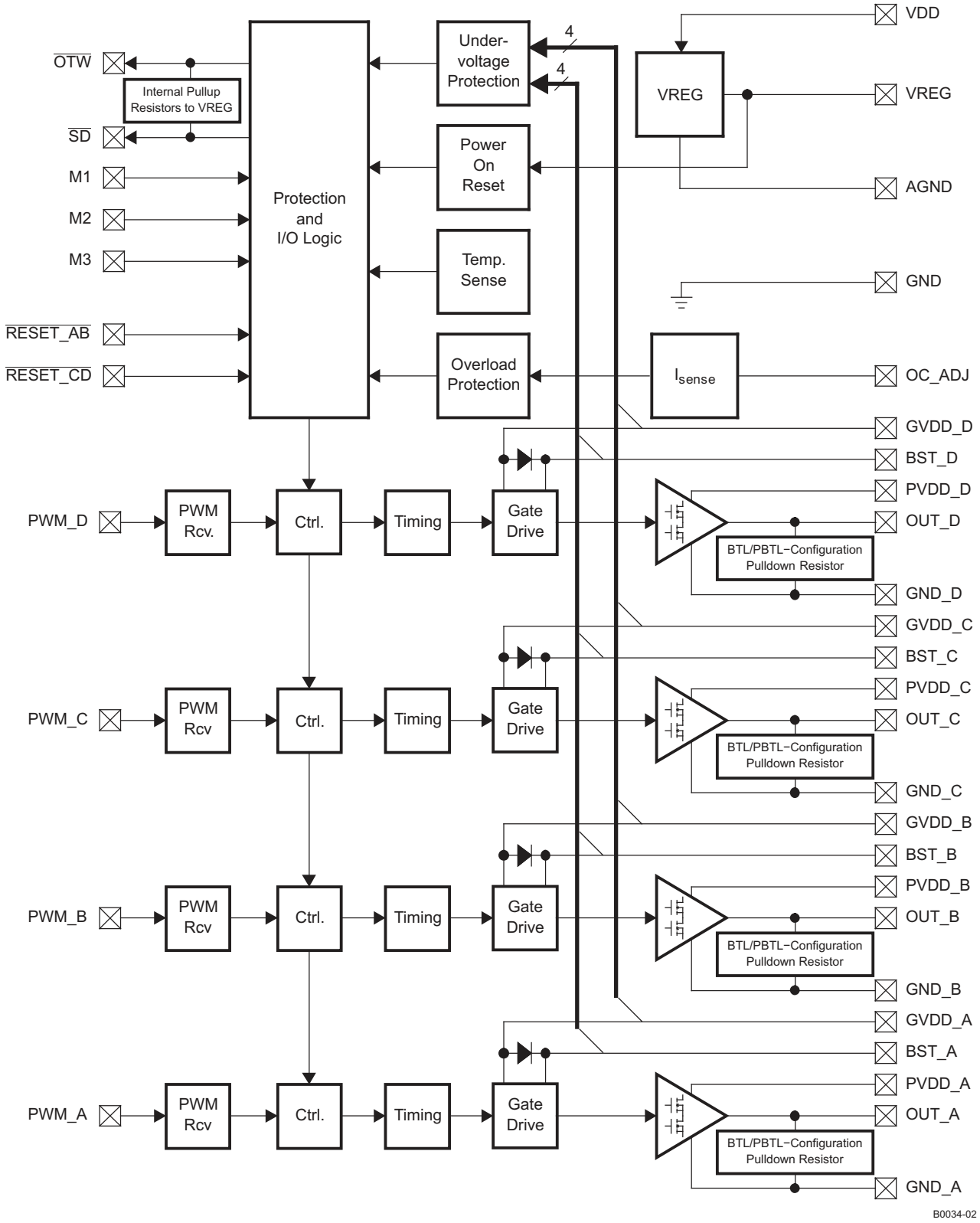
TERMINAL		FUNCTION (1)	DESCRIPTION
NAME	NO.		
AGND	11	P	Analog ground
BST_A	43	P	HS bootstrap supply (BST). External capacitor to OUT_A required.
BST_B	34	P	HS bootstrap supply (BST). External capacitor to OUT_B required.
BST_C	33	P	HS bootstrap supply (BST). External capacitor to OUT_C required.
BST_D	24	P	HS bootstrap supply (BST). External capacitor to OUT_D required.
GND	10	P	Ground
GND_A	38	P	Power ground for half-bridge A
GND_B	37	P	Power ground for half-bridge B
GND_C	30	P	Power ground for half-bridge C
GND_D	29	P	Power ground for half-bridge D
GVDD_A	44	P	Gate-drive voltage supply. Requires 0.1-µF capacitor to GND.
GVDD_B	1	P	Gate-drive voltage supply. Requires 0.1-µF capacitor to GND.
GVDD_C	22	P	Gate-drive voltage supply. Requires 0.1-µF capacitor to GND.
GVDD_D	23	P	Gate-drive voltage supply. Requires 0.1-µF capacitor to GND.
M1	15	I	Mode selection 1
M2	14	I	Mode selection 2
M3	13	I	Mode selection 3
NC	3, 4, 19, 20, 25, 42	–	No connect. Pins may be grounded.
OC_ADJ	9	O	Analog overcurrent programming. Requires resistor to ground.
$\overline{\text{OTW}}$	2	O	Overtemperature warning signal, open drain, active low
OUT_A	39	O	Output, half-bridge A
OUT_B	36	O	Output, half-bridge B
OUT_C	31	O	Output, half-bridge C
OUT_D	28	O	Output, half-bridge D
PVDD_A	40, 41	P	Power supply input for half-bridge A. Requires close decoupling of 0.1-µF capacitor to GND_A.
PVDD_B	35	P	Power supply input for half-bridge B. Requires close decoupling of 0.1-µF capacitor to GND_B.
PVDD_C	32	P	Power supply input for half-bridge C. Requires close decoupling of 0.1-µF capacitor to GND_C.
PVDD_D	26, 27	P	Power supply input for half-bridge D. Requires close decoupling of 0.1-µF capacitor to GND_D.
PWM_A	6	I	Input signal for half-bridge A
PWM_B	8	I	Input signal for half-bridge B
PWM_C	16	I	Input signal for half-bridge C
PWM_D	18	I	Input signal for half-bridge D
$\overline{\text{RESET\_AB}}$	7	I	Reset signal for half-bridge A and half-bridge B, active low
$\overline{\text{RESET\_CD}}$	17	I	Reset signal for half-bridge C and half-bridge D, active low
$\overline{\text{SD}}$	5	O	Shutdown signal, open-drain, active-low
VDD	21	P	Power supply for digital voltage regulator. Requires 0.1-µF capacitor in parallel with a 10-µF capacitor to GND.
VREG	12	P	Digital regulator supply filter. Requires 0.1-µF capacitor to AGND.

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
PVDD_X	Half-bridge supply	DC supply voltage	0	18	19	V
GVDD_X	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator input	DC supply voltage	10.8	12	13.2	V
R_L (BTL)	Load impedance	Output filter: L = 10 µH, C = 470 nF. Output AD modulation, switching frequency > 350 kHz		6-8		Ω
R_L (SE)				3-4		
R_L (PBTL)				3-4		
L_{Output} (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition		10		µH
L_{Output} (SE)				10		
L_{Output} (PBTL)				10		
F_{PWM}	PWM frame rate		192	384	432	kHz
T_J	Junction temperature		0		125	°C

AUDIO SPECIFICATIONS (BTL)

PVDD_X = 18 V, GVDD = VDD = 12 V, BTL mode, R_L = 8 Ω, R_{OC} = 22 KΩ, C_{BST} = 33-nF, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, case temperature = 75°C (unless otherwise noted). Audio performance is recorded as a chipset, using TAS5086 PWM processor with an effective modulation index limit of 96.1%. All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel, DDV package	R_L = 6 Ω, 10% THD, clipped input signal		26		W
		R_L = 8 Ω, 10% THD, clipped input signal		20		
		R_L = 6 Ω, 0 dBFS, unclipped input signal		20		
		R_L = 8 Ω, 0 dBFS, unclipped input signal		16		
THD+N	Total harmonic distortion + noise	0 dBFS		<0.1%		
		1 W		<0.06%		
V_n	Output integrated noise	A-weighted		50	200	µV
SNR	Signal-to-noise ratio (1)	A-weighted	94	105		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5086 modulator	94	105		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, 4 channels switching (2)		.6		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

AUDIO SPECIFICATIONS (Single-Ended Output)

PVDD_X = 18 V, GVDD = VDD = 12 V, SE mode, R_L = 3 Ω, R_{OC} = 22 KΩ, C_{BST} = 33-nF, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, case temperature = 75°C (unless otherwise noted). Audio performance is recorded as a chipset, using TAS5086 PWM processor with an effective modulation index limit of 96.1%. All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	TYP	UNIT
P_O	Power output per channel, DDV package	R_L = 3 Ω, 10% THD, clipped input signal	12.5	W
		R_L = 4 Ω, 10% THD, clipped input signal	10.0	
		R_L = 3 Ω, 0 dBFS, unclipped input signal	9.5	
		R_L = 4 Ω, 0 dBFS, unclipped input signal	7.5	
THD+N	Total harmonic distortion + noise	0 dBFS, 4 Ω	.09	%
		1 W, 4 Ω	.05	
V_n	Output integrated noise	A-weighted	18	μV
SNR	Signal-to-noise ratio (1)	A-weighted	100	dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5086 modulator	100	dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, 4 channels switching (2)	.6	W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

AUDIO SPECIFICATIONS (PBTL)

PVDD_X = 18 V, GVDD = VDD = 12 V, PBTL mode, R_L = 3 Ω, R_{OC} = 22 KΩ, C_{BST} = 33-nF, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, case temperature = 75°C (unless otherwise noted). Audio performance is recorded as a chipset, using TAS5086 PWM processor with an effective modulation index limit of 96.1%. All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	TYP	UNIT
P_O	Power output per channel, DDV package	R_L = 3 Ω, 10% THD, clipped input signal	50	W
		R_L = 4 Ω, 10% THD, clipped input signal	40	
		R_L = 3 Ω, 0 dBFS, unclipped input signal	37	
		R_L = 4 Ω, 0 dBFS, unclipped input signal	30	
THD+N	Total harmonic distortion + noise	0 dBFS, 3 Ω	.14	%
		1 W, 3 Ω	.02	
V_n	Output integrated noise	A-weighted	30	μV
SNR	Signal-to-noise ratio (1)	A-weighted	105	dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5086 modulator	105	dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0 W, 1 channel switching (2)	.6	W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

ELECTRICAL CHARACTERISTICS

R_L = 8 Ω, F_{PWM} = 384 kHz (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Voltage Regulator and Current Consumption						
VREG	Voltage regulator, only used as a reference node	VDD = 12 V	3	3.3	3.6	V
IVDD	VDD supply current	Operating, 50% duty cycle		6	9	mA
		Idle, reset mode		5.5	8	
IGVDD_X	Gate supply current per half-bridge	50% duty cycle		3.6	5.5	mA
		Reset mode		1.0	2.0	
IPVDD_X	Half-bridge idle current	50% duty cycle, without output filter or load		9	15	mA
		Reset mode, no switching		.1	.2	mA
Output Stage MOSFETs						
$R_{DSon,LS}$	Drain-to-source resistance, LS	T_J = 25°C, includes metallization resistance, GVDD = 12 V		140	155	mΩ
$R_{DSon,HS}$	Drain-to-source resistance, HS	T_J = 25°C, includes metallization resistance, GVDD = 12 V		140	155	mΩ
I/O Protection						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_X, voltage rising			9.6		V
$V_{uvp,G}$	Undervoltage protection limit, GVDD_X, voltage falling			9.2		V
BST_{uvpF}	Puts device into RESET when BST voltage falls below limit			6.2		V
BST_{uvpR}	Brings device out of RESET when BST voltage rises above limit			6.6		V
OTW(1)	Overtemperature warning			125		°C
OTW_{HYST}(1)	Temperature drop needed below OTW temperature for $\overline{OTW}$ to be inactive after the $\overline{OTW}$ event			25		°C
OTE(1)	Overtemperature error			155		°C
OTE-$OTW_{differential}$(1)	OTE-OTW differential			30		°C
OTE_{HYST}(1)	A reset event must occur for $\overline{SD}$ to be released following an OTE event.			30		°C
OLPC	Overload protection counter	F_{PWM} = 384 kHz		1.25		ms
I_{OC}	Overcurrent limit protection	Resistor—programmable, max. current, R_{OCP} = 22 kΩ	4.0	5.0	6.0	A
I_{OCT}	Overcurrent response time			150		ns
R_{OCP}	OC programming resistor range	Resistor tolerance = 5% for typical value; the minimum resistance should not be less than 20kΩ.	20	22		kΩ
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when $\overline{RESET}$ is active to provide bootstrap capacitor charge. Not used in SE mode		3.0		kΩ
PAD	PWM Activity Detector, causes device reset when PWM input signal is stopped.	PWM stopped and time measured for device to go into RESET (Output switching stopped)	10	25		µS

(1) Specified by design

ELECTRICAL CHARACTERISTICS (continued)

R_L= 8 Ω, F_{PWM} = 384 kHz (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Digital Specifications						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3, RESET_AB, RESET_CD	2			V
V_{IL}	Low-level input voltage				0.8	V
I_{lkg}	Input leakage current	Static, High PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3, RESET_AB, RESET_CD			100	µA
		Static, Low PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3, RESET_AB, RESET_CD	–10		10	
OTW/Shutdown (SD)						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$ to VREG, $\overline{SD}$ to VREG		20	26	32	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	3	3.3	3.6	V
		External pullup of 4.7 kΩ to 5 V			5.5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.25	0.5	V

TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

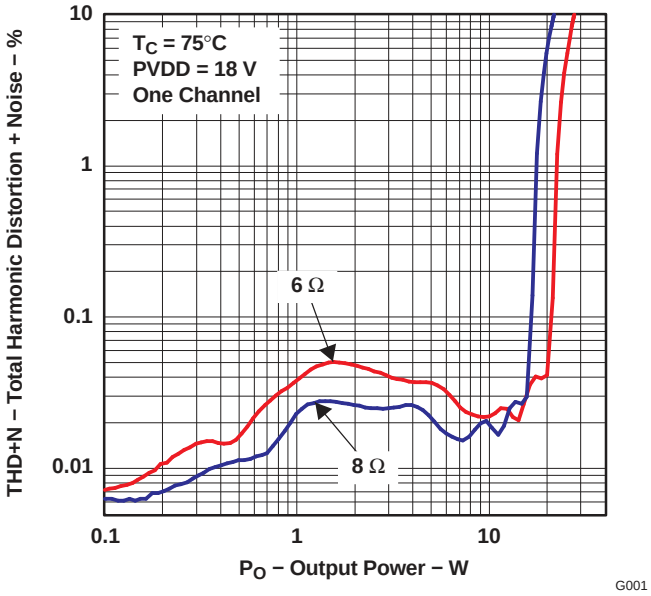


Figure 1.

OUTPUT POWER vs SUPPLY VOLTAGE

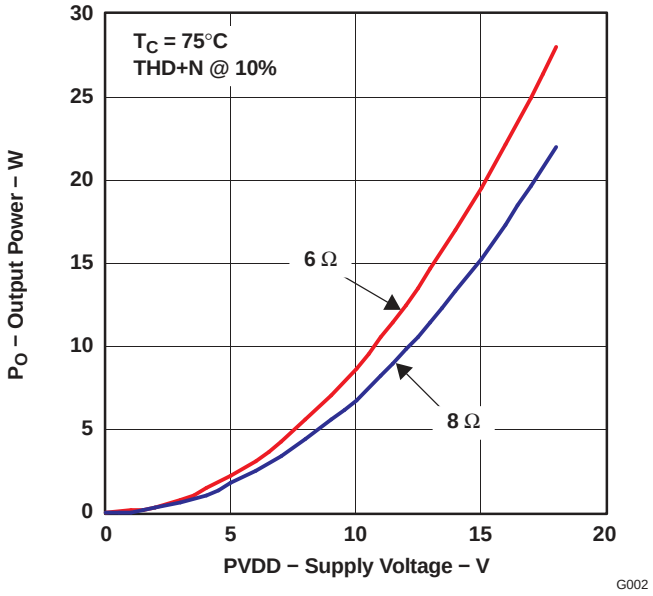


Figure 2.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

UNCLIPPED OUTPUT POWER
vs
SUPPLY VOLTAGE

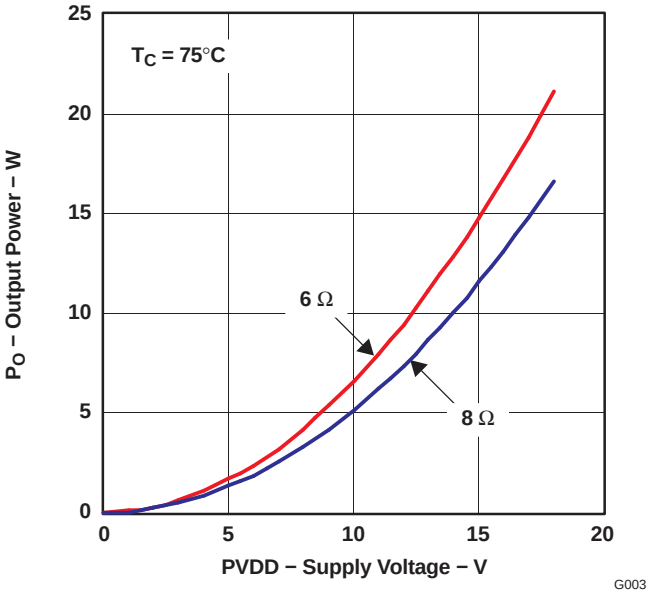


Figure 3.

SYSTEM EFFICIENCY
vs
OUTPUT POWER

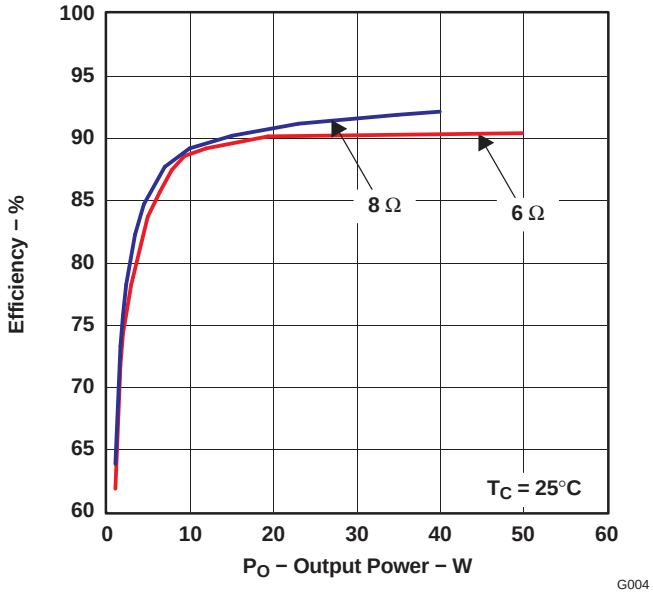


Figure 4.

SYSTEM POWER LOSS
vs
OUTPUT POWER

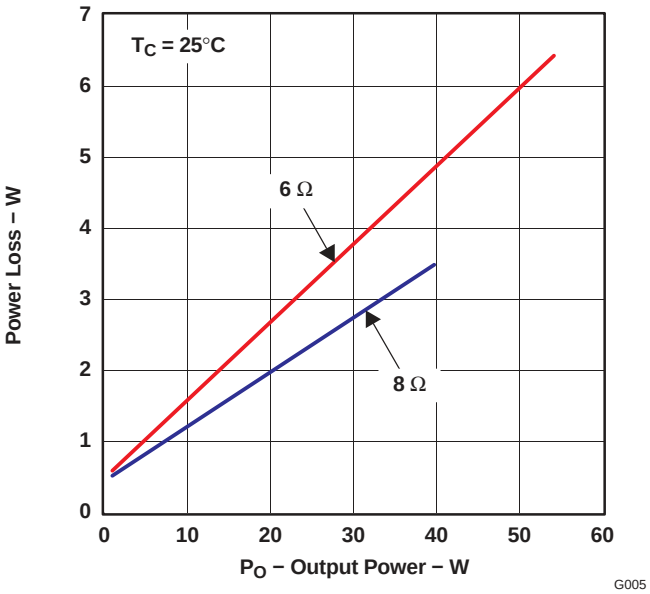


Figure 5.

SYSTEM OUTPUT POWER
vs
CASE TEMPERATURE

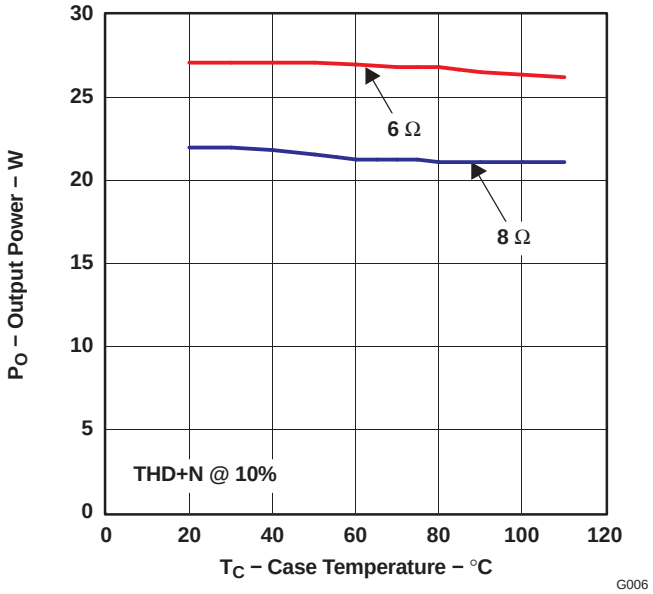


Figure 6.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

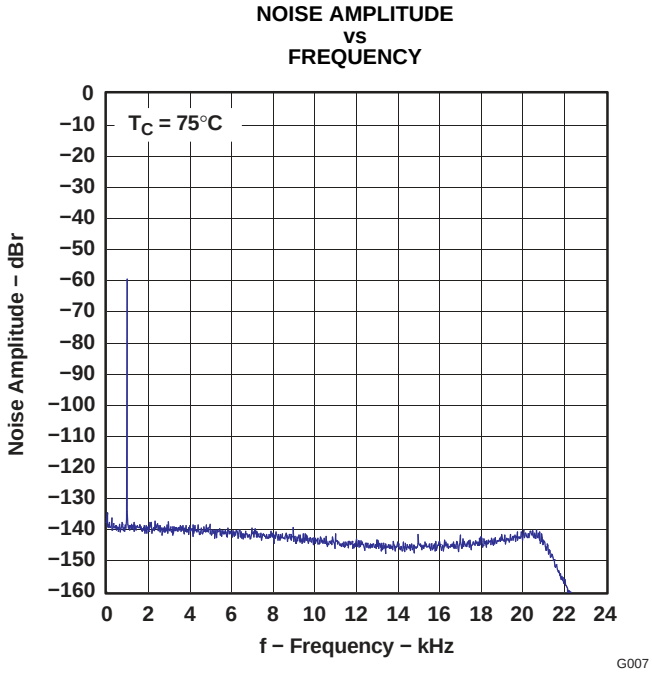


Figure 7.

TYPICAL CHARACTERISTICS, SE CONFIGURATION

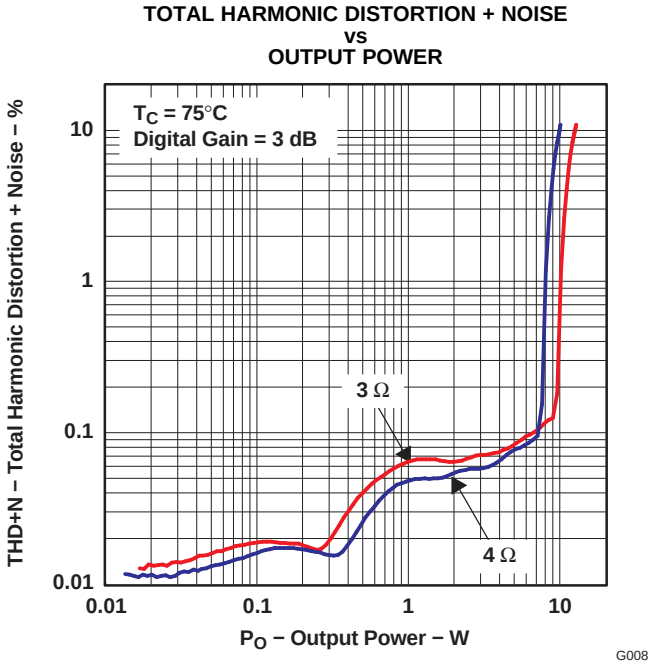


Figure 8.

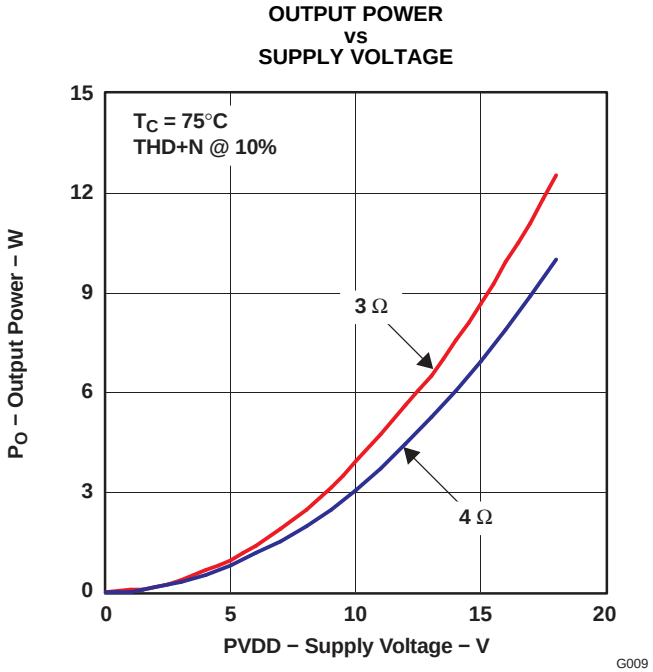


Figure 9.

TYPICAL CHARACTERISTICS, SE CONFIGURATION (continued)

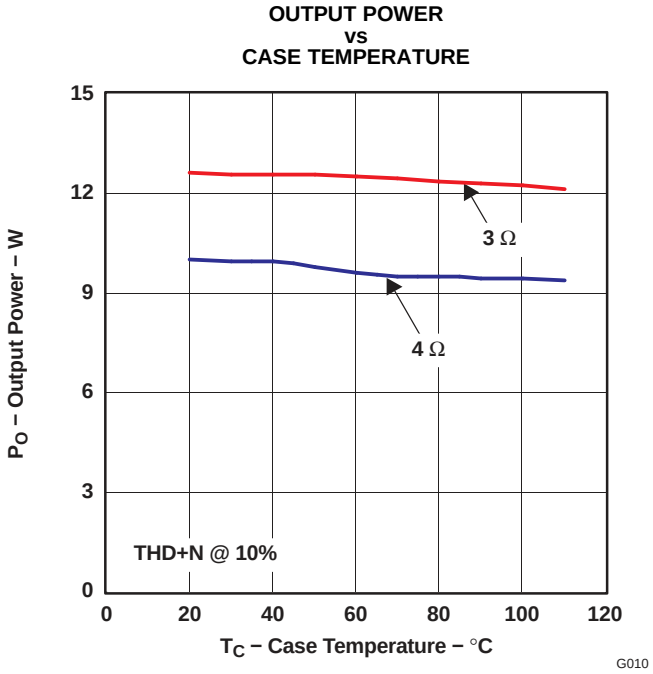


Figure 10.

TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

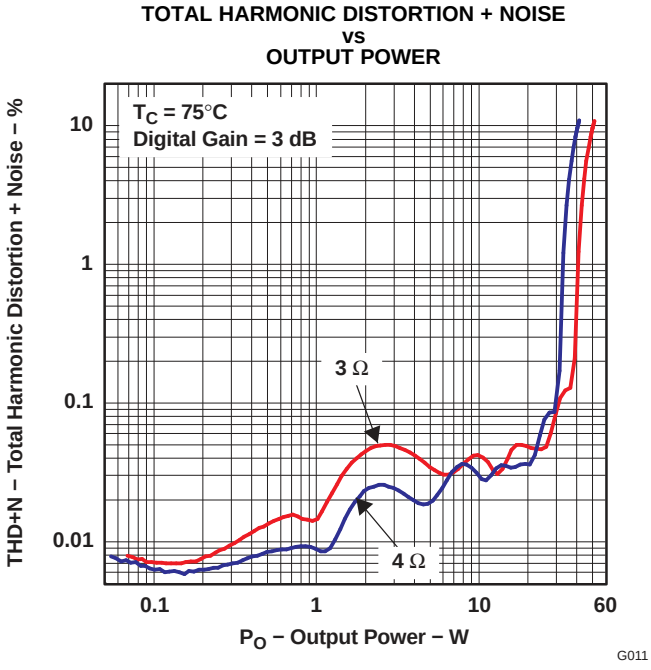


Figure 11.

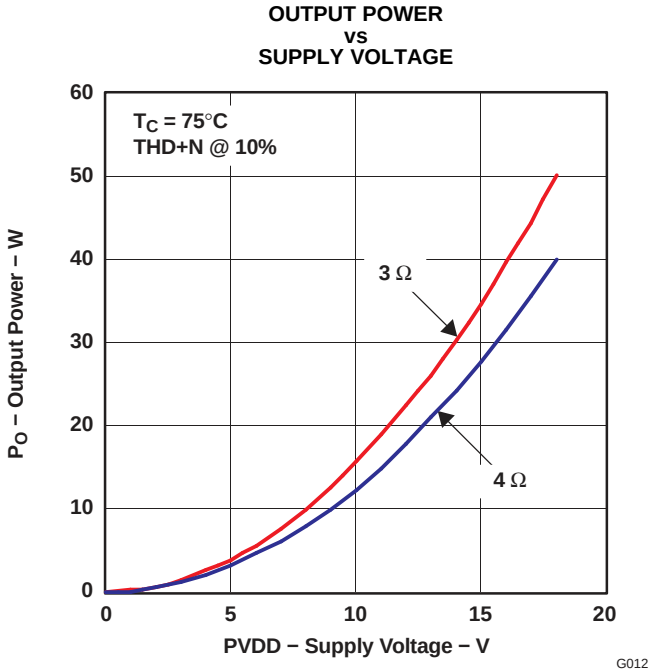


Figure 12.

TYPICAL CHARACTERISTICS, PBTL CONFIGURATION (continued)

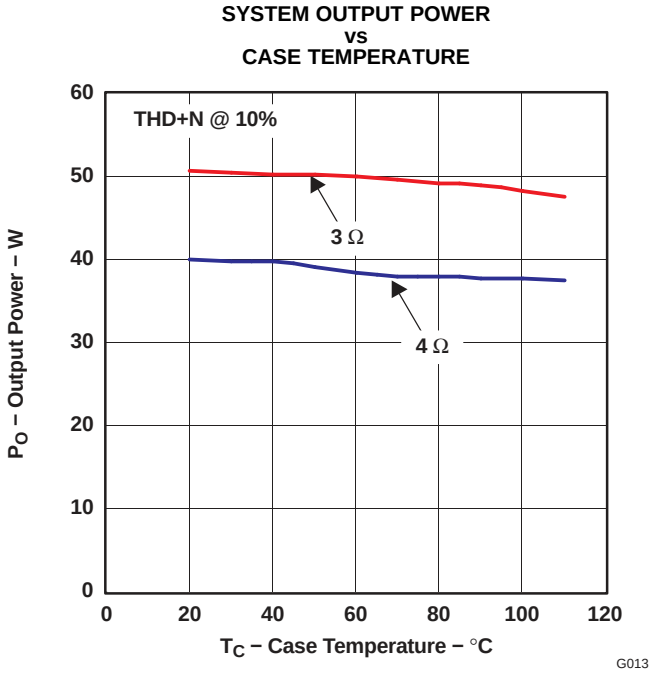
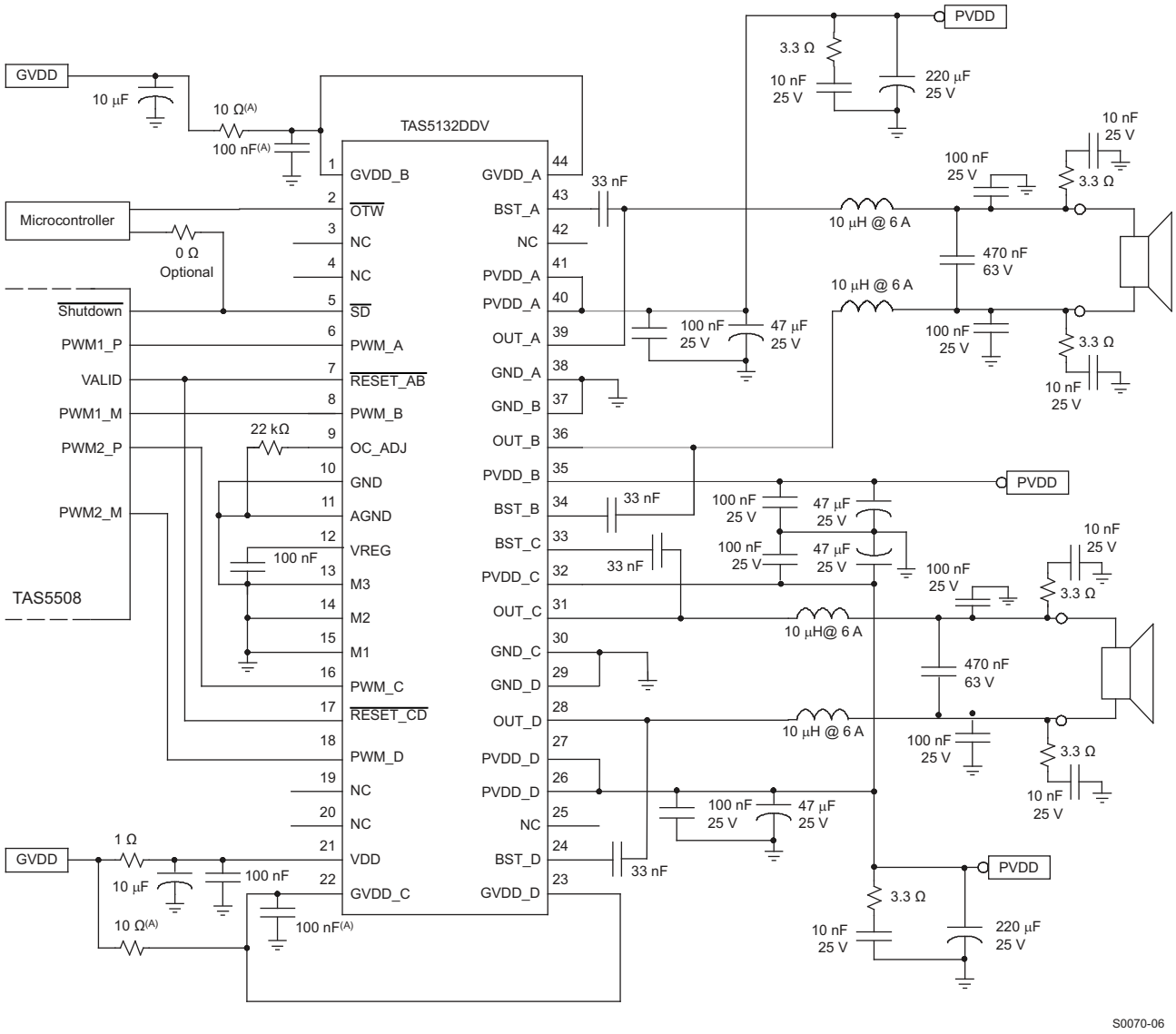
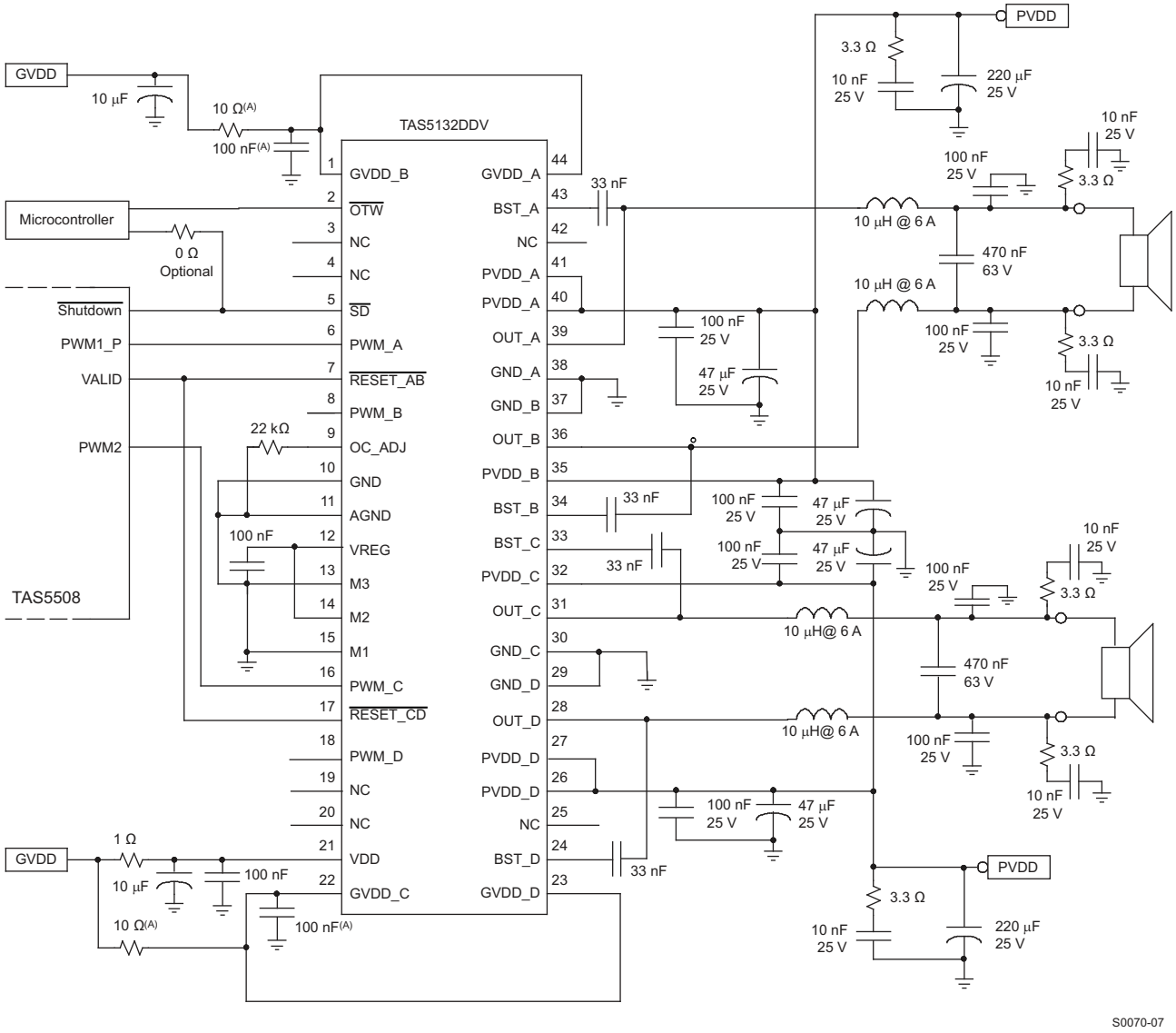


Figure 13.



A. Optional component, GVDD_A and GVDD_B can potentially share the same decoupling components. Also, GVDD_C and GVDD_D can potentially share the same decoupling components.

Figure 14. Typical Differential (2N) BTL Application With AD Modulation Filters



A. Optional component, GVDD_A and GVDD_B can potentially share the same decoupling components. Also, GVDD_C and GVDD_D can potentially share the same decoupling components.

Figure 15. Typical Non-Differential (1N) BTL Application With AD Modulation Filters

THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5132 needs only a 12-V supply in addition to the (typical) 18-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 192 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5132 reference design. For additional information on recommended power supply and required components, see the application diagrams given previously in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 18-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5132 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The TAS5132 does not require a power-up sequence. The outputs of the H-bridges remain in a low-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output. The output impedance is approximately 3KΩ under this condition, unless mode 1, 0, 0 (Single-ended Mode), is used. This means that the TAS5132 should be held in reset for at least 200 μS to ensure that the bootstrap capacitors are charged. This also assumes that the recommended 0.033-μF bootstrap capacitors are used. Changes to bootstrap capacitor values will change the bootstrap capacitor charge time.

When the TAS5132 is being used with TI PWM modulators such as the TAS5086, no special attention to the state of $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ is required, provided that the chipset is configured as recommended.

Powering Down

The TAS5132 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ low during power down, thus preventing audible artifacts, including pops or clicks.

When the TAS5132 is being used with TI PWM modulators such as the TAS5086, no special attention to the state of $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ is required, provided that the chipset is configured as recommended.

ERROR REPORTING

The $\overline{\text{SD}}$ and $\overline{\text{OTW}}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{SD}}$ pin going low. Likewise, $\overline{\text{OTW}}$ goes low when the device junction temperature exceeds 125°C (see the following table).

$\overline{\text{SD}}$	$\overline{\text{OTW}}$	DESCRIPTION
0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	1	Overload (OLP) or undervoltage (UVP)
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

Note that asserting either $\overline{\text{RESET\_AB}}$ or $\overline{\text{RESET\_CD}}$ low forces the $\overline{\text{SD}}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device, resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{\text{SD}}$ and $\overline{\text{OTW}}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5132 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5132 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{SD}}$ pin low. In situations other than overload and overtemperature, the device automatically recovers when the fault condition has been removed. For highest possible reliability, recovering from an overload fault requires external reset of the device (see the *Device Reset* section of this data sheet) no sooner than 1 second after the shutdown.

The TAS5132 contains circuitry associated with its PWM inputs that will detect the condition when a PWM input is continuously high or low. This function is named PWM Activity Detector (PAD). Without this protection circuitry, if a PWM input is continuously high or low, the PVDD power supply voltage could appear on the associated output pin. This condition could damage either the output load (loudspeaker) or the device. If a PWM input remains either high or low for over 10 µS, the device's outputs will be set into a Hi-Z state. If this error condition occurs, $\overline{\text{SD}}$ will not be asserted low.

Use of TAS5132 in High-Modulation-Index Capable Systems

This device requires at least 50 ns of low time on the output per 384-kHz PWM frame rate in order to keep the bootstrap capacitors charged. As an example, if the modulation index is set to 99.2% in the TAS5086, this setting allows PWM pulse durations down to 20 ns. This signal, which does not meet the 50-ns requirement, is sent to the PWM_X pin, and this low-state pulse time does not allow the bootstrap capacitor to stay charged. In this situation, the low voltage across the bootstrap capacitor can cause the bootstrap UVP circuitry to avtivate and shutdown the device. The TAS5132 device requires limiting the TAS5086 modulation index to 96.1% to keep the bootstrap capacitor charged under all signals and loads.

Therefore, TI strongly recommends using a TI PWM processor, such as TAS5508 or TAS5086, with the modulation index set at 96.1% to interface with TAS5132. This is done by writing 0x04 to the Modulation Limit Register (0x10) in the TAS5086 or 0x04 to the Modulation Limit Register (0x16) in the TAS5508.

Overcurrent (OC) Protection With Current Limiting and Overload Detection

The device has independent, fast-reacting current detectors with on all high-side and low-side power-stage FETs. See the following table for OC-adjust resistor values. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, i.e., it performs a current-limiting function, rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state.

Current limiting and overload protection are independent for half-bridges A and B and, respectively, C and D. That is, if the bridge-tied load between half-bridges A and B causes an overload fault, only half-bridges A and B are shut down.

OC-Adjust Resistor Values (kΩ)	Max. Current Before OC Occurs (A)
22	5.2
27	4.6
30	4.2
33	3.8
42	3.2
47	2.9
56	2.5
69.8	2.0

Overtemperature Protection

The TAS5132 has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW}$) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 155°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. OTE is latched in this case. To clear the OTE latch, both $\overline{RESET\_AB}$ and $\overline{RESET\_CD}$ must be asserted. Thereafter, the device resumes normal operation.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5132 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.6 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

Two reset pins are provided for independent control of half-bridges A/B and C/D. When $\overline{RESET\_AB}$ is asserted low, all four power-stage FETs in half-bridges A and B are forced into a high-impedance (Hi-Z) state. Likewise, asserting $\overline{RESET\_CD}$ low forces all four power-stage FETs in half-bridges C and D into a high-impedance state. Thus, both reset pins are well suited for hard-muting the power stage if needed.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset inputs low enables weak pulldown of the half-bridge outputs. In the SE mode, the weak pulldowns are not enabled, and it is therefore recommended to ensure bootstrap capacitor charging by providing a low pulse on the PWM inputs when reset is asserted high.

Asserting either reset input low removes any fault information to be signalled on the $\overline{SD}$ output, i.e., $\overline{SD}$ is forced high.

A rising-edge transition on either reset input allows the device to resume operation after an overload fault.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5132DDV	ACTIVE	HTSSOP	DDV	44	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5132	Samples
TAS5132DDVR	ACTIVE	HTSSOP	DDV	44	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5132	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

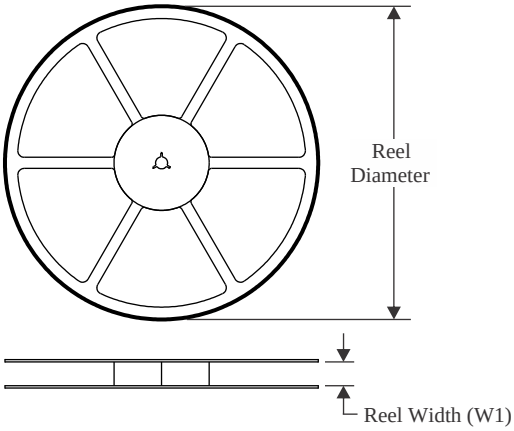
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

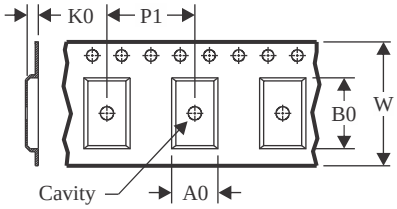
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

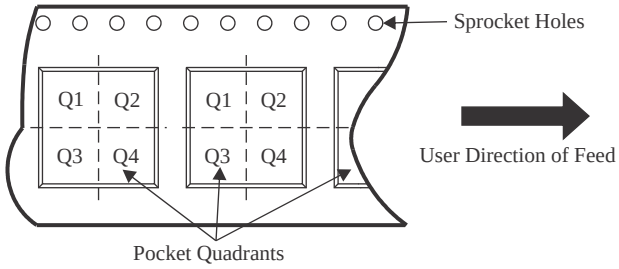


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

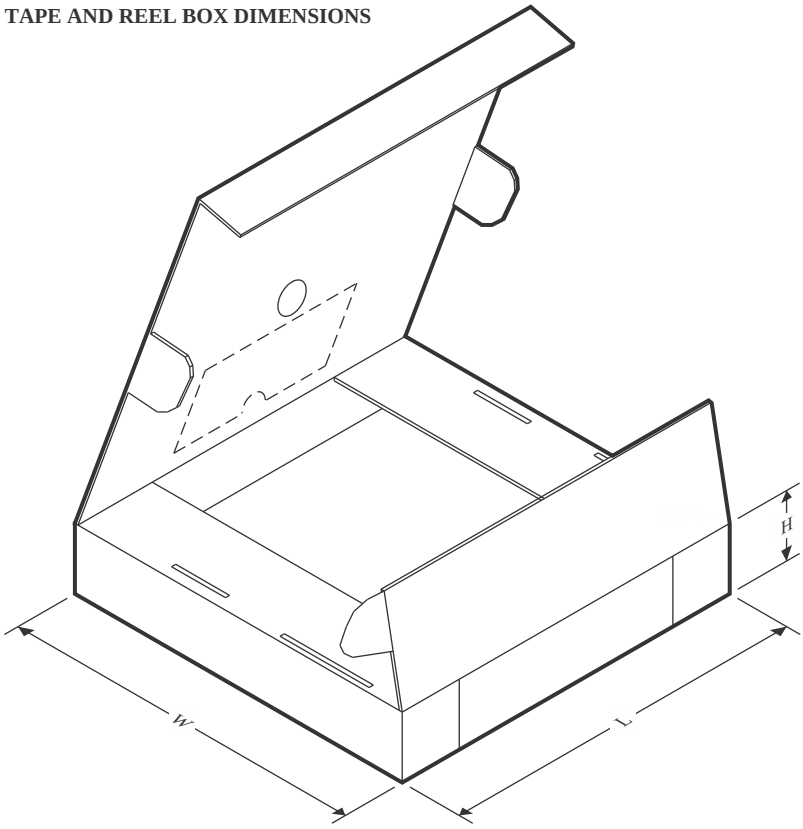
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5132DDVR	HTSSOP	DDV	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

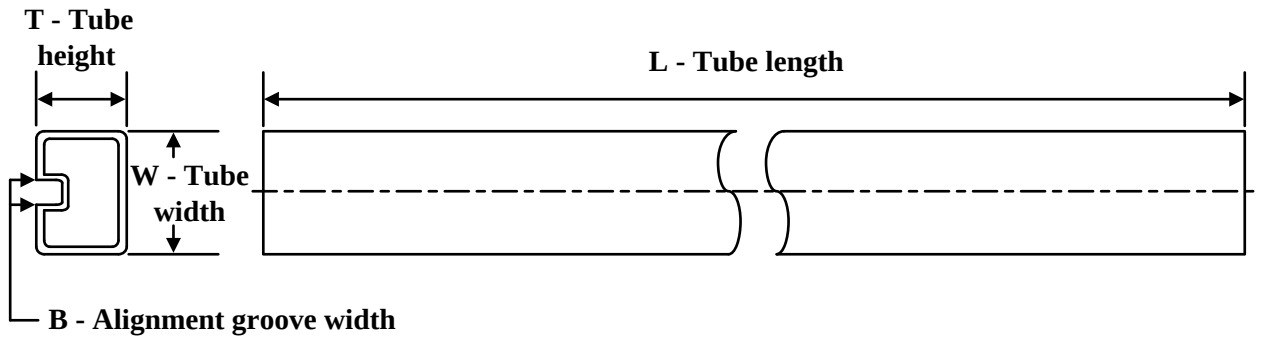
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5132DDVR	HTSSOP	DDV	44	2000	350.0	350.0	43.0

TUBE

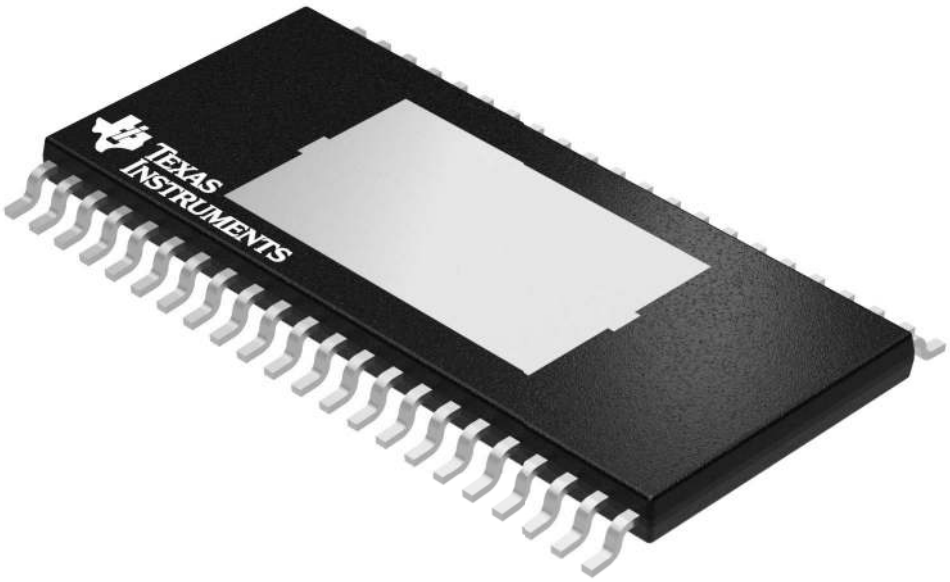


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5132DDV	DDV	HTSSOP	44	35	530	11.89	3600	4.9

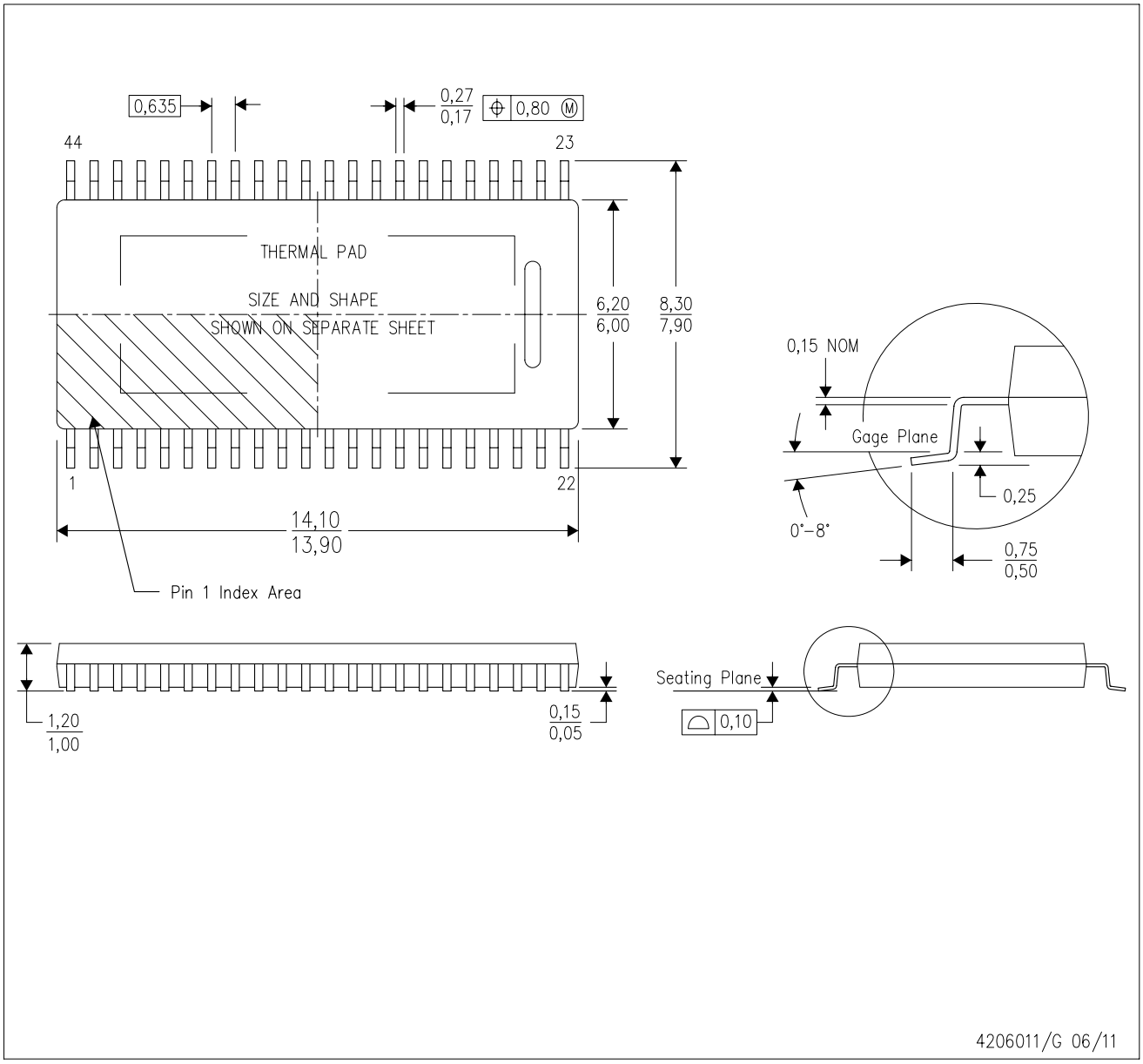
DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDV (R–PDSO–G44) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

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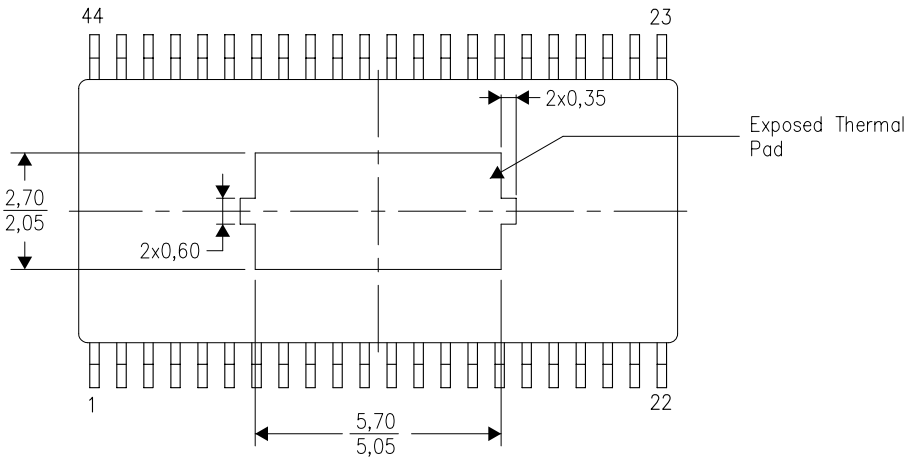
DDV (R–PDSO–G44) PowerPAD ™SMALL OUTLINE PACKAGE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206975–3/D 07/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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