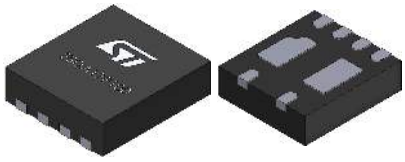
# ESDA17P100-1U2M

Datasheet

## High power transient voltage suppressor



**µQFN package**

## Features

- Low clamping voltage
- Peak pulse power: 4800 W (8/20 µs)
- Stand-off voltage 15 V
- Unidirectional diode
- Low leakage current: 0.2 µA at 25 °C
- Complies with IEC 61000-4-2 level 4
  - ±30 kV (air discharge)
  - ±30 kV (contact discharge)

## Applications

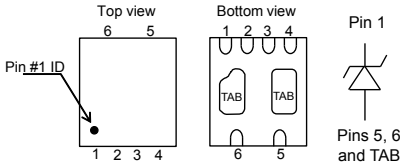
Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones, tablets, portable multimedia
- USB $V_{BUS}$ protection
- Power supply protection
- Battery protection

## Description

The ESDA17P100-1U2M is a unidirectional single line TVS diode designed to protect the power line against EOS and ESD transients.

The device is ideal for applications where high power TVS and board space saving is required.




| Pin | Name | Description |
|---|---|---|
| 1 | $V_{BUS}$ | $V_{BUS}$ pin |
| 2, 3, 4 | NC | Non connected pin |
| 5, 6 | GND | Ground pin |
| TAB | GND | Ground pin |

| Product status link |
|---|
| ESDA17P100-1U2M |

# 1 ESDA17P100-1U2M_Characteristics

**Table 1. Absolute maximum ratings ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{PP}$ | Peak pulse voltage | IEC 61000-4-2:<br>Contact discharge<br>Air discharge | <br>>30<br>>30 | kV |
| $P_{PP}$ | Peak pulse power | 8/20µs | 4800 | W |
| $I_{PP}$ | Peak pulse current | 8/20µs | 160 | A |
| $T_{stg}$ | Storage junction temperature range | | -55 to + 150 | °C |
| $T_{op}$ | Operating junction temperature range | | -55 to + 150 | °C |

**Figure 1. Electrical characteristics (definitions)**

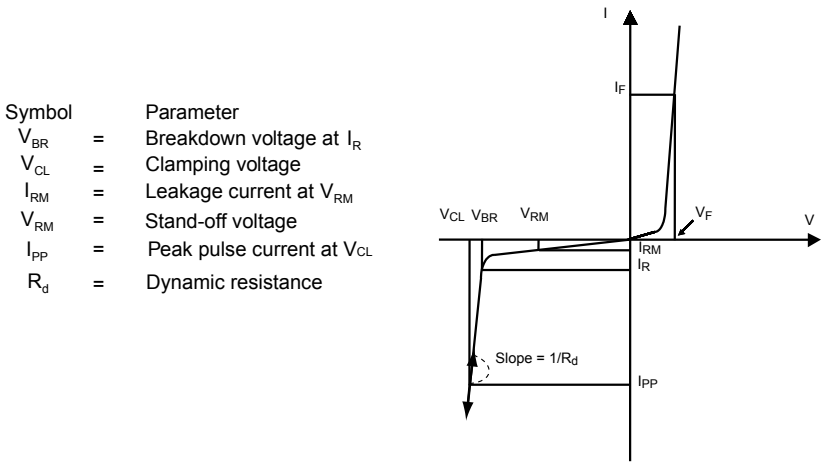



**Table 2. Electrical characteristics ($T_{amb}$ = 25 °C)**

| Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BR}$ | $I_R$ = 1 mA | 15.7 | 16.5 | 17.7 | V |
| $V_{RM}$ | | | | 15 | V |
| $I_{RM}$ | $V_{RM}$ = 12 V | | | 100 | nA |
| $I_{RM}$ | $V_{RM}$ = 15 V | | | 200 | nA |
| $R_d$ | 8/20 µs | | 0.07 | | Ω |
| $V_{CL}$ | $I_{PP}$ = 100 A, 8/20 µs | | 24 | 26 | V |
| $V_{CL}$ | $I_{PP}$ = 160 A, 8/20 µs | | 28 | 30 | V |
| $C_{BUS}$ | $V_{BUS}$ = 0 V, f = 1 MHz, $V_{OSC}$ = 30 mV | | 1200 | | pF |

## 1.1 Characteristics (curves)

**Figure 2. Peak power dissipation versus initial temperature (typical value)**

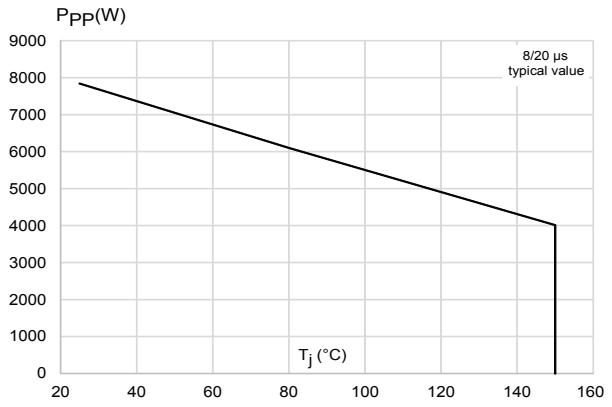



**Figure 3. Peak pulse power versus exponential pulse duration ($T_j$ = 25 °C, typical value)**

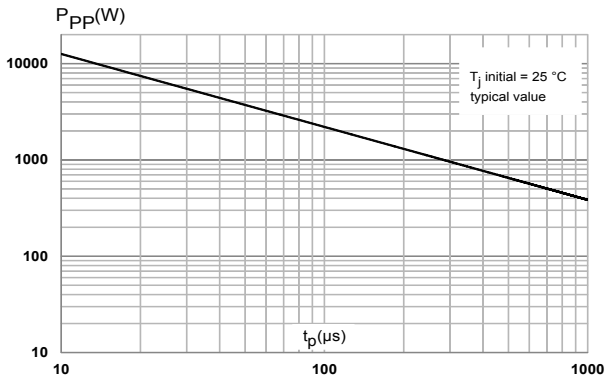



**Figure 4. Peak pulse current versus clamping voltage (max. value)**

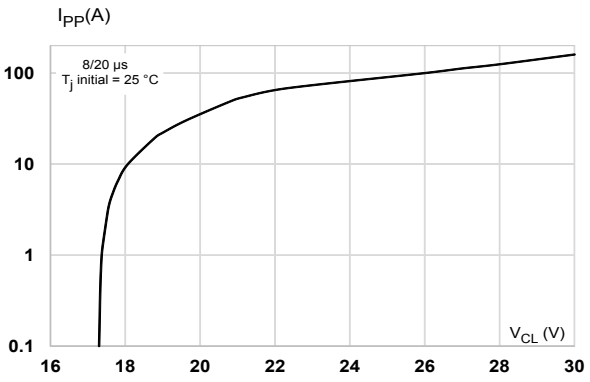



**Figure 5. Leakage current versus junction temperature (typical value)**

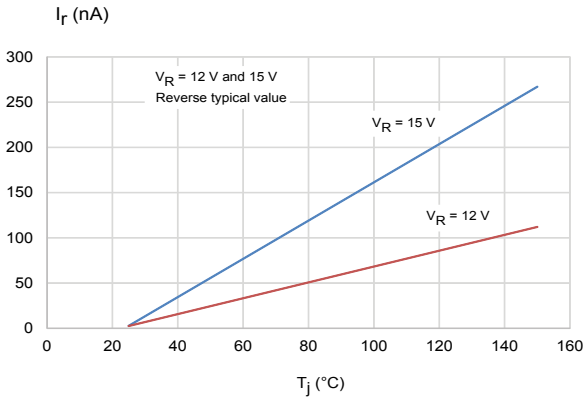



**Figure 6. ESD response to IEC 61000-4-2 (+8kV contact discharge)**

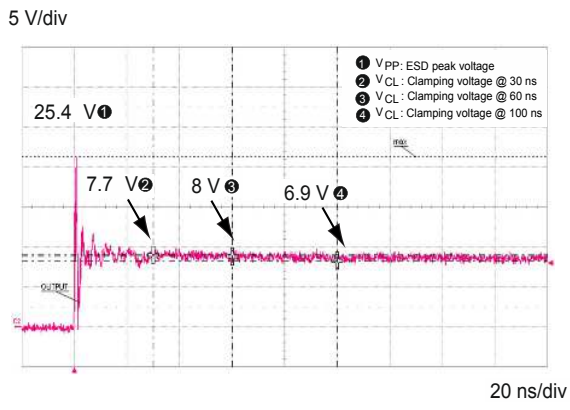
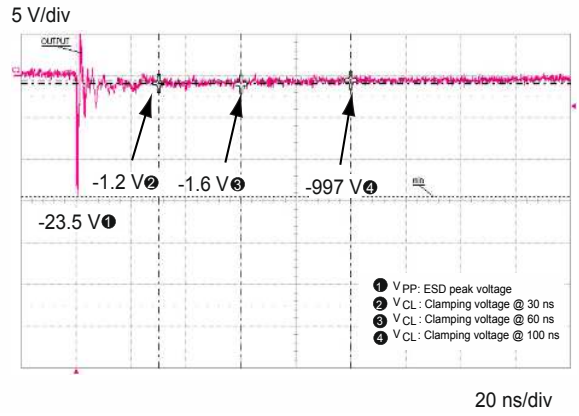



**Figure 7. ESD response to IEC 61000-4-2 (-8kV contact discharge)**



# 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 2.1 µQFN package information

**Figure 8. µQFN package outline**

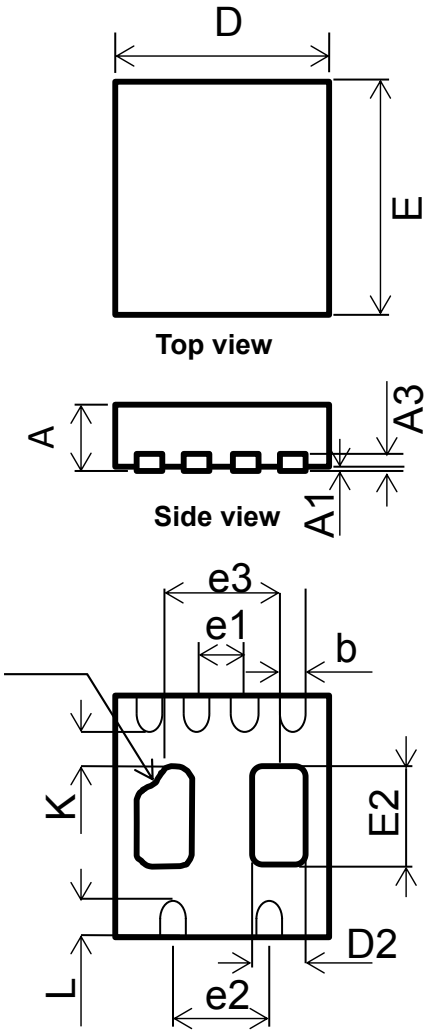


Table 3. **µQFN package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.51 | 0.55 | 0.60 | 0.0201 | 0.0217 | 0.0236 |
| A1 | 0.00 | 0.02 | 0.05 | 0.0000 | 0.0008 | 0.0020 |
| A3 | | 0.15 | | | | |
| b | 0.15 | 0.20 | 0.25 | 0.0059 | 0.0079 | 0.0098 |
| D | 1.70 | 1.80 | 1.90 | 0.0669 | 0.0709 | 0.0748 |
| E | 1.90 | 2.0 | 2.10 | 0.0748 | 0.0787 | 0.0827 |
| e1 | | 0.4 | | | 0.0157 | |
| e2 | | 0.80 | | | 0.0315 | |
| D2 | 0.30 | 0.45 | 0.55 | 0.0118 | 0.0177 | 0.0217 |
| E2 | 0.69 | 0.84 | 0.94 | 0.0272 | 0.0331 | 0.0370 |
| e3 | | 0.95 | | | 0.0374 | |
| k | | 0.28 | | | 0.0110 | |
| L | 0.20 | 0.30 | 0.40 | 0.0079 | 0.0118 | 0.0157 |
| N | | 6.00 | | | | |

Figure 9. **µQFN footprint**

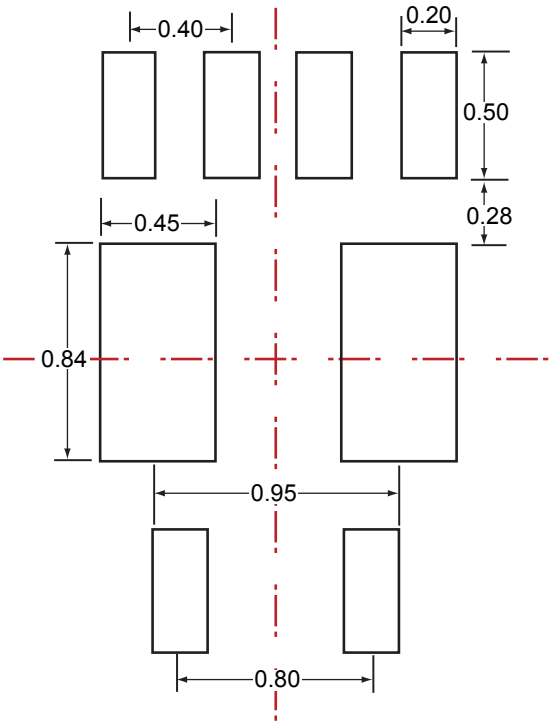


Figure 10. **Marking layout**

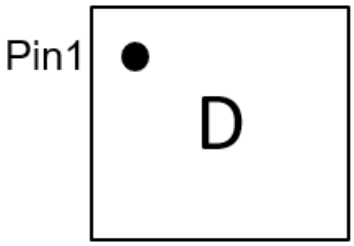



Figure 11. **Package orientation in reel**

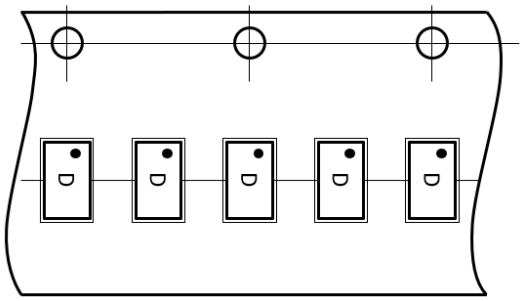



Figure 12. **Tape outline**

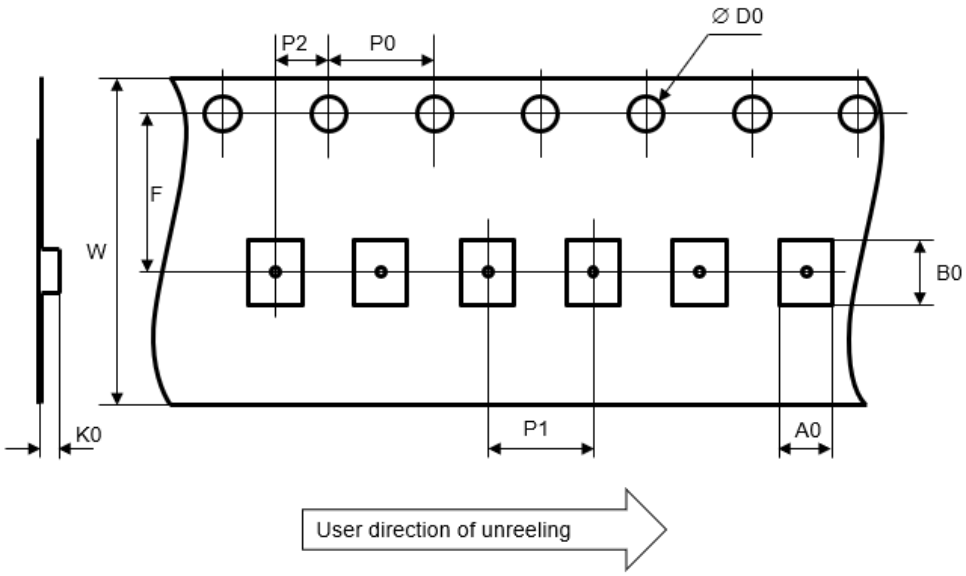



Table 4. **Tape and reel mechanical data**

| Ref. | Dimensions | | |
|---|---|---|---|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| A0 | 1.95 | 2.00 | 2.05 |
| B0 | 2.25 | 2.30 | 2.35 |
| D0 | 1.40 | 1.50 | 1.60 |
| F | 3.45 | 3.50 | 3.55 |
| K0 | 0.70 | 0.75 | 0.80 |
| P0 | 3.90 | 4.00 | 4.10 |
| P1 | 3.90 | 4.00 | 4.10 |
| P2 | 1.95 | 2.00 | 2.05 |
| W | 7.90 | 8.00 | 8.30 |

# 3 Recommendation on PCB assembly

## 3.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).
2. General design rule
   a. Stencil thickness (T) = 75 ~ 125 µm
   b. Aspect ratio =

$$\frac{W}{T} \geq 1.5 \quad (1)$$

   c. Aspect area =

$$\frac{L \times W}{2T(L + W)} \geq 0.66 \quad (2)$$

3. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for leads: Opening to footprint ratio is 90%.

**Figure 13. Stencil opening dimensions**

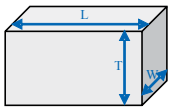
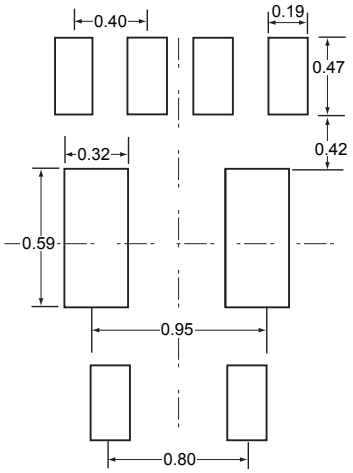



**Figure 14. Recommended stencil window position**




## 3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during PCB movement.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

## 3.3 Placement

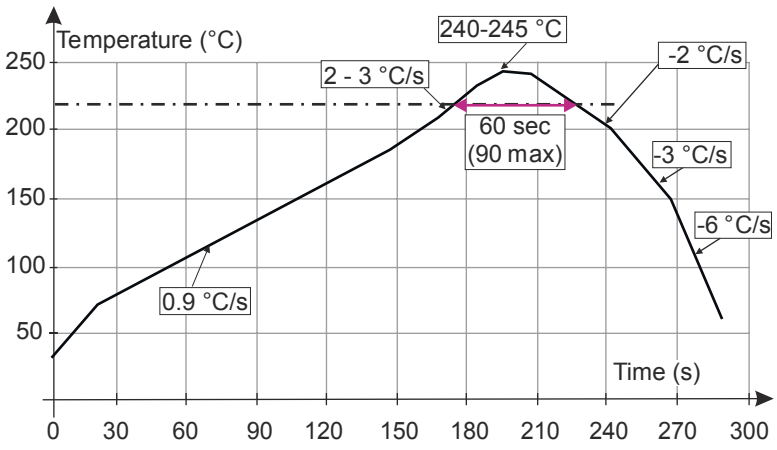
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick, and place and reflow soldering by using optimized tools.

## 3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

## 3.5 Reflow profile

**Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting**




*Note: Minimize air convection currents in the reflow oven to avoid component movement.*

# 4 ESDA17P100-1U2M_Ordering information

**Figure 16. Ordering information scheme**

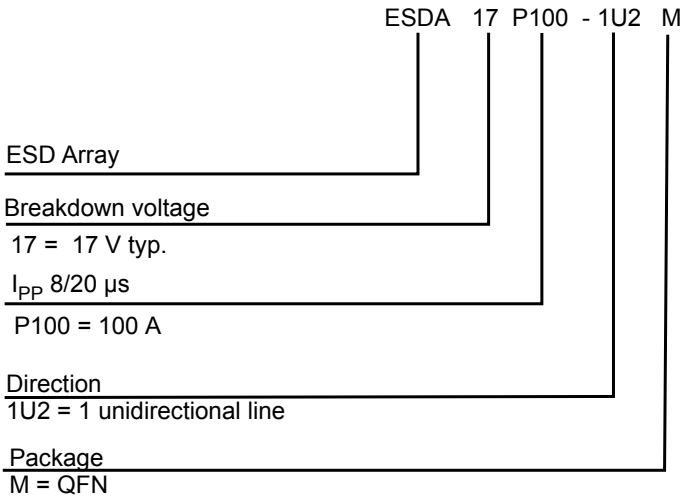



**Table 5. Ordering information**

| Order code | Marking(1) | Package | Weight | Base qty. | Delivery mode |
|---|---|---|---|---|---|
| ESDA17P100-1U2M | D | µQFN | 6 mg | 5000 | Tape and reel |

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

## Revision history

Table 6. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 14-Mar-2017 | 1 | Initial release. |
| 07-Feb-2023 | 2 | Updated package view, Figure 8 and Table 3. |

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