0.1 GHz to 18 GHz, GaAs SP4T Switch

Data Sheet **HMC641A**

FEATURES

- Broadband frequency range: 0.1 GHz to 18 GHz
- Nonreflective 50 Ω design
- Low insertion loss: 2.1 dB to 12 GHz
- High isolation: 42 dB to 12 GHz
- High input linearity
  - P1dB: 25 dBm typical at V_{SS} = −5 V
  - IP3: 41 dBm typical
- High power handling at V_{SS} = −5 V
  - 24 dBm through path
  - 23 dBm terminated path
- Integrated 2 to 4 line decoder
- 8-pad, 1.92 mm × 1.60 mm × 0.102 mm, CHIP

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, and electronic counter measures (ECMs)
- Broadband telecommunications systems

FUNCTIONAL BLOCK DIAGRAM

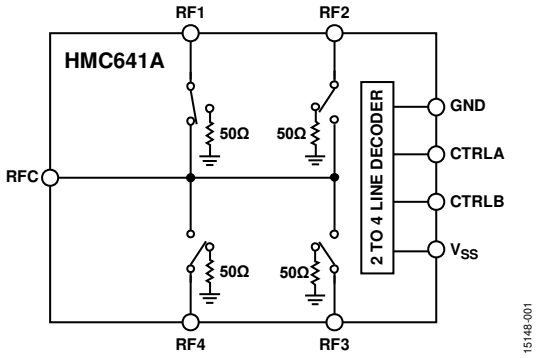

Figure 1.

GENERAL DESCRIPTION

The HMC641A is a nonreflective, single-pole, four-throw (SP4T) switch, manufactured using a gallium arsenide (GaAs) process. This switch typically provides low insertion loss of 2.1 dB and high isolation of 42 dB in broadband frequency range from 0.1 GHz to 18 GHz.

The HMC641A includes an on-chip, binary 2 to 4 line decoder that provides control from two logic input lines.

The switch operates with a negative supply voltage of −5 V to −3 V and requires two negative logic control voltages.

All electrical performance data is acquired with the HMC641A that all RFx pads are connected to by the 50 Ω transmission lines via one 3.0 mil × 0.5 mil ribbon bond of minimal length.

Rev. D

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REVISION HISTORY

10/2018—Rev. C to Rev. D

Updated Outline Dimensions 10

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

3/2017—Rev. 02.0316 to Rev. C

Updated Format ..... Universal
Changes to Features Section, Figure 1, and General Description Section 1
Changed V_{SS} = −5 V to V_{SS} = −5 V to −3 V, Table 1 3
Changes to Table 1 3
Deleted Bias Voltage & Current Table, TTL/CMOS Control Voltage Table, and Truth Table 3
Changes to Table 2 4
Added Power Derating Curve Section and Figure 2; Renumbered Sequentially 4
Added Figure 4 5
Deleted GND Interface Schematic Figure and TTL Interface Circuit Figure 5
Changes to Table 3 and Figure 5 5
Added Table 4; Renumbered Sequentially 8
Added Theory of Operation Section 8
Added Applications Information Section, Figure 14, Figure 15, and Assembly Diagram Section 9
Updated Outline Dimensions 10
Updated Ordering Guide 10

SPECIFICATIONS

V_{SS} = −5 V to −3 V, V_{CTL} = 0 V or V_{SS}, T_{DIE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BROADBAND FREQUENCY RANGE	f		0.1		18	GHz
INSERTION LOSS		0.1 GHz to 12 GHz		2.1	2.4	dB
		0.1 GHz to 18 GHz		2.3	3.0	dB
ISOLATION						
Between RFC and RF1 to RF4		0.1 GHz to 12 GHz	39	42		dB
		0.1 GHz to 18 GHz	36	38		dB
RETURN LOSS						
RFC		0.1 GHz to 18 GHz		15		dB
RF1 to RF4						
On State		0.1 GHz to 18 GHz		15		dB
Off State		0.1 GHz to 18 GHz		15		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		15		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		95		ns
INPUT LINEARITY[1]		250 MHz to 18 GHz				
1 dB Compression	P1dB	V_{SS} = −5 V	22	25		dBm
		V_{SS} = −3 V		22		dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing				
		V_{SS} = −5 V	38	41		dBm
		V_{SS} = −3 V		41		dBm
SUPPLY		V_{SS} pin				
Voltage	V_{SS}		−5		−3	V
Current	I_{SS}			1.9	6	mA
DIGITAL CONTROL INPUTS		CTRLA and CTRLB pins				
Voltage	V_{CTL}					
Low	V_{INL}	V_{SS} = −5 V	−3		0	V
		V_{SS} = −3 V	−1		0	V
High	V_{INH}	V_{SS} = −5 V	−5		−4.2	V
		V_{SS} = −3 V	−3		−2.2	V
Current	I_{CTL}					
Low	I_{INL}			50		µA
High	I_{INH}			0.2		µA

[1] Input linearity performance degrades at frequencies less than 250 MHz; see Figure 10, Figure 11, Figure 12, and Figure 13.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	−7 V
Digital Control Input Voltage	V_{SS} − 0.5 V to +1 V
RF Input Power[1] (f = 250 MHz to 18 GHz, T_{DIE} = 85°C)	
V_{SS} = −5 V	
Through Path	24 dBm
Terminated Path	23 dBm
Hot Switching	20 dBm
V_{SS} = −3 V	
Through Path	21 dBm
Terminated Path	20 dBm
Hot Switching	17 dBm
Temperature	
Junction Temperature, T_J	150°C
Die Bottom Temperature Range, T_{DIE}	−55°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction to Die Bottom Thermal Resistance	
Through Path	201°C/W
Terminated Path	322°C/W
ESD Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] For power derating at frequencies less than 250 MHz, see Figure 2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

POWER DERATING CURVE

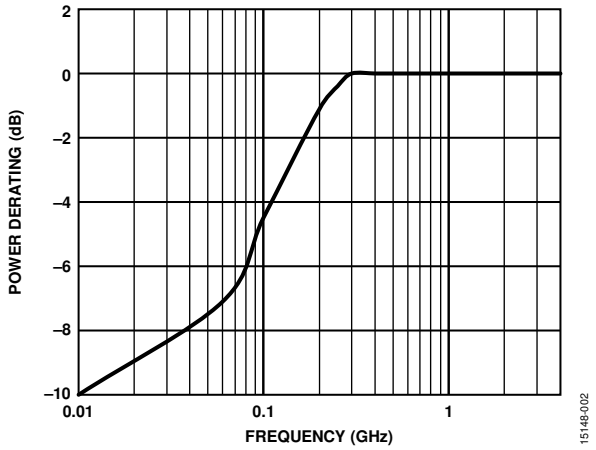

Figure 2. Power Derating at Frequencies Less Than 250 MHz

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

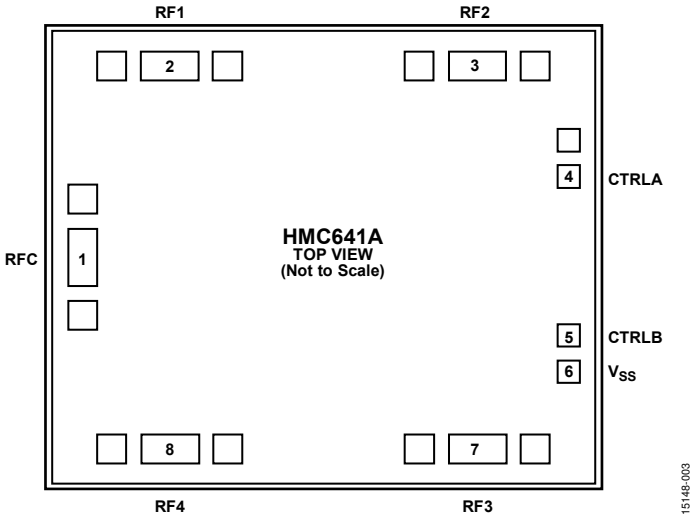

Figure 3. Pin Configuration

Table 3. Pad Function Descriptions[1]

Pad No.	Mnemonic	Description
1	RFC	RF Common Pad. This pad is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
2	RF1	RF Throw Pad 1. This pad is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
3	RF2	RF Throw Pad 2. This pad is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
4	CTRLA	Control Input A; see Table 4. See Figure 5 for the interface schematic.
5	CTRLB	Control Input B; see Table 4. See Figure 5 for the interface schematic.
6	V_{SS}	Negative Supply Voltage.
7	RF3	RF Throw Pad 3. This pad is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
8	RF4	RF Throw Pad 4. This pad is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
Die Bottom	GND	Ground. Die bottom must be attached directly to the ground plane eutectically or with conductive epoxy.

[1] No connection is required for the unlabeled grounds.

INTERFACE SCHEMATICS

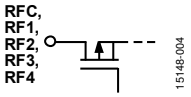

Figure 4. RFC to RF4 Interface Schematic

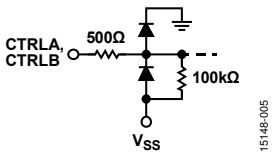

Figure 5. CTRLA and CTRLB Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

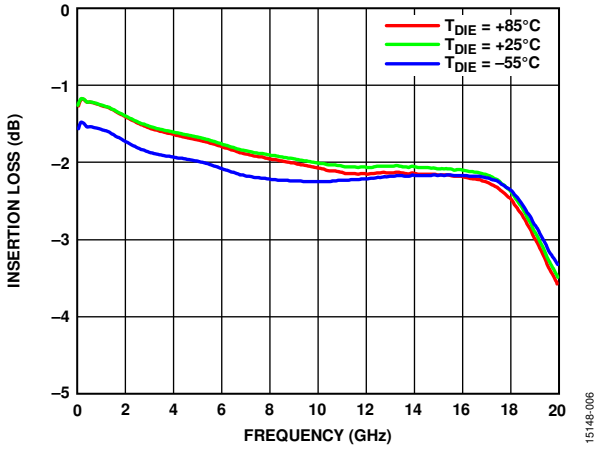

Figure 6. Insertion Loss Between RFC and RF1 vs. Frequency over Temperature

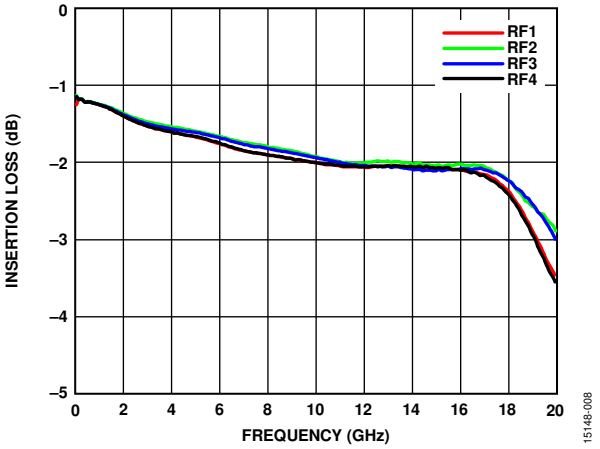

Figure 8. Insertion Loss Between RFC and RF1 to RF4 vs. Frequency

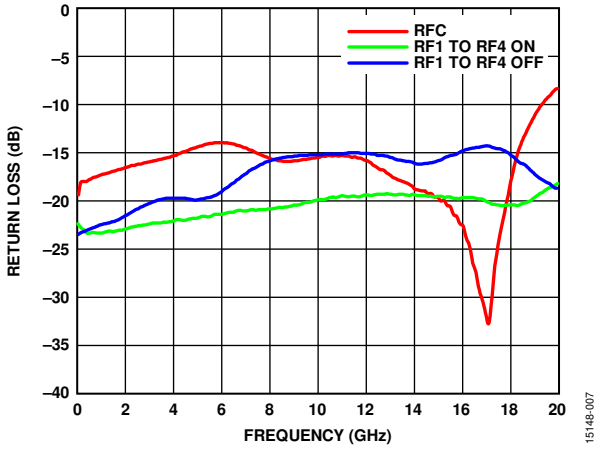

Figure 7. Return Loss for RFC, RF1 to RF4 On and RF1 to RF4 Off vs. Frequency

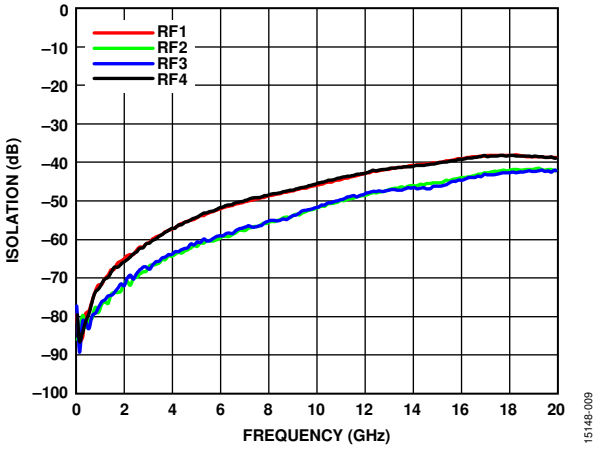

Figure 9. Isolation Between RFC and RF1 to RF4 vs. Frequency

INPUT POWER COMPRESSION (P1dB) AND THIRD-ORDER INTERCEPT (IP3)

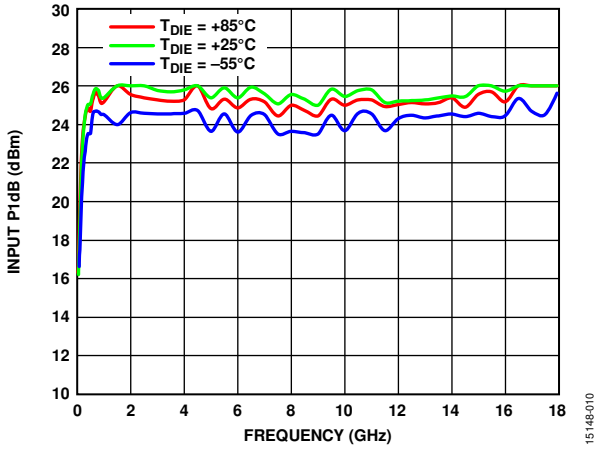

Figure 10. Input P1dB vs. Frequency over Temperature, V_{SS} = –5 V

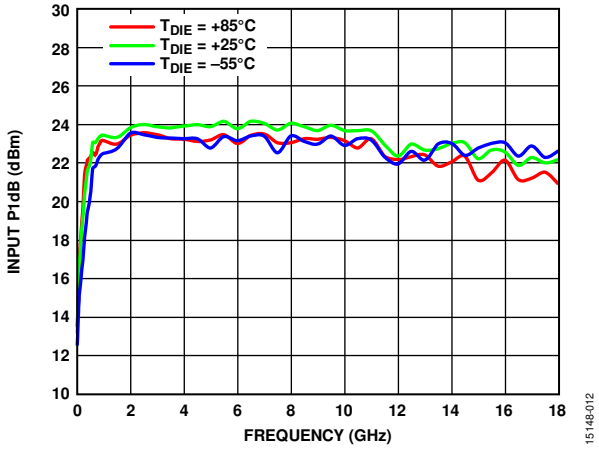

Figure 12. Input P1dB vs. Frequency over Temperature, V_{SS} = –3 V

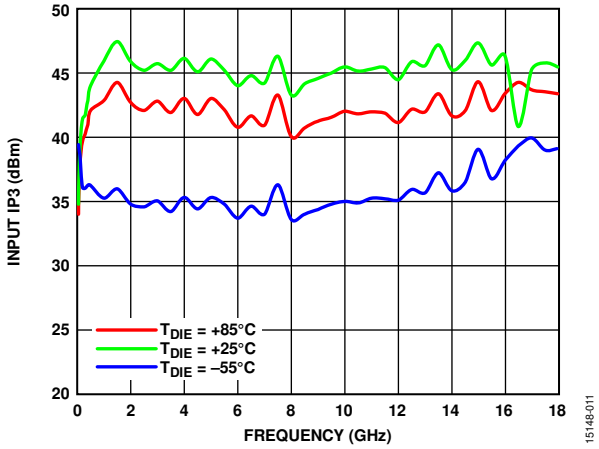

Figure 11. Input IP3 vs. Frequency over Temperature, V_{SS} = –5 V

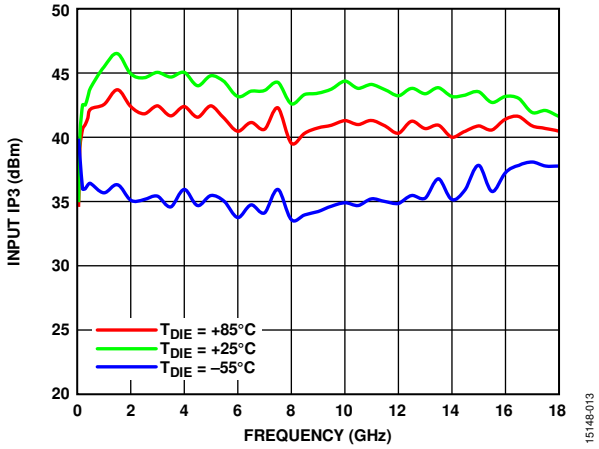

Figure 13. Input IP3 vs. Frequency over Temperature, V_{SS} = –3 V

THEORY OF OPERATION

The HMC641A requires a negative supply voltage at the V_{SS} pad and two logic control inputs at the CTRLA and CTRLB pads to control the state of the RF paths.

Depending on the logic level applied to the CTRLA and CTRLB pads, one RF path is in the insertion loss state while the other three paths are in an isolation state (see Table 4). The insertion loss path conducts the RF signal between the RF throw pad and RF common pad while the isolation paths provide high loss between RF throw pads terminated to internal 50 Ω resistors and the insertion loss path.

The ideal power-up sequence is as follows:

1. Ground to the die bottom.
2. Power up V_{SS}.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the V_{SS} supply can inadvertently become forward-biased and damage the internal electrostatic discharge (ESD) protection structures.
4. Apply an RF input signal. The design is bidirectional; the RF input signal can be applied to the RFC pad while the RF throw pads are the outputs or the RF input signal can be applied to the RF throw pads while the RFC pad is the output. All of the RF pads are dc-coupled to 0 V, and no dc blocking is required at the RF pads when the RF line potential is equal to 0 V.

The power-down sequence is the reverse of the power-up sequence.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths			
CTRLA	**CTRLB**	**RF1 to RFC**	**RF2 to RFC**	**RF3 to RFC**	**RF4 to RFC**
High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

MOUNTING AND BONDING TECHNIQUES

The HMC641A is back metallized and must be attached directly to the ground plane with gold tin (AuSn) eutectic preforms or with electrically conductive epoxy.

The die thickness is 0.102 mm (4 mil). The 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the HMC641A (see Figure 14).

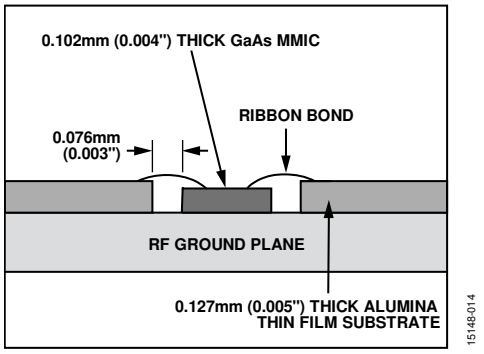

Figure 14. Bonding RF Pads to 5 mil Substrate

When using 0.254 mm (10 mil) thick alumina thin film substrates, the HMC641A must be raised 0.150 mm (6 mil) so the surface of the HMC641A is coplanar with the surface of the substrate. One way to accomplish this is by attaching the 0.102 mm (4 mil) thick die to a 0.150 mm (6 mil) thick molybdenum heat spreader (moly tab), which is then attached to the ground plane (see Figure 15).

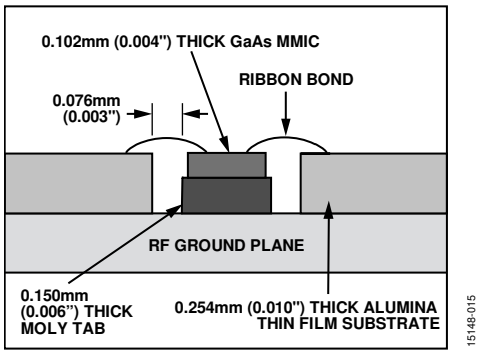

Figure 15. Bonding RF Pads to 10 mil Substrate

Microstrip substrates are placed as close to the HMC641A as possible to minimize bond length. Typical die to substrate spacing is 0.076 mm (3 mil).

RF bonds made with 3 mil × 5 mil ribbon are recommended. DC bonds made with 1 mil diameter wire are recommended. All bonds must be as short as possible.

ASSEMBLY DIAGRAM

An assembly diagram of the HMC641A is shown in Figure 16.

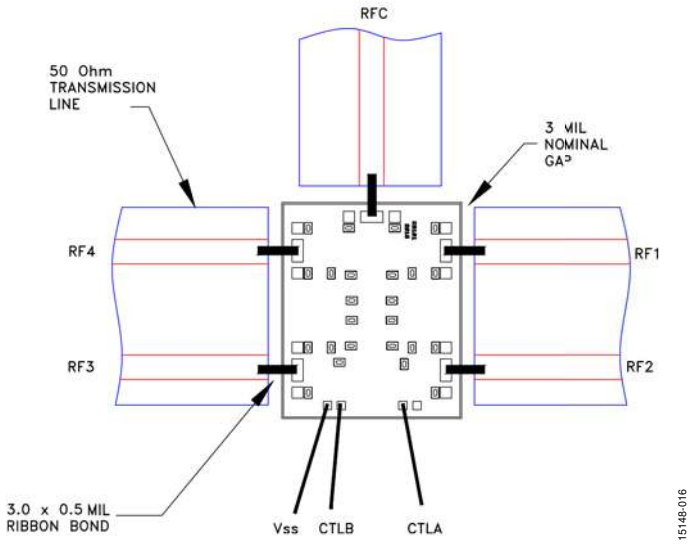

Figure 16. Die Assembly Diagram

OUTLINE DIMENSIONS

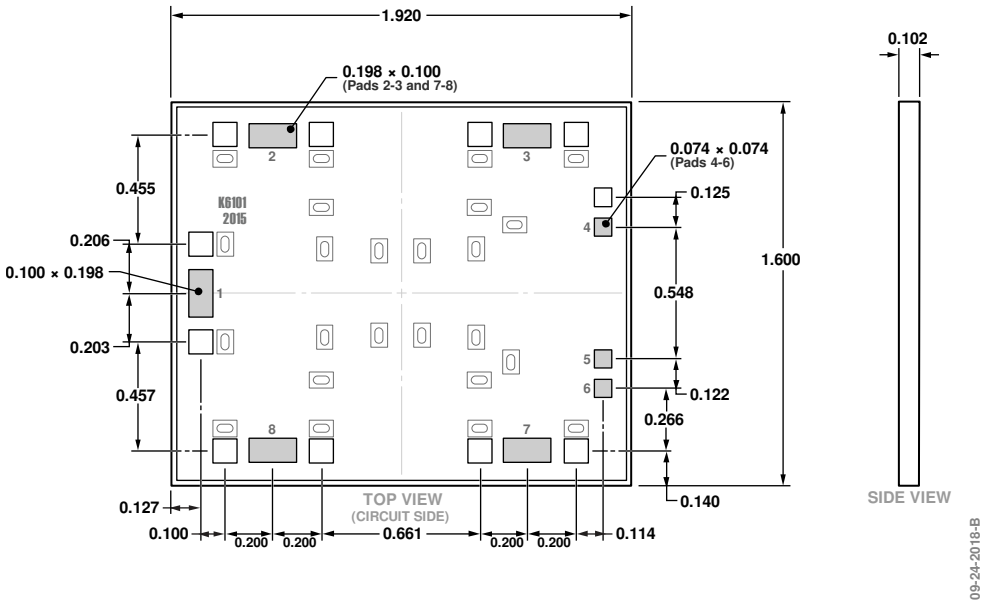

Figure 17. 8-Pad Bare Die [CHIP]
(C-8-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
HMC641A	−55°C to +85°C	8-Pad Bare Die [CHIP]	C-8-9
HMC641A-SX	−55°C to +85°C	8-Pad Bare Die [CHIP]	C-8-9

[1] The HMC641A is a RoHS compliant part.
[2] The HMC641A-SX is a sample order model.