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National Semiconductor

April 2005

DS92LV1023
40-66 MHz 10 Bit Bus LVDS Serializer

General Description

The DS92LV1023 is a 400 to 660 Mb/s serializer for high-speed unidirectional serial data transmission over FR-4 printed circuit board backplanes and balanced copper cables. It transforms a 10-bit wide parallel LVCMOS/LVTTL data bus into a single high speed Bus LVDS serial data stream with embedded clock. This single serial data stream simplifies PCB design and reduces PCB cost by narrowing data paths that in turn reduce PCB size and number of layers. The single serial data stream also reduces cable size, the number of connectors, and eliminates clock-to-data and data-to-data skew.

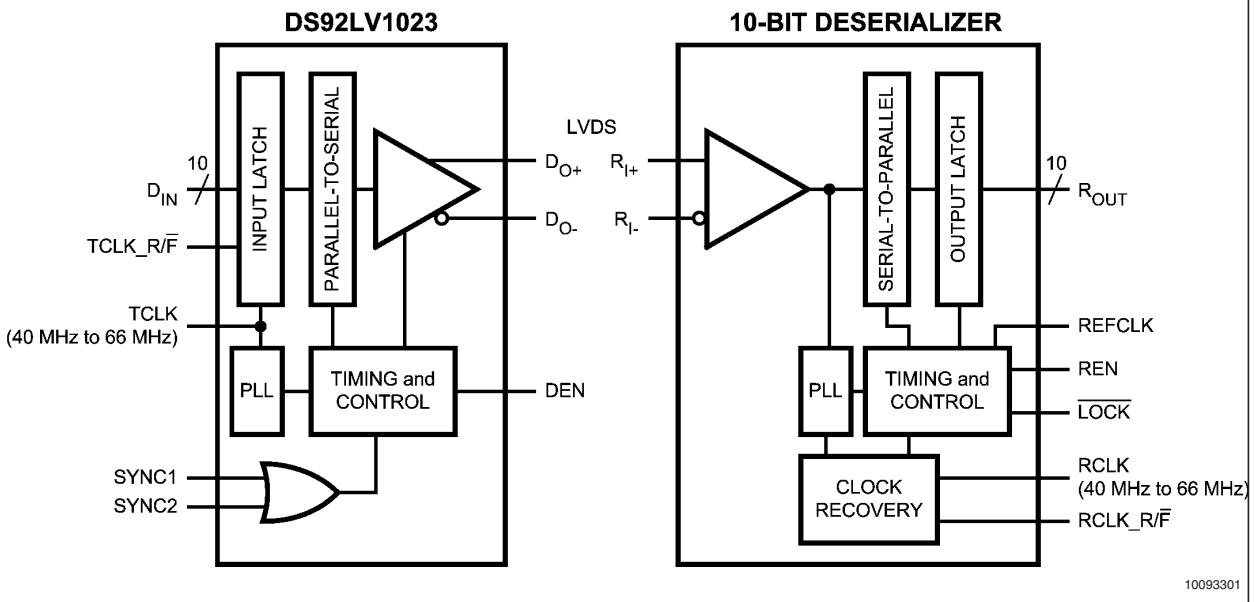
The DS92LV1023 works well with any National Semiconductor's Bus LVDS 10–bit deserializer within its specified frequency operating range. It features low power consumption, pin selectable edge trigger on clock, and high impedance outputs in power down mode.

The DS92LV1023 was designed with the flow-through pinout and is available in a space saving 28–lead SSOP package.

Features

- 40–66 MHz Single 10:1 Serializer with 400–660 Mb/s throughput
- Robust Bus LVDS serial data transmission with embedded clock for exceptional noise immunity and low EMI
- Guaranteed transition every data transfer cycle
- Low power consumption < 250 mW (typ) @ 66 MHz
- Single differential pair eliminates multichannel skew
- Flow-through pinout for easy PCB layout
- Programmable edge trigger on clock
- High impedance on driver outputs when power is off
- Bus LVDS serial output rated for 27Ω load
- Small 28-lead SSOP package

Block Diagrams



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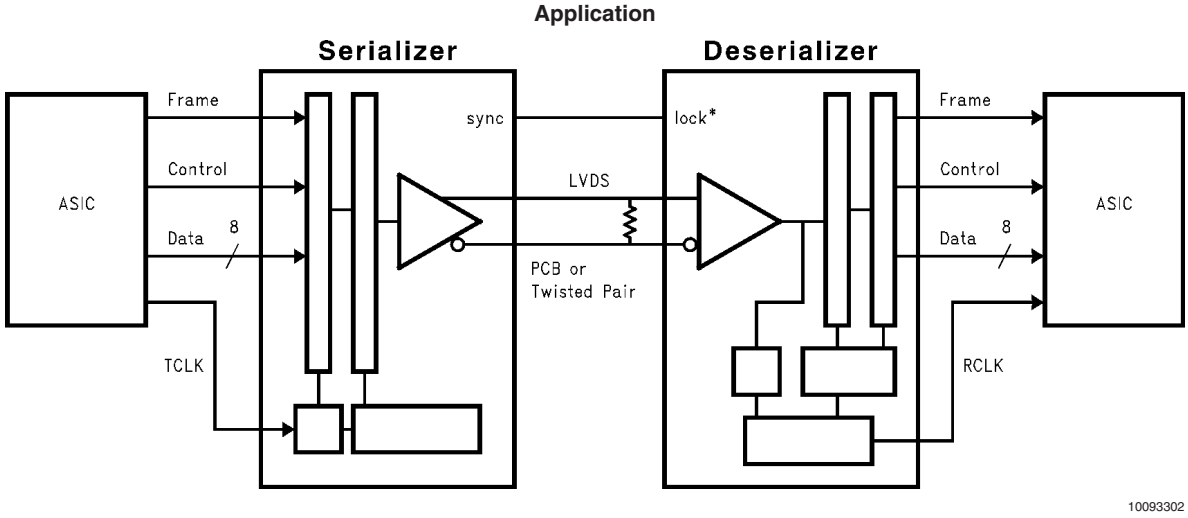
Block Diagrams (Continued)



Functional Description

The DS92LV1023 is a 10-bit Serializer device which together with a compatible deserializer (i.e. DS92LV1224) forms a chipset designed to transmit data over FR-4 printed circuit board backplanes and balanced copper cables at clock speeds from 40 to 66 MHz.

The chipset has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE®.

The following sections describe each operation and passive state.

Initialization

Initialization of both devices must occur before data transmission begins. Initialization refers to synchronization of the Serializer and Deserializer PLL's to local clocks, which may be the same or separate. Afterwards, synchronization of the Deserializer to Serializer occurs.

Step 1: When you apply V_{CC} to both Serializer and/or Deserializer, the respective outputs enter TRI-STATE®, and on-chip power-on circuitry disables internal circuitry. When V_{CC} reaches V_{CC}OK (2.5V) the PLL in each device begins locking to a local clock. For the Serializer, the local clock is the transmit clock (TCLK) provided by the source ASIC or other device. For the Deserializer, you must apply a local clock to the REFCLK pin.

The Serializer outputs remain in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer is now ready to send data or SYNC patterns, depending on the levels of the SYNC1 and SYNC2 inputs or a data stream. The SYNC pattern sent by the Serializer consists of six ones and six zeros switching at the input clock rate.

Note that the Deserializer $\overline{\text{LOCK}}$ output will remain high while its PLL locks to the incoming data or to SYNC patterns on the input.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete initialization. The Deserializer will lock to non-repetitive data patterns. However, the transmission of SYNC patterns enables the Deserializer to lock to the Serializer signal within a specified time. See *Figure 7*.

The user's application determines control of the SYNC1 and SYNC 2 pins. One recommendation is a direct feedback loop from the $\overline{\text{LOCK}}$ pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

When the Deserializer detects edge transitions at the Bus LVDS input, it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the $\overline{\text{LOCK}}$ output will go low. When $\overline{\text{LOCK}}$ is low, the Deserializer outputs represent incoming Bus LVDS data.

Data Transfer

After initialization, the Serializer will accept data from inputs DIN0–DIN9. The Serializer uses the TCLK input to latch incoming Data. The TCLK_R/$\overline{\text{F}}$ pin selects which edge the Serializer uses to strobe incoming data. TCLK_R/$\overline{\text{F}}$ high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for 5*TCLK cycles, the data at DIN0-DIN9 is ignored regardless of clock edge.

After determining which clock edge to use, a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The Serializer transmits serialized data and clock bits (10+2 bits) from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 66 MHz, the serial rate is 66 x 12 = 792 Mega-bits-per-second. Since only 10 bits are from input data, the serial "payload" rate is 10 times the TCLK frequency. For instance, if TCLK = 66 MHz, the payload data rate is 66 x 10 = 660 Mbps. The data source provides TCLK and must be in the range of 40 MHz to 66 MHz nominal.

The Serializer outputs (DO±) can drive a point-to-point connection or in limited multi-point or multi-drop backplanes. The outputs transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$ = high, and SYNC1 and SYNC2 are low. When DEN is driven low, the Serializer output pins will enter TRI-STATE.

When the Deserializer synchronizes to the Serializer, the $\overline{\text{LOCK}}$ pin is low. The Deserializer locks to the embedded

Data Transfer (Continued)

clock and uses it to recover the serialized data. ROUT data is valid when LOCK is low. Otherwise ROUT0–ROUT9 is invalid.

The ROUT0-ROUT9 pins use the RCLK pin as the reference to data. The polarity of the RCLK edge is controlled by the RCLK_R/F input.

ROUT(0-9), LOCK and RCLK outputs will drive a maximum of three CMOS input gates (15 pF load) with a 66 MHz clock.

Resynchronization

When the Deserializer PLL locks to the embedded clock edge, the Deserializer LOCK pin asserts a low. If the Deserializer loses lock, the LOCK pin output will go high and the outputs (including RCLK) will enter TRI-STATE.

The user's system monitors the LOCK pin to detect a loss of synchronization. Upon detection, the system can arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. Multiple resynchronization approaches are possible. One recommendation is to provide a feedback loop using the LOCK pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for multiple control in a multi-drop application. Sending sync patterns for resynchronization is desirable when lock times within a specific time are critical. However, the Deserializer can lock to random data, which is discussed in the next section.

Random Lock Initialization and Resynchronization

The initialization and resynchronization methods described in their respective sections are the fastest ways to establish the link between the Serializer and Deserializer. However, the DS92LV1224 can attain lock to a data stream without requiring the Serializer to send special SYNC patterns. This allows the DS92LV1224 to operate in "open-loop" applications. Equally important is the Deserializer's ability to support hot insertion into a running backplane. In the open loop or hot insertion case, we assume the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. The primary constraint on the "random" lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. As described in the next paragraph, the data contained in the data stream can also affect lock time.

If a specific pattern is repetitive, the Deserializer could enter "false lock" - falsely recognizing the data pattern as the clocking bits. We refer to such a pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes place in a clock cycle over multiple cycles. This occurs when any bit, except DIN 9, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. In the worst case, the Deserializer could become locked to the data pattern rather than the clock. Circuitry within the DS92LV1224 can detect that the possibility of "false lock" exists. The circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the LOCK output from becoming active until the potential "false lock" pattern changes. The false lock detect circuitry expects the data will eventually change, causing the Deserializer to lose lock to the data pattern and then continue searching for clock bits in the serial data stream. Graphical representations of RMT are shown in *Figure 1*. Please note that RMT only applies to bits DIN0-DIN8.

Powerdown

When no data transfer occurs, you can use the Powerdown state. The Serializer and Deserializer use the Powerdown state, a low power sleep mode, to reduce power consumption. The Deserializer enters Powerdown when you drive PWRDN and REN low. The Serializer enters Powerdown when you drive PWRDN low. In Powerdown, the PLL stops and the outputs enterTRI-STATE, which disables load current and reduces supply current to the milliampere range. To exit Powerdown, you must drive the PWRDN pin high.

Before valid data exchanges between the Serializer and Deserializer, you must reinitialize and resynchronize the devices to each other. Initialization of the Serializer takes 510 TCLK cycles. The Deserializer will initialize and assert LOCK high until lock to the Bus LVDS clock occurs.

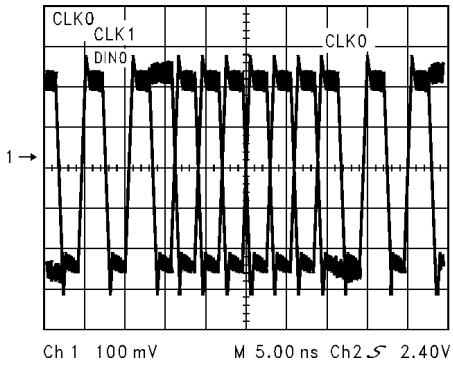
TRI-STATE

The Serializer enters TRI-STATE when the DEN pin is driven low. This puts both driver output pins (DO+ and DO–) into TRI-STATE. When you drive DEN high, the Serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2, PWRDN, TCLK_R/F).

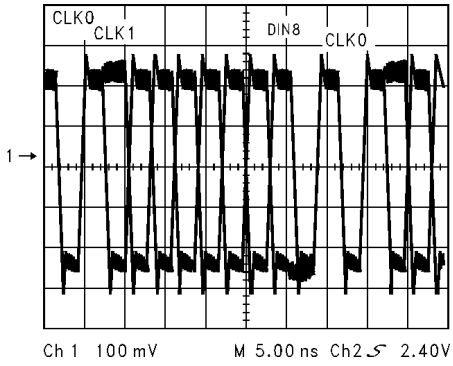
When you drive the REN pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT9) and RCLK will enter TRI-STATE. The LOCK output remains active, reflecting the state of the PLL.

Ordering Information

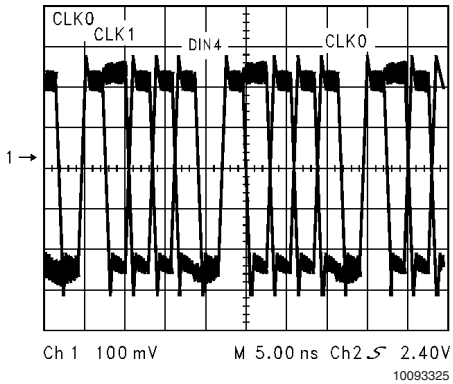
NSID	Function	Package
DS92LV1023TMSA	Serializer	MSA28



DIN0 Held Low-DIN1 Held High Creates an RMT Pattern



DIN8 Held Low-DIN9 Held High Creates an RMT Pattern



DIN4 Held Low-DIN5 Held High Creates an RMT Pattern

FIGURE 1. RMT Patterns Seen on the Bus LVDS Serial Output

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage	−0.3V to (V_{CC} +0.3V)
LVCMOS/LVTTL Output Voltage	−0.3V to (V_{CC} +0.3V)
Bus LVDS Driver Output Voltage	−0.3V to +3.9V
Bus LVDS Output Short Circuit Duration	10mS
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 seconds)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C Package:	
28L SSOP	1.27 W
Package Derating:	
	10.3 mW/˚C above
28L SSOP	+25˚C
θ_{ja}	97˚C/W
θ_{jc}	27˚C/W
ESD Rating	
HBM (1.5kOhm, 100pF)	>1kV
MM	> 250V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	˚C
Supply Noise Voltage (V_{CC})			100 mV_{P-P}	

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
SERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS (apply to DIN0-9, TCLK, $\overline{PWRDN}$, TCLK_R/$\overline{F}$, SYNC1, SYNC2, DEN)							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			-0.86	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V		−10	±1	+10	µA
SERIALIZER Bus LVDS DC SPECIFICATIONS (apply to pins DO+ and DO−)							
V_{OD}	Output Differential Voltage (DO+)−(DO−)	RL = 27Ω, *Figure 10*		200	290		mV
ΔV_{OD}	Output Differential Voltage Unbalance					35	mV
V_{OS}	Offset Voltage			1.05	1.1	1.3	V
ΔV_{OS}	Offset Voltage Unbalance				4.8	35	mV
I_{OS}	Output Short Circuit Current	D0 = 0V, DIN = High, $\overline{PWRDN}$ and DEN = 2.4V			−56	−90	mA
I_{OZ}	TRI-STATE Output Current	$\overline{PWRDN}$ or DEN = 0.8V, DO = 0V or VCC		−10	±1	+10	µA
I_{OX}	Power-Off Output Current	VCC = 0V, DO=0V or 3.6V		−20	±1	+25	µA
SERIALIZER SUPPLY CURRENT (apply to pins DVCC and AVCC)							
I_{CCD}	Serializer Supply Current	RL = 27Ω	f = 40 MHz		47	60	mA
	Worst Case	*Figure 2*	f = 66 MHz		75	90	mA
I_{CCXD}	Serializer Supply Current Powerdown	$\overline{PWRDN}$ = 0.8V			47	500	µA

Serializer Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period		15.15	T	25.0	nS
t_{TCIH}	Transmit Clock High Time		0.4T	0.5T	0.6T	nS
t_{TCIL}	Transmit Clock Low Time		0.4T	0.5T	0.6T	nS
t_{CLKT}	TCLK Input Transition Time			3	6	nS
t_{JIT}	TCLK Input Jitter				150	pS (RMS)

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{LLHT}	Bus LVDS Low-to-High Transition Time	R_L = 27Ω C_L=10pF to GND *Figure 3* (Note 4)			0.2	0.4	nS
t_{LHLT}	Bus LVDS High-to-Low Transition Time				0.25	0.4	nS
t_{DIS}	DIN (0-9) Setup to TCLK	R_L = 27Ω, C_L=10pF to GND *Figure 5*		0			nS
t_{DIH}	DIN (0-9) Hold from TCLK			4.0			nS
t_{HZD}	DO ± HIGH to TRI-STATE Delay	R_L = 27Ω, C_L=10pF to GND *Figure 6* (Note 5)			3	10	nS
t_{LZD}	DO ± LOW to TRI-STATE Delay				3	10	nS
t_{ZHD}	DO ± TRI-STATE to HIGH Delay				5	10	nS
t_{ZLD}	DO ± TRI-STATE to LOW Delay				6.5	10	nS
t_{SPW}	SYNC Pulse Width	R_L = 27Ω *Figure 8*		$5*t_{TCP}$			nS
t_{PLD}	Serializer PLL Lock Time			$510*t_{TCP}$		$513*t_{TCP}$	nS
t_{SD}	Serializer Delay	R_L = 27Ω, *Figure 9*		t_{TCP}+ 1.0	t_{TCP}+ 2.0	t_{TCP}+ 3.0	nS
t_{DJIT}	Deterministic Jitter	R_L = 27Ω, C_L=10pF to GND, (Note 6)	40 MHz	-320	-80	150	pS
			66 MHz	-200	-70	80	pS
t_{RJIT}	Random Jitter	R_L = 27Ω, C_L=10pF to GND			19	25	pS (RMS)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 4: t_{LLHT} and t_{LHLT} specifications are Guranteed By Design (GBD) using statistical analysis.

Note 5: Because the Serializer is in TRI-STATE mode, the Deserializer will lose PLL lock and have to resynchronize before data transfer.

Note 6: t_{DJIT} specifications are Guranteed By Design using statistical analysis.

AC Timing Diagrams and Test Circuits

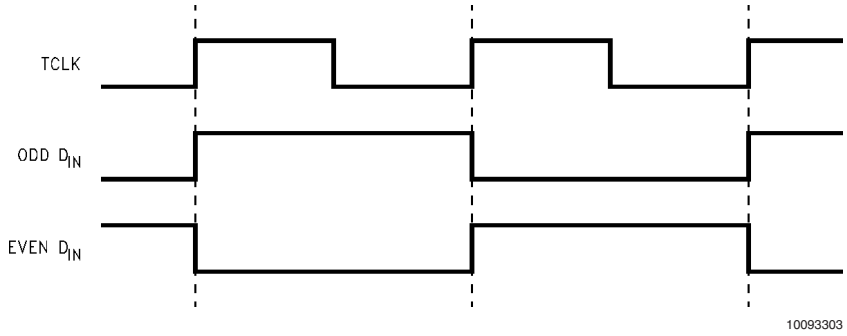


FIGURE 2. "Worst Case" Serializer ICC Test Pattern

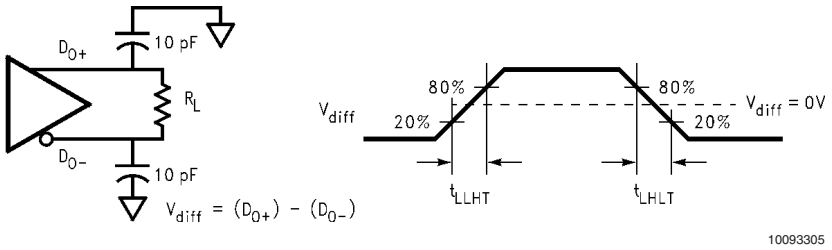


FIGURE 3. Serializer Bus LVDS Output Load and Transition Times

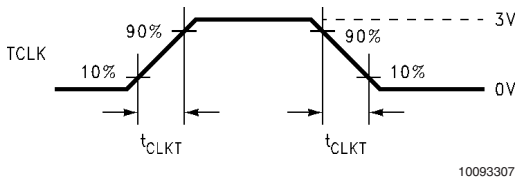
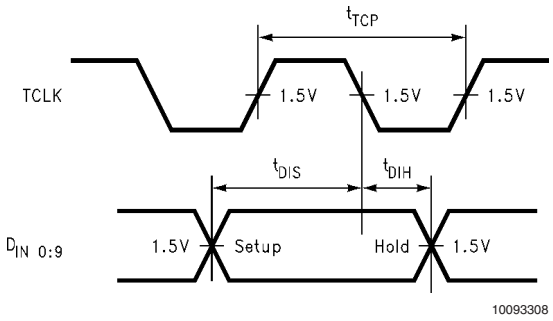


FIGURE 4. Serializer Input Clock Transition Time



Timing shown for TCLK_R/$\overline{F}$ = LOW

FIGURE 5. Serializer Setup/Hold Times

AC Timing Diagrams and Test Circuits (Continued)

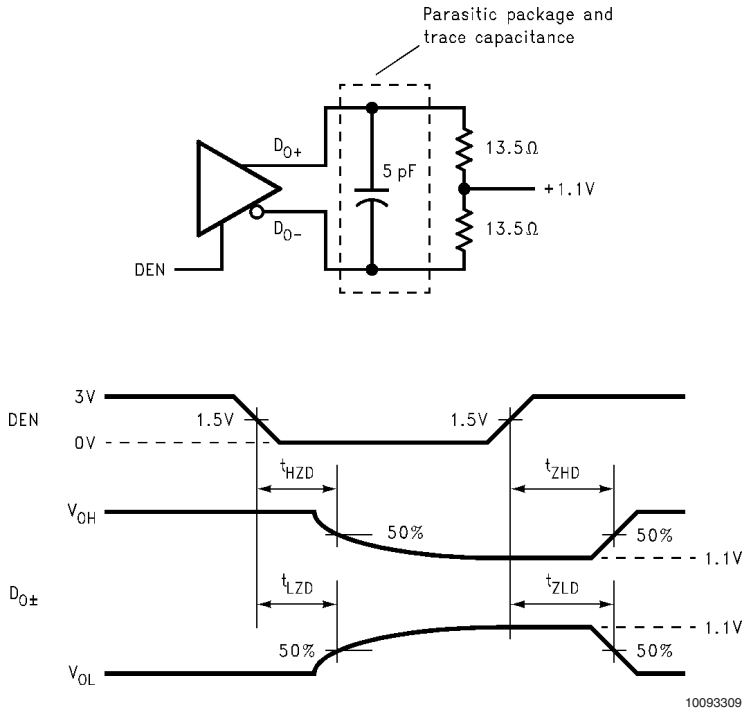


FIGURE 6. Serializer TRI-STATE Test Circuit and Timing

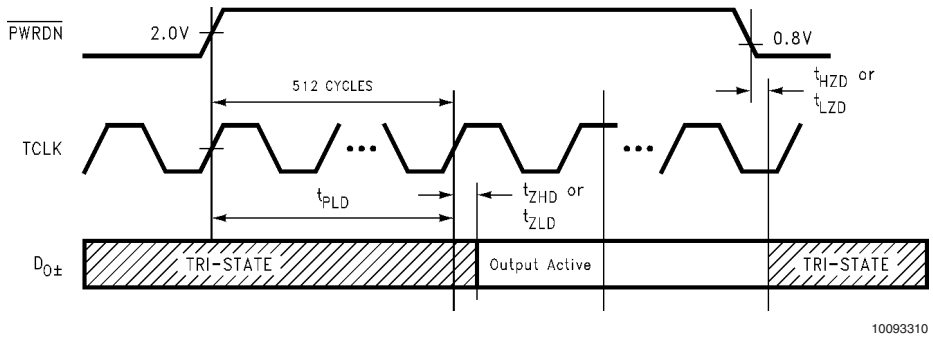


FIGURE 7. Serializer PLL Lock Time, and $\overline{PWRDN}$ TRI-STATE Delays

AC Timing Diagrams and Test Circuits (Continued)

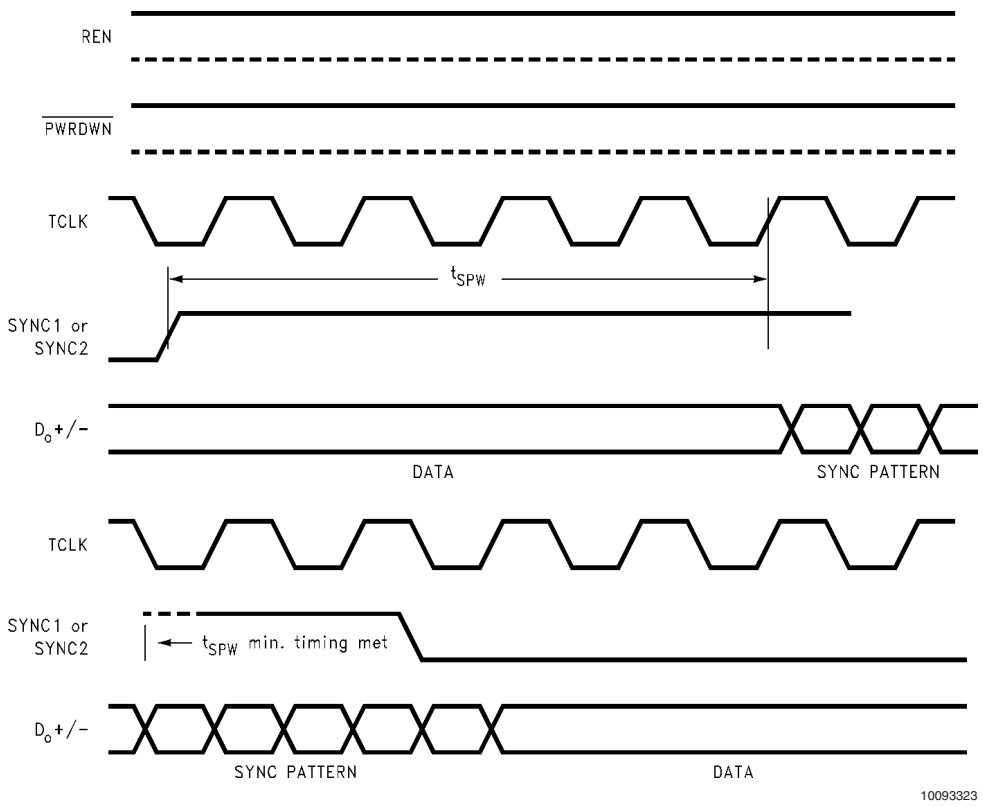


FIGURE 8. SYNC Timing Delays

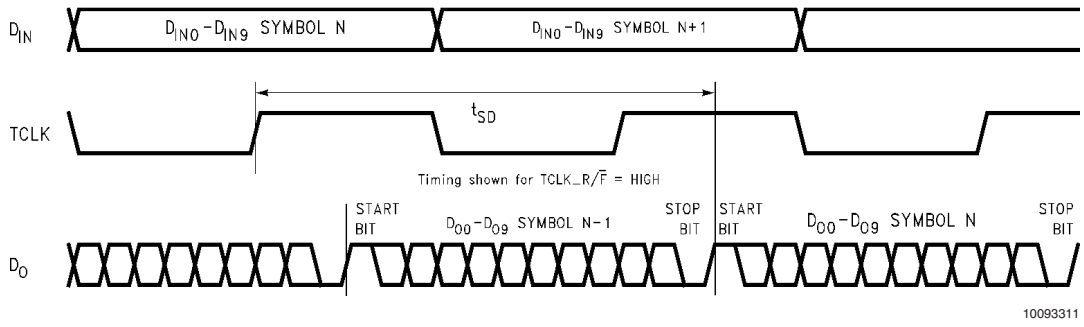
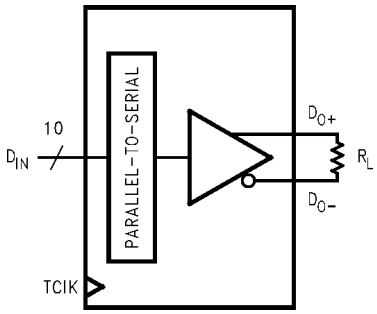


FIGURE 9. Serializer Delay

AC Timing Diagrams and Test Circuits (Continued)



$V_{OD} = (DO^+)–(DO^–)$.

Differential output signal is shown as (DO+)–(DO–), device in Data Transfer mode.

FIGURE 10. V_{OD} Diagram

Application Information

USING THE SERIALIZER AND DESERIALIZER CHIPSET

The Serializer and Deserializer chipset is an easy to use transmitter and receiver pair that sends 10 bits of parallel LVTTL data over a serial Bus LVDS link up to 660 Mbps. An on-board PLL serializes the input data and embeds two clock bits within the data stream. The Deserializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and then deserialize the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the $\overline{LOCK}$ output high when loss of lock occurs.

POWER CONSIDERATIONS

An all CMOS design of the Serializer and Deserializer makes them inherently low power devices. In addition, the constant current source nature of the Bus LVDS outputs minimizes the slope of the speed vs. I_{CC} curve of conventional CMOS designs.

TRANSMITTING DATA

Once you power up the Serializer and Deserializer, they must be phase locked to each other to transmit data. Phase locking occurs when the Deserializer locks to incoming data or when the Serializer sends patterns. The Serializer sends SYNC patterns whenever the SYNC1 or SYNC2 inputs are high. The $\overline{LOCK}$ output of the Deserializer remains high until it has locked to the incoming data stream. Connecting the $\overline{LOCK}$ output of the Deserializer to one of the SYNC inputs of the Serializer will guarantee that enough SYNC patterns are sent to achieve Deserializer lock.

The Deserializer can also lock to incoming data by simply powering up the device and allowing the “random lock” circuitry to find and lock to the data stream.

While the Deserializer $\overline{LOCK}$ output is low, data at the Deserializer outputs (ROUT0-9) is valid, except for the specific case of loss of lock during transmission which is further discussed in the "Recovering from LOCK Loss" section below.

HOT INSERTION

All the BLVDS devices are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), and then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground. Random lock hot insertion is illustrated in *Figure 11*.

PCB CONSIDERATIONS

The Bus LVDS Serializer and Deserializer should be placed as close to the edge connector as possible. In multiple Deserializer applications, the distance from the Deserializer to the slot connector appears as a stub to the Serializer driving the backplane traces. Longer stubs lower the impedance of the bus, increase the load on the Serializer, and lower the threshold margin at the Deserializers. Deserializer devices should be placed much less than one inch from slot connectors. Because transition times are very fast on the Serializer Bus LVDS outputs, reducing stub lengths as much as possible is the best method to ensure signal integrity.

TRANSMISSION MEDIA

The Serializer and Deserializer can also be used in point-to-point configuration of a backplane, through a PCB trace, or through twisted pair cable. In point-to-point configuration, the transmission media need only be terminated at the receiver end. Please note that in point-to-point configuration, the potential of offsetting the ground levels of the Serializer vs. the Deserializer must be considered. Also, Bus LVDS provides a +/– 1.2V common mode range at the receiver inputs.

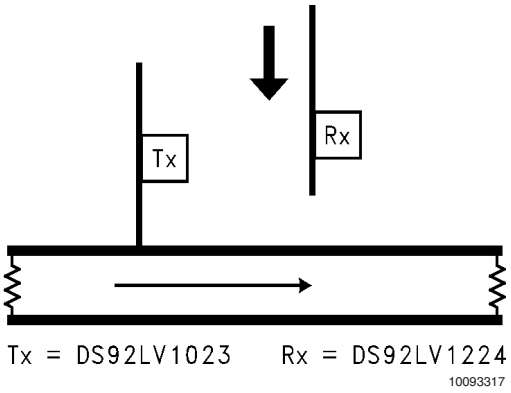
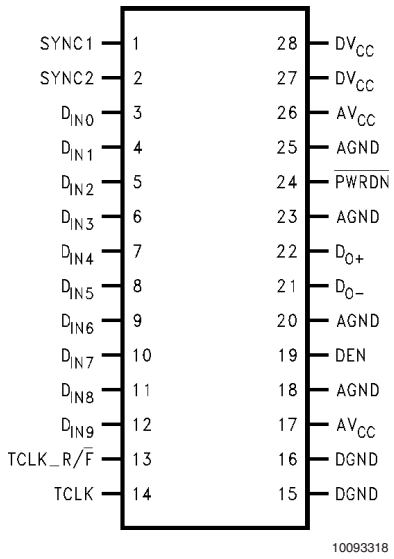


FIGURE 11. Random Lock Hot Insertion

Pin Diagrams

DS92LV1023TMSA - Serializer



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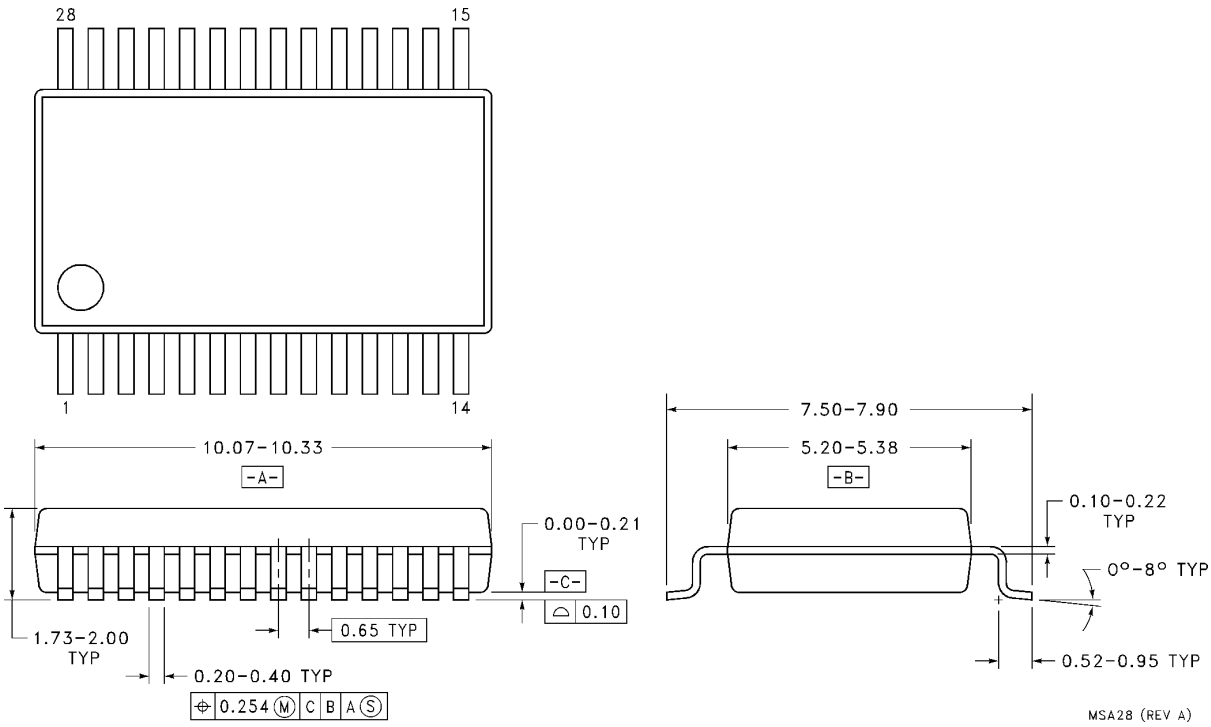
Serializer Pin Description

Pin Name	I/O	No.	Description
DIN	I	3–12	Data Input. LVTTL levels inputs. Data on these pins are loaded into a 10-bit input register.
TCLK_R/$\overline{F}$	I	13	Transmit Clock Rising/Falling strobe select. LVTTL level input. Selects TCLK active edge for strobing of DIN data. High selects rising edge. Low selects falling edge.
DO+	O	22	+ Serial Data Output. Non-inverting Bus LVDS differential output.
DO–	O	21	– Serial Data Output. Inverting Bus LVDS differential output.
DEN	I	19	Serial Data Output Enable. LVTTL level input. A low, puts the Bus LVDS outputs in TRI-STATE.
$\overline{PWRDN}$	I	24	Powerdown. LVTTL level input. $\overline{PWRDN}$ driven low shuts down the PLL and TRI-STATEs outputs putting the device into a low power sleep mode.
TCLK	I	14	Transmit Clock. LVTTL level input. Input for 40 MHz–66 MHz (nominal) system clock.
SYNC	I	1, 2	Assertion of SYNC (high) for at least 1024 synchronization symbols to be transmitted on the Bus LVDS serial output. Synchronization symbols continue to be sent if SYNC continues asserted. TTL level input. The two SYNC pins are ORed.
DVCC	I	27, 28	Digital Circuit power supply.
DGND	I	15, 16	Digital Circuit ground.
AVCC	I	17, 26	Analog power supply (PLL and Analog Circuits).
AGND	I	18, 25, 20, 23	Analog ground (PLL and Analog Circuits).

Physical Dimensions inches (millimeters)

unless otherwise noted



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