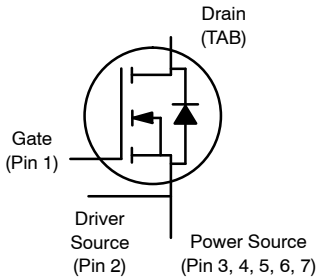
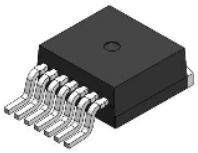
Silicon Carbide (SiC) MOSFET – EliteSiC, 20 mohm, 1200 V, M1, D2PAK-7L

NTBG020N120SC1

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
1200 V	28 mΩ @ 20 V	98 A



N–CHANNEL MOSFET



D2PAK–7L
CASE 418BJ

Features

- Typ. $R_{DS(on)}$ = 20 mΩ
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 220 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 258 pF)
- 100% Avalanche Tested
- T_J = 175°C
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb–Free 2LI (on second level interconnection)

Typical Applications

- UPS
- DC–DC Converter
- Boost Inverter

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	1200	V
Gate–to–Source Voltage			V_{GS}	–15/+25	V
Recommended Operation Values of Gate–to–Source Voltage		T_C < 175°C	V_{GSop}	–5/+20	V
Continuous Drain Current (Note 2)	Steady State	T_C = 25°C	I_D	98	A
Power Dissipation (Note 2)	Steady State	T_C = 25°C	P_D	468	W
Continuous Drain Current (Notes 1, 2)	Steady State	T_A = 25°C	I_D	8.6	A
Power Dissipation (Notes 1, 2)	Steady State	T_A = 25°C	P_D	3.7	W
Pulsed Drain Current (Note 3)	T_A = 25°C		I_{DM}	392	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	–55 to +175	°C
Source Current (Body Diode)			I_S	46	A
Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)}$ = 23 A, L = 1 mH) (Note 4)			E_{AS}	264	mJ
Maximum Lead Temperature for Soldering (1/8″ from case for 5 s)			T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR–4 board using1 in^2 pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4. EAS of 264 mJ is based on starting T_J = 25°C; L = 1 mH, I_{AS} = 23 A, V_{DD} = 120 V, V_{GS} = 18 V.

MARKING DIAGRAM

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability
NTBG020120SC1 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTBG020N120SC1	D2PAK–7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case − Steady State (Note 2)	$R_{\theta JC}$	0.32	°C/W
Junction−to−Ambient − Steady State (Notes 1, 2)	$R_{\theta JA}$	41	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		1200			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 1 mA, referenced to 25°C			0.5		V/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V	T_J = 25°C			100	μA
			T_J = 175°C			1	mA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = +25/−15 V, V_{DS} = 0 V				±1	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 20 mA		1.8	2.7	4.3	V
Recommended Gate Voltage	V_{GOP}			−5		+20	V
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 20 V, I_D = 60 A, T_J = 25°C			20	28	mΩ
		V_{GS} = 20 V, I_D = 60 A, T_J = 175°C			35	50	
Forward Transconductance	g_{FS}	V_{DS} = 20 V, I_D = 60 A			34		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 800 V			2943		pF
Output Capacitance	C_{OSS}				258		
Reverse Transfer Capacitance	C_{RSS}				24		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −5/20 V, V_{DS} = 600 V, I_D = 80 A			220		nC
Threshold Gate Charge	$Q_{G(TH)}$				33		
Gate−to−Source Charge	Q_{GS}				66		
Gate−to−Drain Charge	Q_{GD}				63		
Gate−Resistance	R_G	f = 1 MHz			1.6		Ω
SWITCHING CHARACTERISTICS							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −5/20 V, V_{DS} = 800 V, I_D = 80 A, R_G = 2 Ω inductive load			22	35	ns
Rise Time	t_r				20	32	
Turn−Off Delay Time	$t_{d(OFF)}$				42	67	
Fall Time	t_f				9	18	
Turn−On Switching Loss	E_{ON}				461		μJ
Turn−Off Switching Loss	E_{OFF}				400		
Total Switching Loss	E_{tot}				861		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Continuous Drain−Source Diode Forward Current	I_{SD}	V_{GS} = −5 V, T_J = 25°C				46	A
Pulsed Drain−Source Diode Forward Current (Note 3)	I_{SDM}					392	
Forward Diode Voltage	V_{SD}	V_{GS} = −5 V, I_{SD} = 30 A, T_J = 25°C			3.7		V
Reverse Recovery Time	t_{RR}	V_{GS} = −5/20 V, I_{SD} = 80 A, dI_S/dt = 1000 A/μs			31		ns
Reverse Recovery Charge	Q_{RR}				228		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

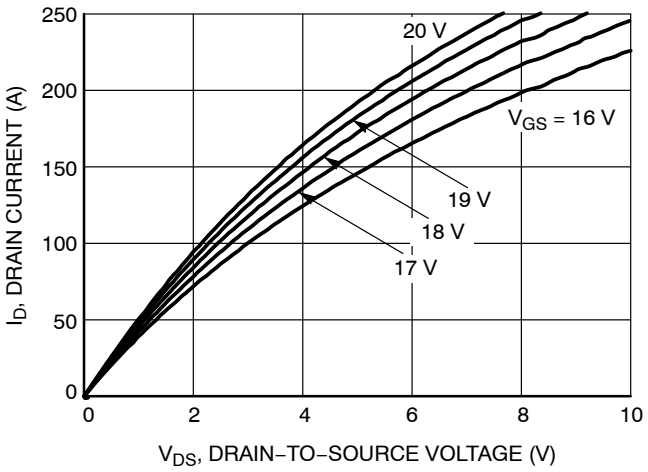


Figure 1. On−Region Characteristics

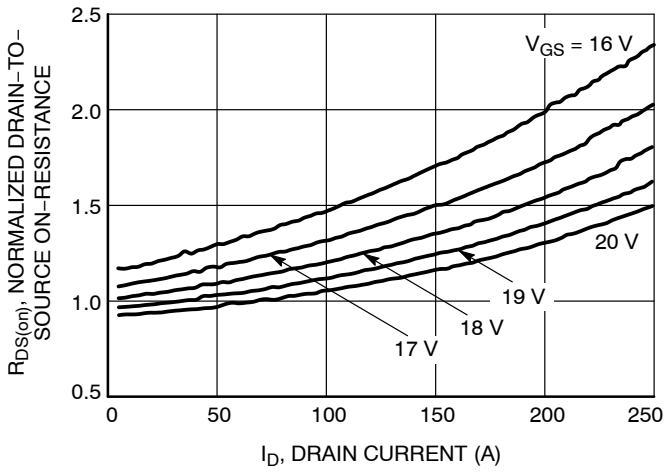


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

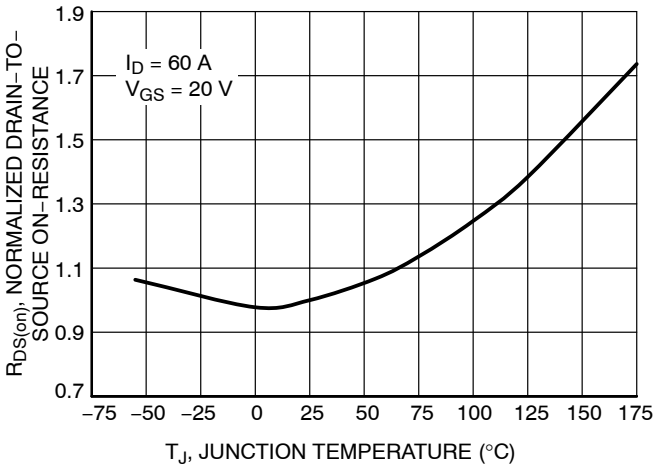


Figure 3. On−Resistance Variation with Temperature

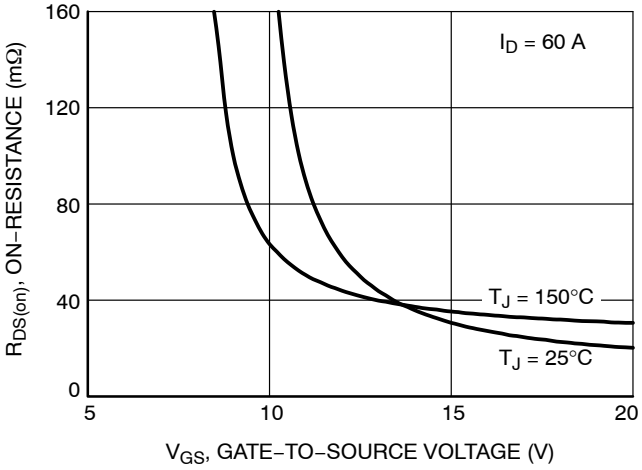


Figure 4. On−Resistance vs. Gate−to−Source Voltage

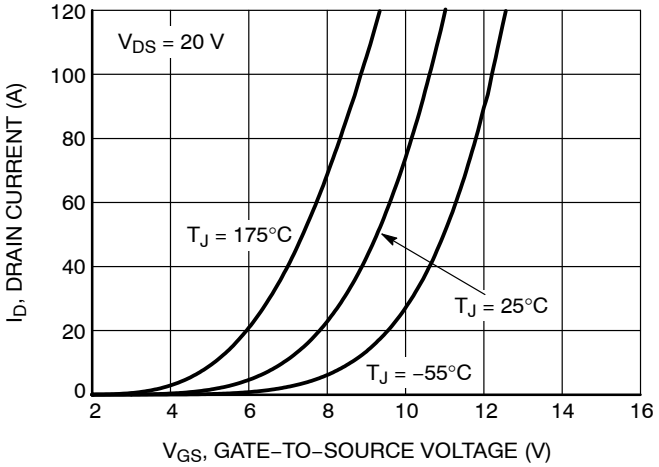


Figure 5. Transfer Characteristics

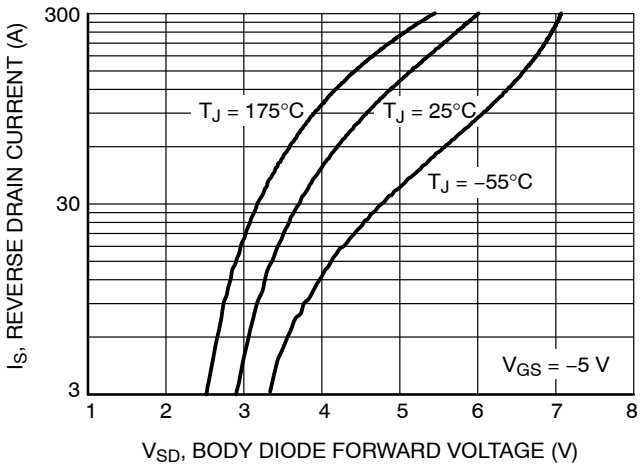


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (continued)

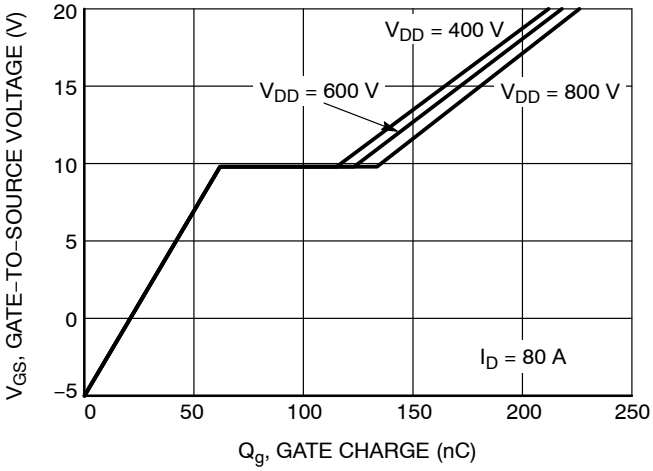


Figure 7. Gate−to−Source Voltage vs. Total Charge

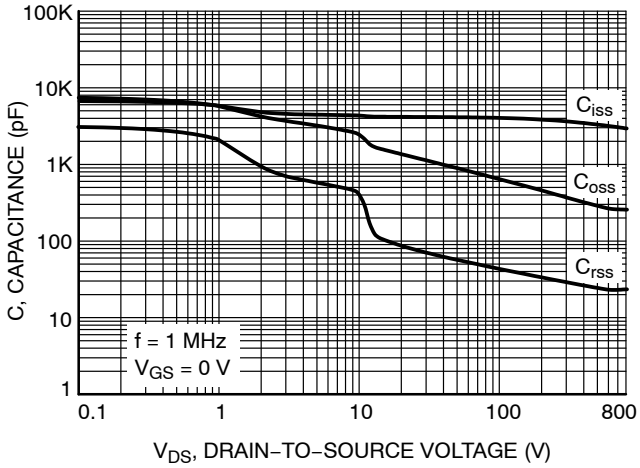


Figure 8. Capacitance vs. Drain−to−Source Voltage

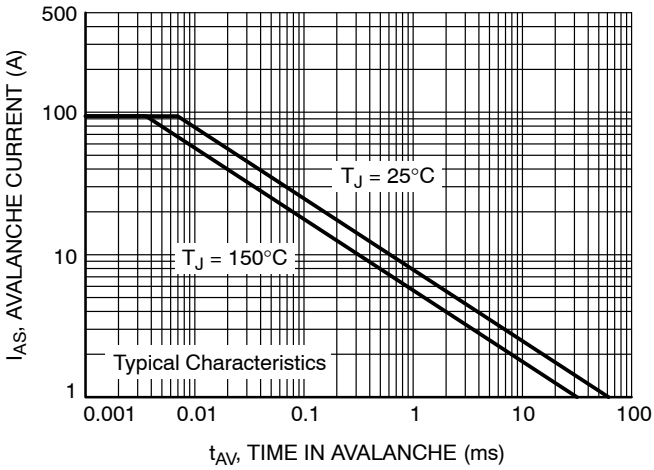


Figure 9. Unclamped Inductive Switching Capability

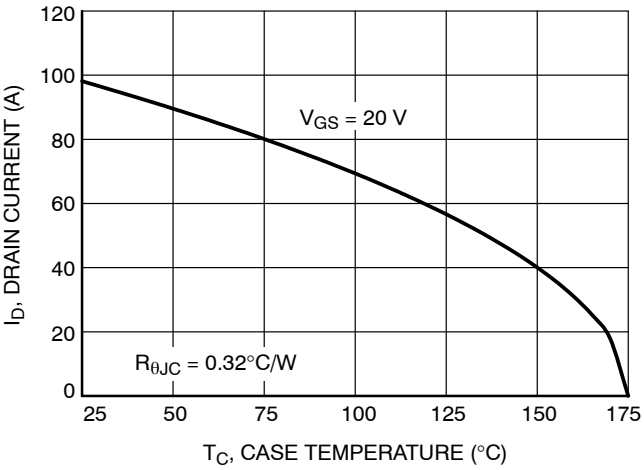


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

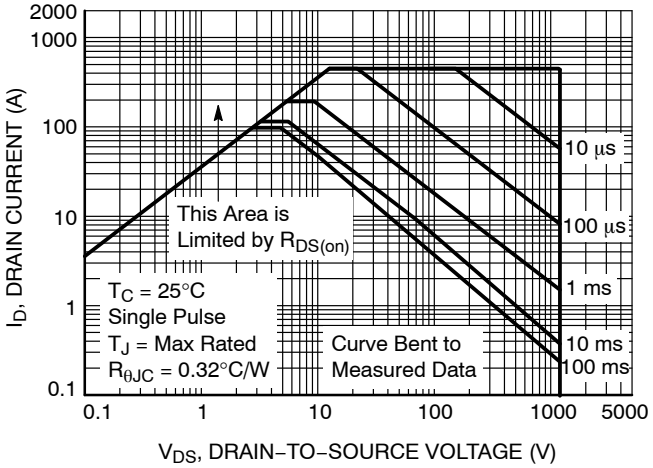


Figure 11. Maximum Rated Forward Biased Safe Operating Area

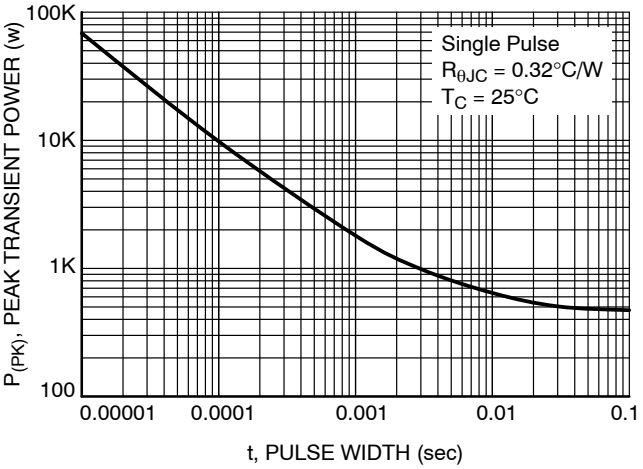


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

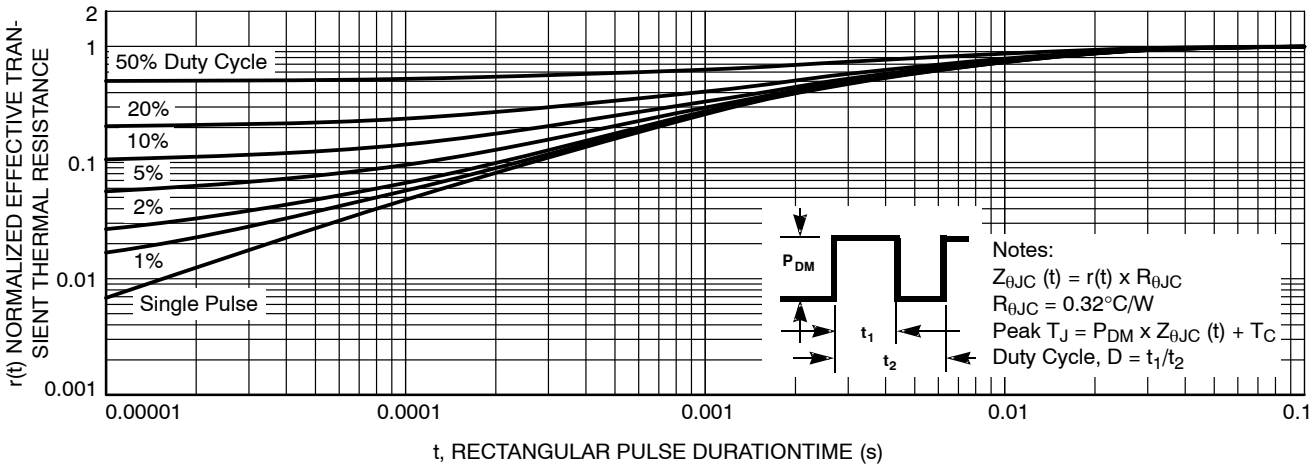
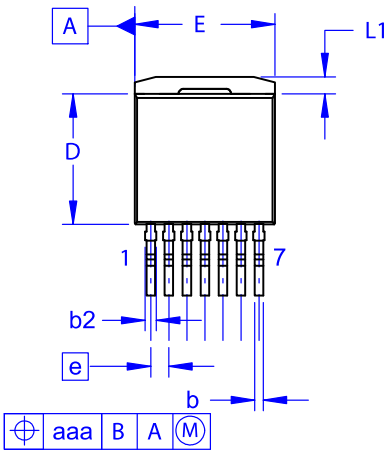


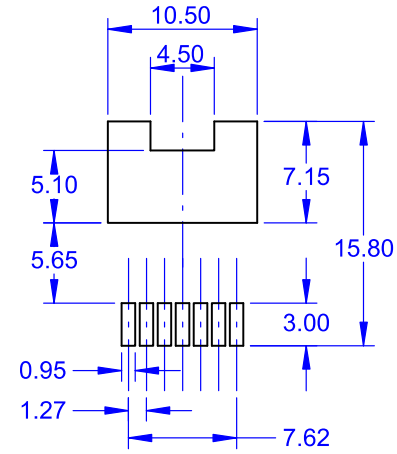
Figure 13. Junction−to−Case Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

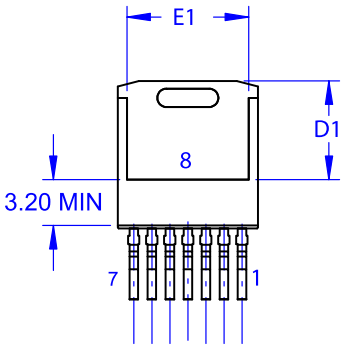
D²PAK7 (TO−263−7L HV)
CASE 418BJ
ISSUE B

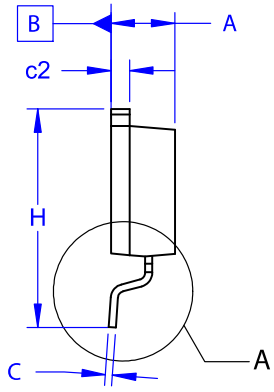
DATE 16 AUG 2019





LAND PATTERN RECOMMENDATION





NOTES:

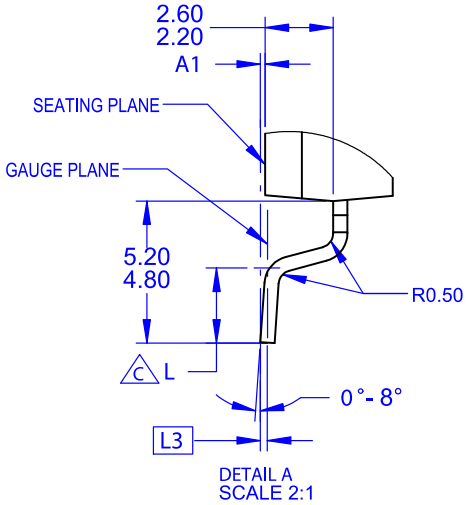
A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. OUT OF JEDEC STANDARD VALUE.
D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



DETAIL A
SCALE 2:1

DOCUMENT NUMBER:	**98AON84234G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**D²PAK7 (TO−263−7L HV)**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales