

Ultra-Low Phase Jitter LVPECL SMD Clock Oscillator

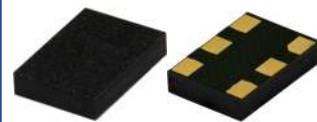
ASVMX-156.250MHz-3BNR



ESD Sensitive



RoHS/RoHS II compliant



7.0 x 5.0 x 1.4mm

Moisture Sensitivity Level – MSL 3

FEATURES:

- 156.25MHz LVPECL
- Typical phase noise: 80fs (Integration range: 1.875MHz-20MHz)
- ± 50 ppm total frequency stability over -40°C to $+85^{\circ}\text{C}$ temperature range
- Industry standard 6-Pin 7 x 5mm LGA package

APPLICATIONS:

- 10/40/400 Gigabit Ethernet
- Fibre Channel 10G/12G SERDES

KEY ELECTRICAL SPECIFICATIONS

Item	Minimum	Maximum	Unit	Condition
Supply Voltage	-0.3	+3.6	V	
Storage Temp.	-55	+125	$^{\circ}\text{C}$	
Lead Temp.(soldering, 10s)		+260	$^{\circ}\text{C}$	
ESD (HBM)		2	kV	

VDD = 2.375 - 3.63V, TA = -40°C to $+85^{\circ}\text{C}$, outputs terminated with 50 Ohms to VDD - 2.⁽¹⁾

Parameters	Minimum	Typical	Maximum	Units	Notes
Frequency	156.250			MHz	
Operating Temperature (TA)	-40		+85	$^{\circ}\text{C}$	
Overall Frequency Stability ⁽²⁾	-50		+50	ppm	
Supply Voltage (VDD)	+2.375		+3.63	V	
Supply Current (IDD)			120	mA	
Output Logic Level	V _{OH}	V _{DD} -1.35	V _{DD} -1.01	V _{DD} -0.8	V
	V _{OL}	V _{DD} -2.0	V _{DD} -1.78	V _{DD} -1.6	V
Peak to Peak Output Swing (V _{swing})	0.65	0.77	0.95	V	Single ended
Start-up Time			20	ms	
Rise Time (Tr)	300			ps	RL=50 Ω , CL=0pF 20% to 80%
Fall Time (Tf)	300				
Duty Cycle	45		55	%	
Phase Noise	Integration Range: 12kHz to 20MHz		175	fsRMS	
	Integration Range: 1.875MHz to 20MHz		80		

Notes:

1. Guaranteed after thermal equilibrium
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to $+85^{\circ}\text{C}$.

PART IDENTIFICATION

ASVMX-156.250MHz -3BNR -

Packing

Blank: Bulk or Tube

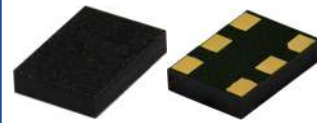
T: Tape & Reel (1k/reel)

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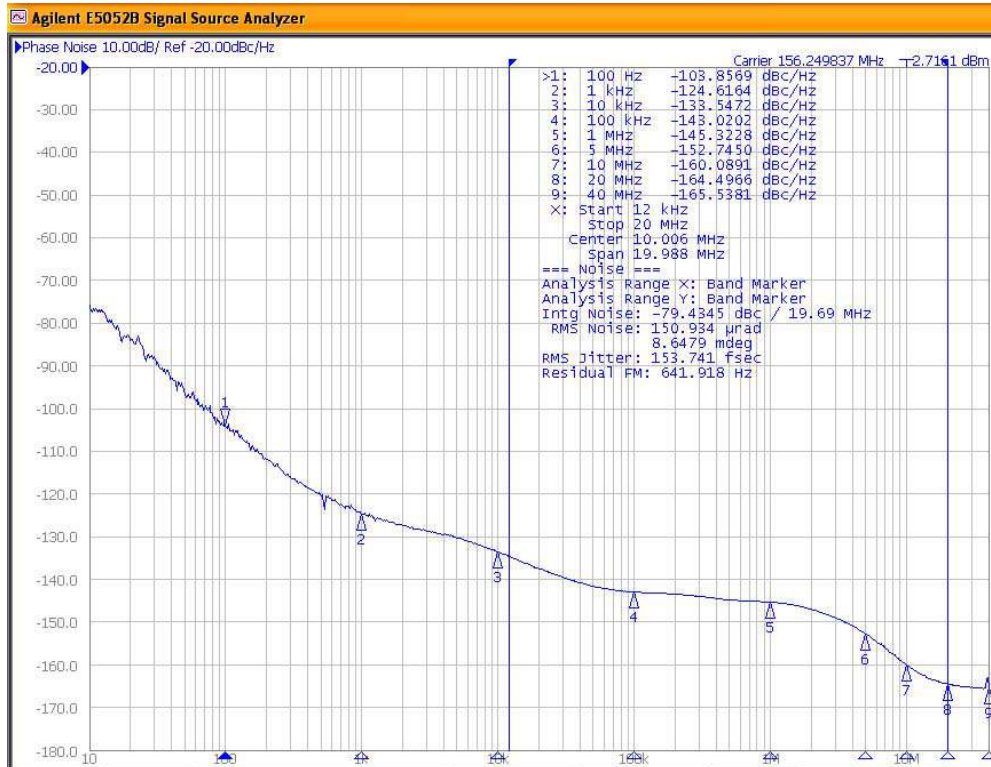
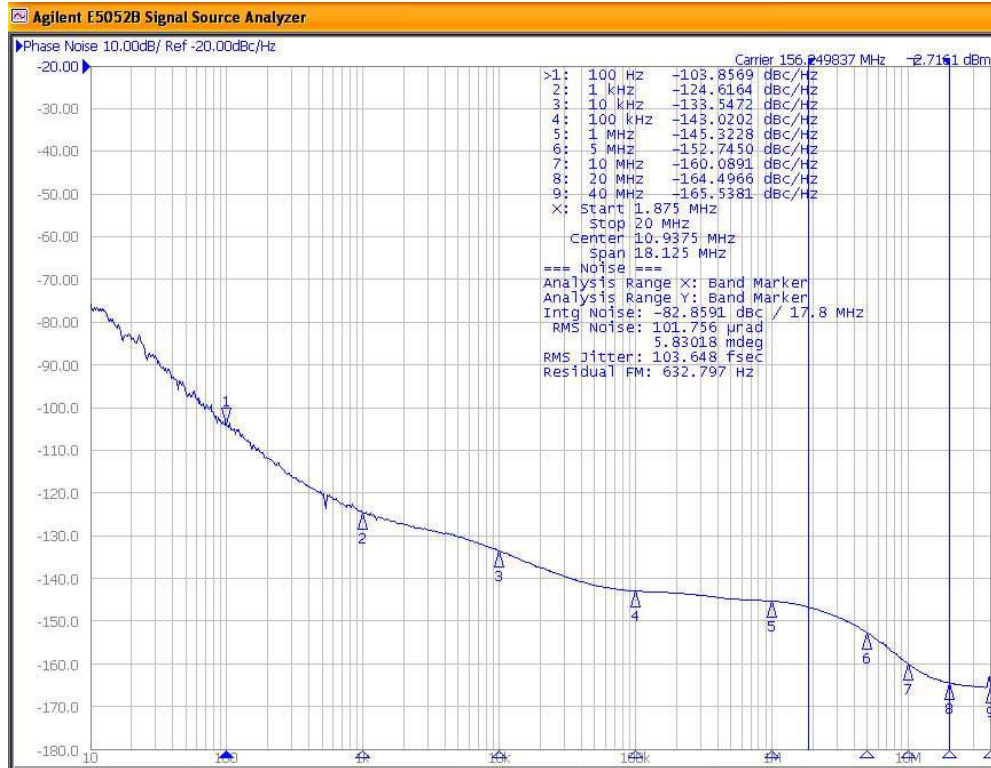


RoHS/RoHS II compliant



7.0 x 5.0 x 1.4mm

TYPICAL PHASE NOISE



ABRACON IS
ISO9001:2008
CERTIFIED



2 Faraday, Suite# B | Irvine | CA 92618 Revised: 04.27.15

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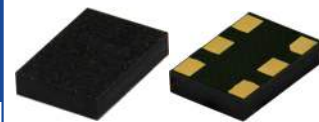
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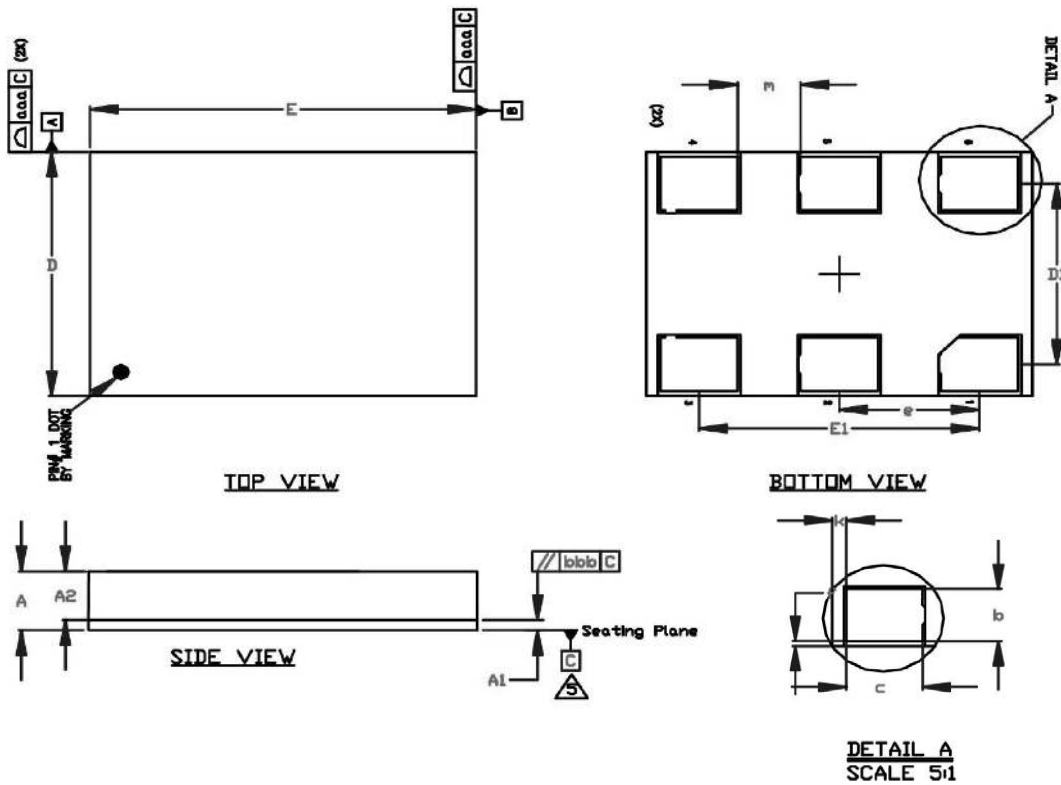


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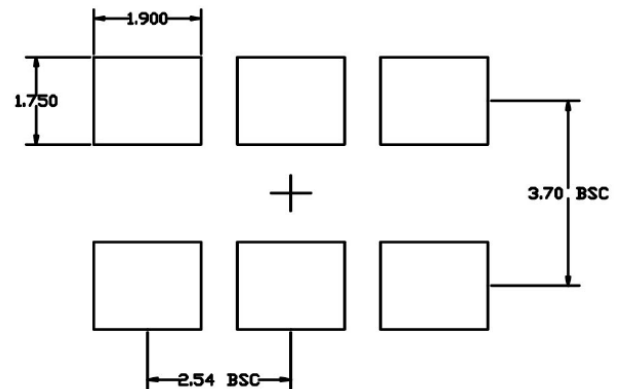
OUTLINE DIMENSION



Ref.	Min.	Nom.	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	4.900	5.000	5.100
D1	3.700 BSC		
E	6.900	7.000	7.100
E1	5.080 BSC		
b	1.050	1.100	1.150
c	1.350	1.400	1.450
e	2.540 BSC		
f	0.050	0.100	0.150
k	0.210	0.260	0.310
m	1.090	1.140	1.190
n	36		

Dimensional Tolerance	
aaa	0.100
bbb	0.070

Recommended Land Pattern



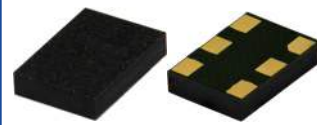
Dimensions: mm

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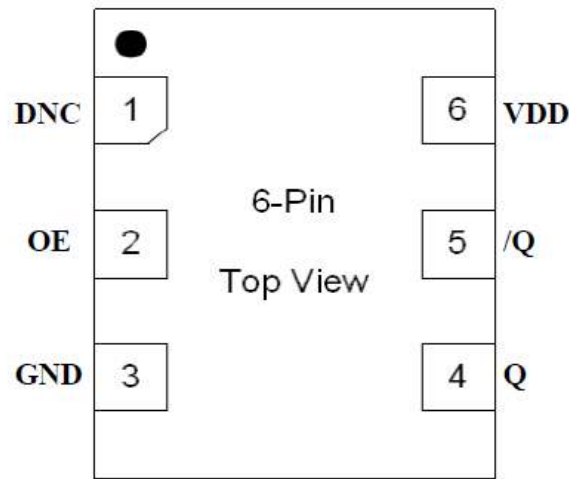


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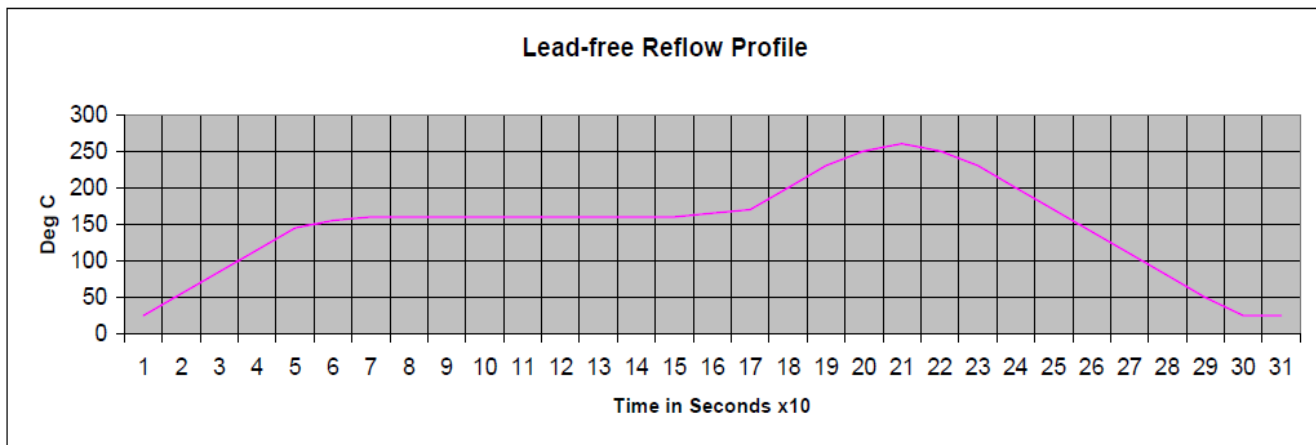
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PIN CONFIGURATION



Pin #	Pin Name	Pin Type	Pin Level	Pin Function
1	DNC			Make no connection, leave floating
2	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state. 0 = Disabled, 1= Enabled, 50k Ω Pull-up
3	GND	PWR		Power Supply Ground
4	Q	O	LVPECL	Clock Output
5	/Q	O	LVPECL	Complimentary Clock Output
6	VDD	PWR		Power Supply

REFLOW PROFILE



Parameters	Specifications
Average Ramp-up Rate	3°C /second max.
Pre-Heat Temp 150 – 200°C	60 – 180 second
Temp > 217°C	60 – 150 second
Time @ Peak Temperature	20 – 40 second
Peak Temperature	260°C + 0°C / -5°C
Ramp-down Rate	-6°C / second max.
Time 25°C to Peak Temp.	8 minutes max.

