TS472

Very low noise microphone preamplifier with 2.0 V bias output and active low standby mode

Features

- Low noise: 10 nV/√Hz typ. equivalent input noise at F = 1 kHz
- Fully-differential input/output
- 2.2 to 5.5 V single supply operation
- Low power consumption at 20 dB: 1.8 mA
- Fast start up time at 0 dB: 5 ms typ.
- Low distortion: 0.1% typ.
- 40 kHz bandwidth regardless of the gain
- Active low standby mode function (1 µA max)
- Low noise 2.0 V microphone bias output
- Available in flip-chip lead-free package and in QFN24 4 x 4 mm package
- ESD protection (2 kV)

Applications

- Video and photo cameras with sound input
- Sound acquisition and voice recognition
- Video conference systems
- Notebook computers and PDAs

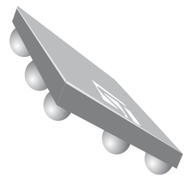
Description

The TS472 is a differential-input microphone preamplifier optimized for high-performance PDA and notebook audio systems.

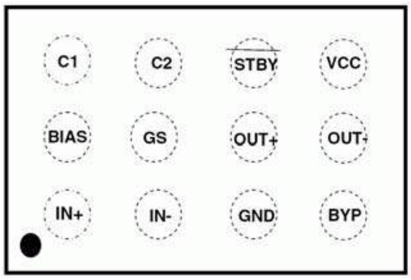
This device features an adjustable gain from 0 to 40 dB with excellent power-supply and common-mode rejection ratios. In addition, the TS472 has a very low noise microphone bias generator of 2 V.

It also includes a complete shutdown function, with active low standby mode.

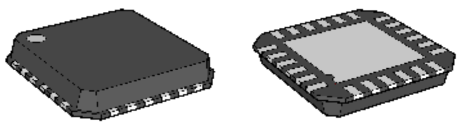
Flip-chip - 12 bumps



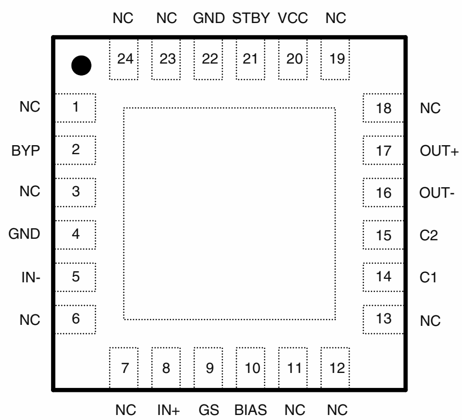
Pin connections (top view)



QFN24



Pin connections (top view)



Contents

1 Typical application schematic

Figure 1 shows a typical application schematic for the TS472.

Figure 1. Application schematic (flip-chip)

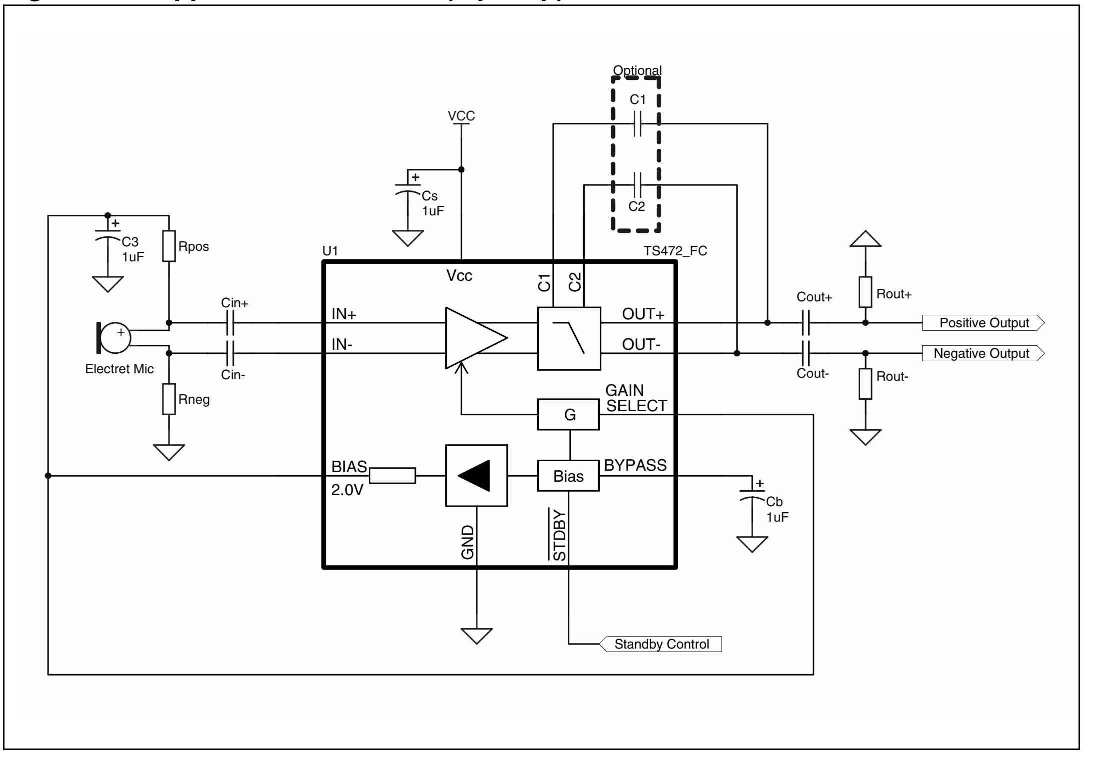


Table 1. Description of external components

Components	Functional description
C_{in+}, C_{in-}	Input coupling capacitors that block the DC voltage at the amplifier input terminal.
C_{out+}, C_{out-}	Output coupling capacitors that block the DC voltage coming from the amplifier output terminal (pins C2 and D2) and determine the lower cut-off frequency (see *Section 4.3: Lower cut-off frequency*).
R_{out+}, R_{out-}	Output load resistors used to charge the output coupling capacitors C_{out}. These output resistors can be represented by an input impedance of a following stage.
R_{pos}, R_{neg}	Polarizing resistors for biasing of a microphone.
C_s	Supply bypass capacitor that provides power supply filtering.
C_b	Bypass pin capacitor that provides half-supply filtering.
C_1, C_2	Low pass filter capacitors allowing to cut the high frequency.
C_3	Bias output filtering capacitor.

Table 2. Pin descriptions

Pin name	Flip-chip designator	QFN designator	Pin description
IN+	A1	8	Positive differential input
IN-	B1	5	Negative differential input
BIAS	A2	10	2 V bias output
GND	C1	4, 22	Ground
STBY	C3	21	Standby
BYP	D1	2	Bypass
GS	B2	9	Gain select
OUT-	D2	16	Negative differential output
OUT+	C2	17	Positive differential output
C1	A3	14	Low-pass filter capacitor
C2	B3	15	Low-pass filter capacitor
Vcc	D3	20	Power supply
NC	---	3, 6, 7, 11, 12, 13, 18, 19, 23, 24	Not connected, floating pins

2 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage	-0.3 to V_{CC}+0.3	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient: Flip-chip QFN24	180 110	°C/W
ESD	Human body model	2	kV
ESD	Machine model	200	V
	Lead temperature (soldering, 10sec)	250	°C

1. All voltage values are measured with respect to the ground pin.

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.2 to 5.5	V
A	Typical differential gain (GS connected to 4.7 kΩ or bias)	20	dB
V_{STBY}	Standby voltage input: Device ON Device OFF	$1.5 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
T_{op}	Operational free air temperature range	-40 to +85	°C
R_{thja}	Thermal resistance junction to ambient: Flip-chip QFN24	150 60	°C/W

3 Electrical characteristics

Table 5. Electrical characteristics at V_{CC} = 3 V with GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage density R_{EQ} = 100 Ω at 1 kHz		10		$\frac{nV}{\sqrt{Hz}}$
THD+N	Total harmonic distortion + noise 20 Hz ≤ F ≤ 20 kHz, gain = 20 dB, V_{in} = 50 mV_{RMS}		0.1		%
V_{in}	Input voltage, gain = 20 dB		10	70	mV_{RMS}
B_W	Bandwidth at -3 dB Bandwidth at -1 dB pin A3, B3 floating		40 20		kHz
G	Overall output voltage gain (Rgs variable): Minimum gain, Rgs infinite Maximum gain, Rgs = 0	-3 39.5	-1.5 41	0 42.5	dB
Z_{in}	Input impedance referred to GND	80	100	120	kΩ
R_{LOAD}	Resistive load	10			kΩ
C_{LOAD}	Capacitive load			100	pF
I_{CC}	Supply current, gain = 20 dB		1.8	2.4	mA
I_{STBY}	Standby current			1	µA
PSRR	Power supply rejection ratio, gain = 20 dB, F = 217 Hz, V_{ripple} = 200 mVpp, inputs grounded Differential output Single-ended outputs,		-70 -46		dB

Table 6. Bias output: V_{CC} = 3 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{out}	No load condition	1.9	2	2.1	V
R_{out}	Output resistance	80	100	120	W
I_{out}	Output bias current		2		mA
PSRR	Power supply rejection ratio, F = 217 Hz, V_{ripple} = 200 mVpp	70	80		dB

Table 7. Differential RMS noise voltage

Gain (dB)	Input referred noise voltage (μV_{RMS})		Output noise voltage (μV_{RMS})	
	Unweighted filter	A-weighted filter	Unweighted filter	A-weighted filter
0	15	10	15	10
20	3.4	2.3	34	23
40	1.4	0.9	141	91

Table 8. Bias output RMS noise voltage

C_3[1] (μF)	Unweighted filter (μV_{RMS})	A-weighted filter (μV_{RMS})
1	5	4.4
10	2.2	1.2

1. Bias output filtering capacitor.

Table 9. SNR (signal to noise ratio), THD+N < 0.5%

Gain (dB)	Unweighted filter 20 Hz - 20 kHz (dB)			A-weighted filter (dB)		
	V_{CC} = 2.2 V	V_{CC} = 3 V	V_{CC} = 5.5 V	V_{CC} = 2.2 V	V_{CC} = 3 V	V_{CC} = 5.5 V
0	75	76	76	79	80	80
20	82	83	83	89	90	90
40	70	72	74	80	82	84

Figure 2. Current consumption vs. power supply voltage

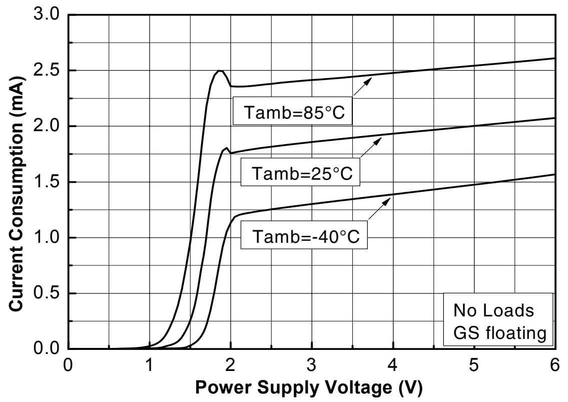


Figure 3. Current consumption vs. power supply voltage

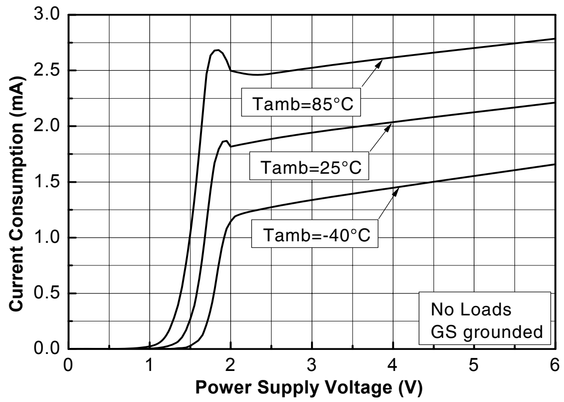


Figure 4. Current consumption vs. standby voltage

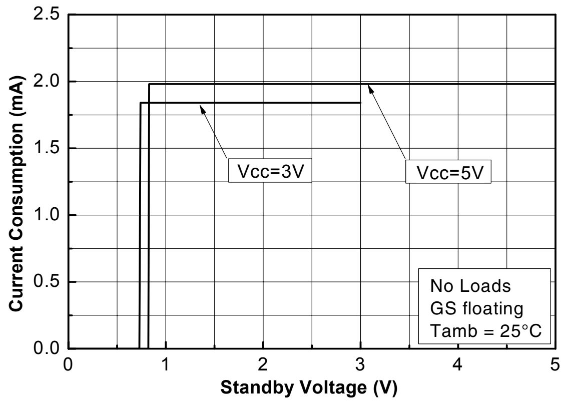


Figure 5. Current consumption vs. standby voltage

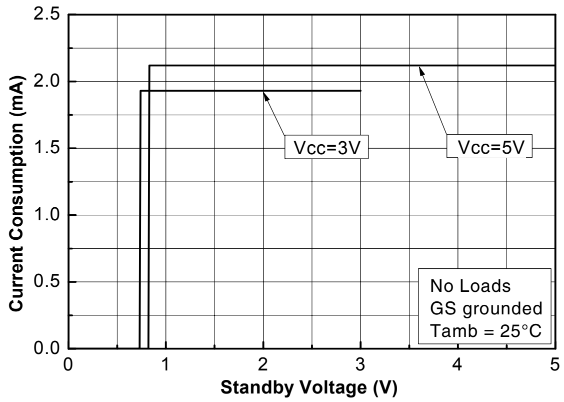


Figure 6. Standby threshold voltage vs. power supply voltage

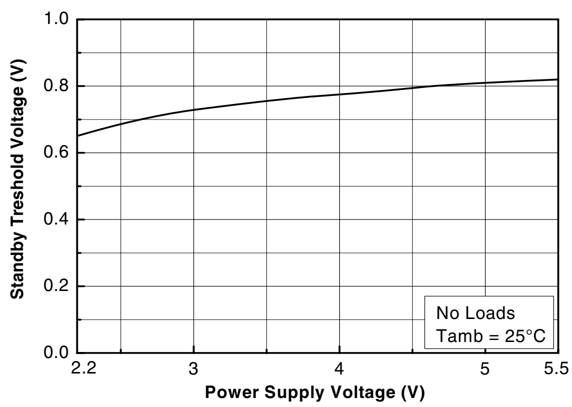


Figure 7. Frequency response

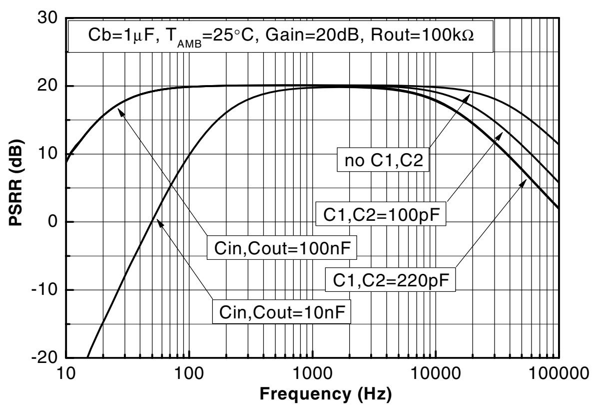


Figure 8. Bias output voltage vs. bias output current

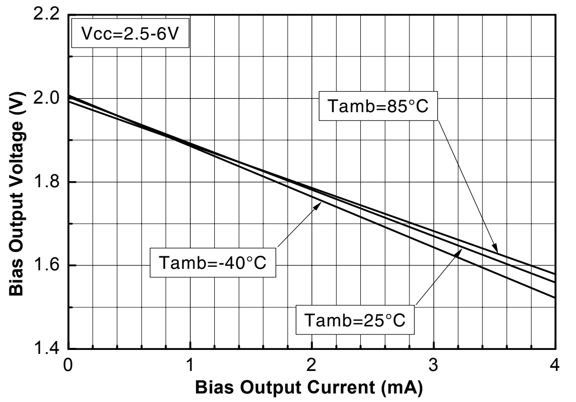


Figure 9. Bias output voltage vs. power supply voltage

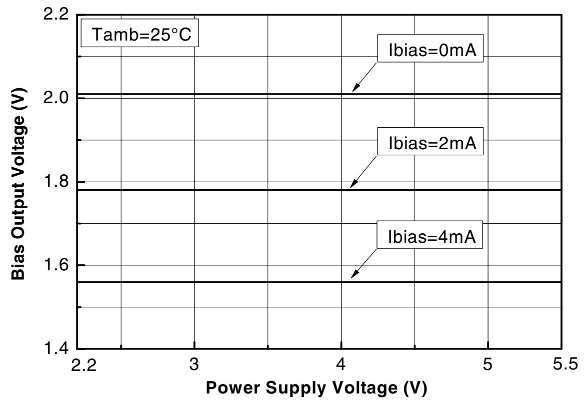


Figure 10. Bias PSRR vs. frequency

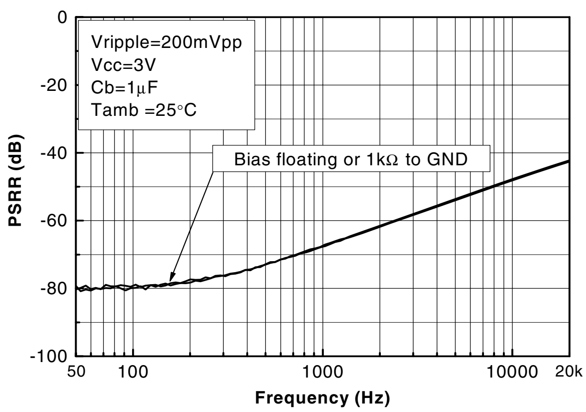


Figure 11. Bias PSRR vs. frequency

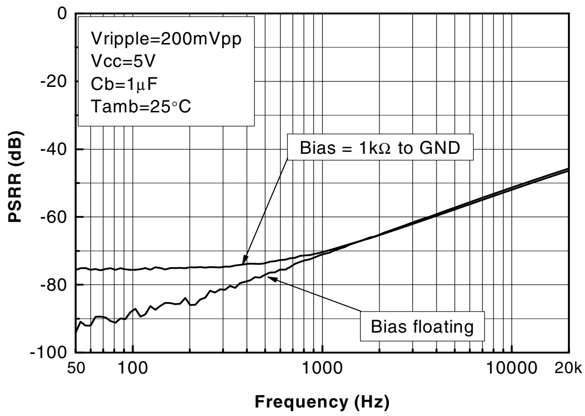


Figure 12. Differential output PSRR vs. frequency

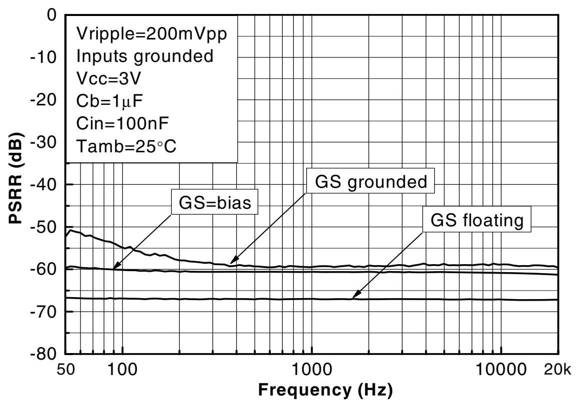


Figure 13. Differential output PSRR vs. frequency

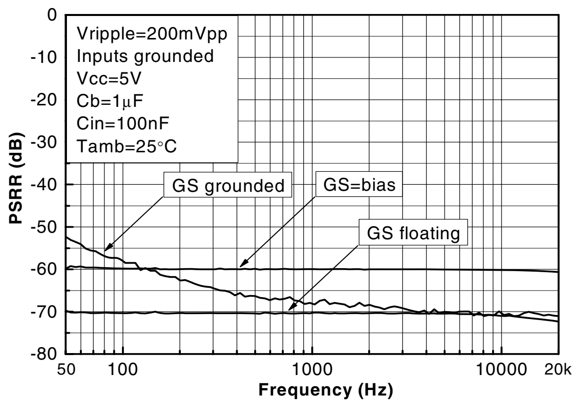


Figure 14. Differential output PSRR vs. frequency

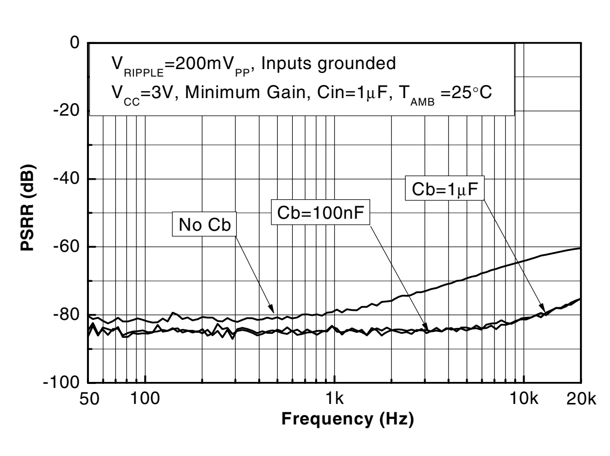


Figure 15. Differential output PSRR vs. frequency

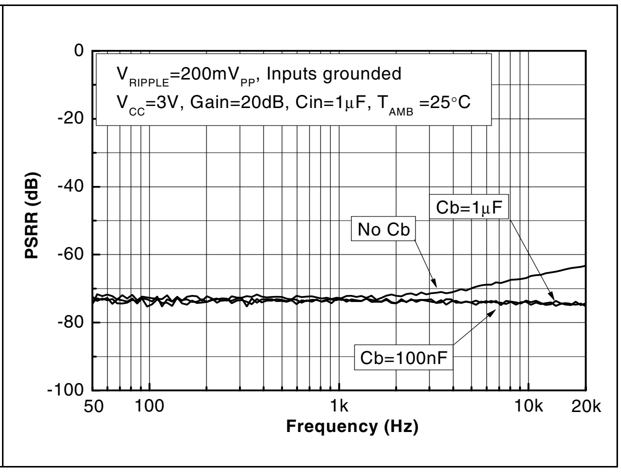


Figure 16. Single-ended output PSRR vs. frequency

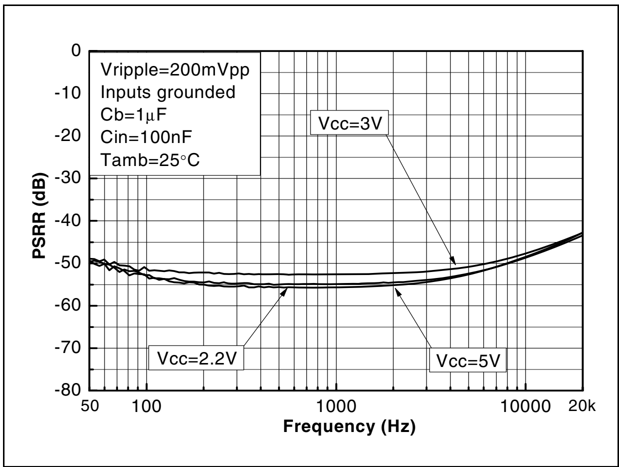


Figure 17. Equivalent input noise voltage density

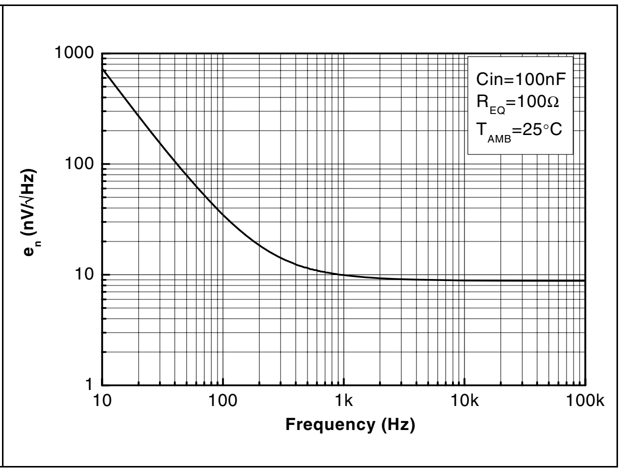


Figure 18. Δgain vs. power supply voltage

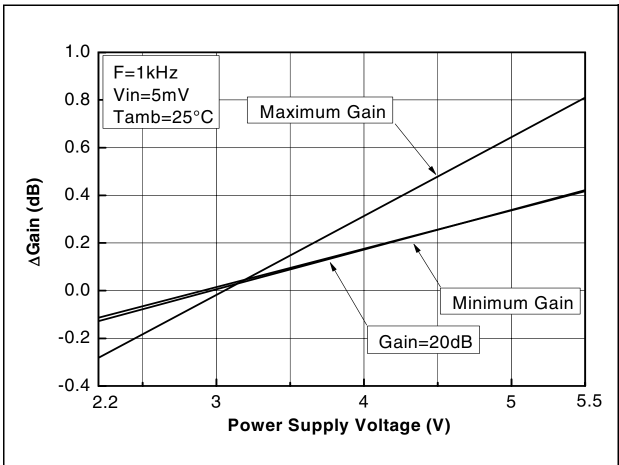


Figure 19. Δgain vs. ambient temperature

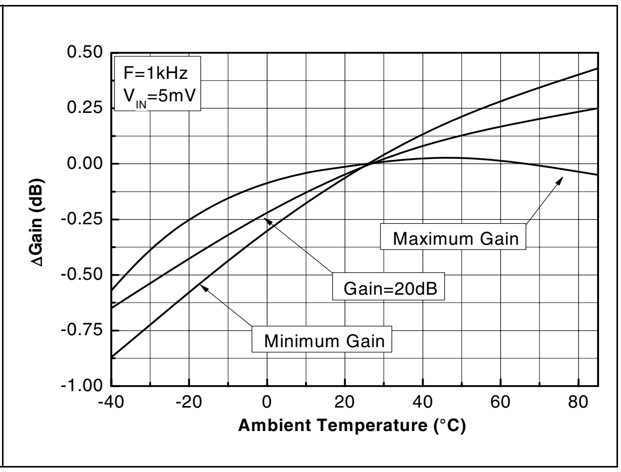


Figure 20. Maximum input voltage vs. gain, THD+N<1%

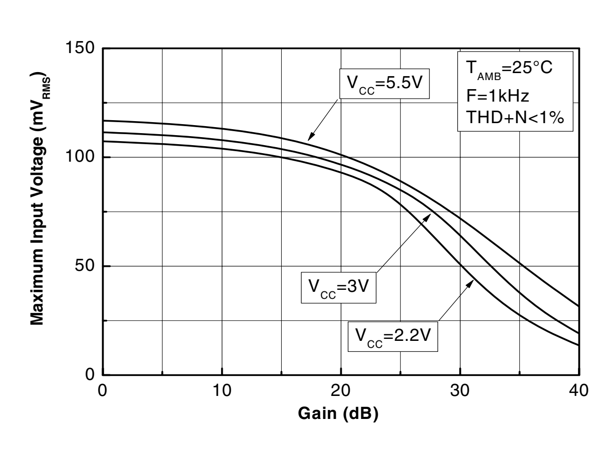


Figure 21. Maximum input voltage vs. power supply voltage, THD+N<1%

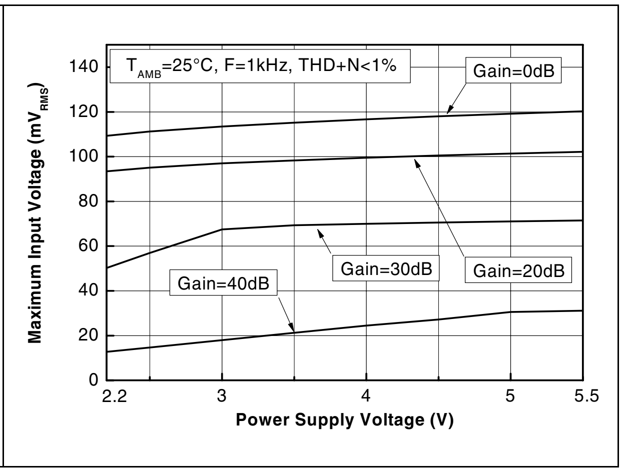


Figure 22. THD+N vs. input voltage

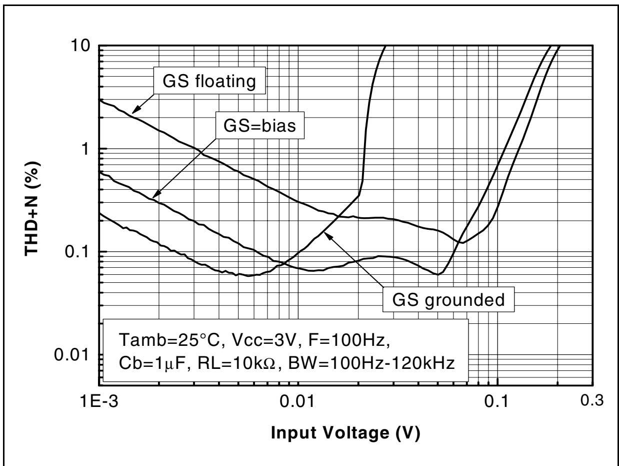


Figure 23. THD+N vs. input voltage

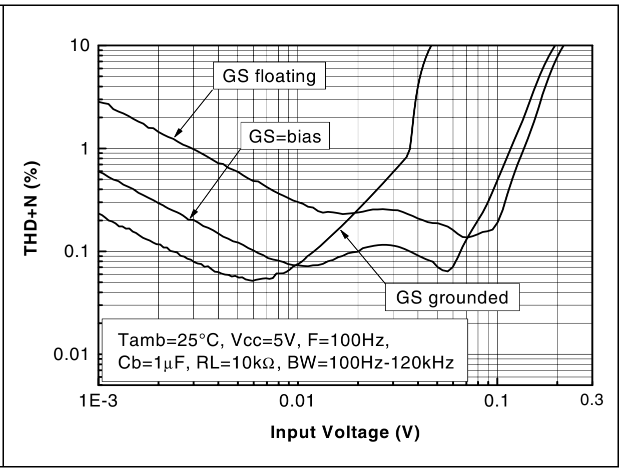


Figure 24. THD+N vs. input voltage

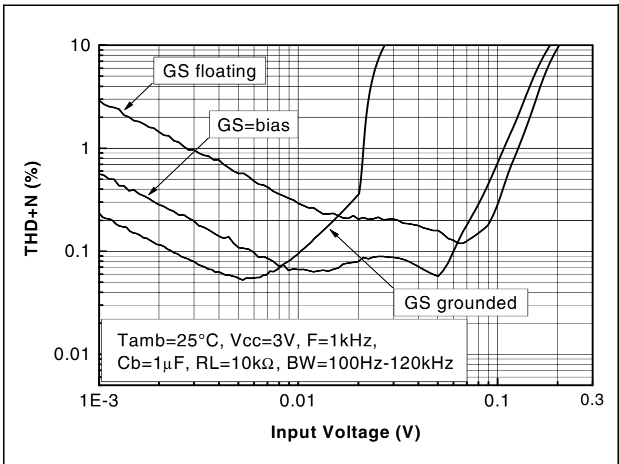


Figure 25. THD+N vs. input voltage

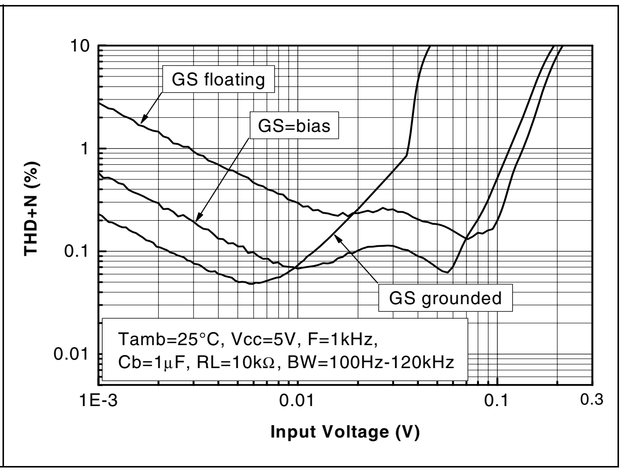


Figure 26. THD+N vs. input voltage

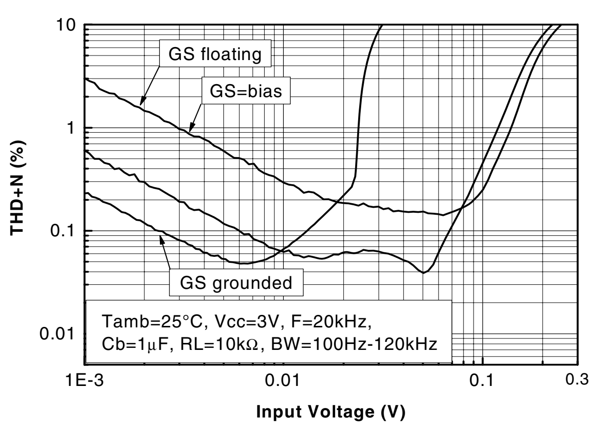


Figure 27. THD+N vs. input voltage

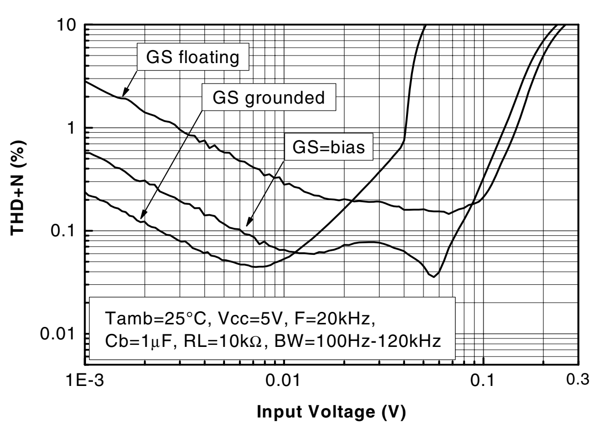


Figure 28. THD+N vs. frequency

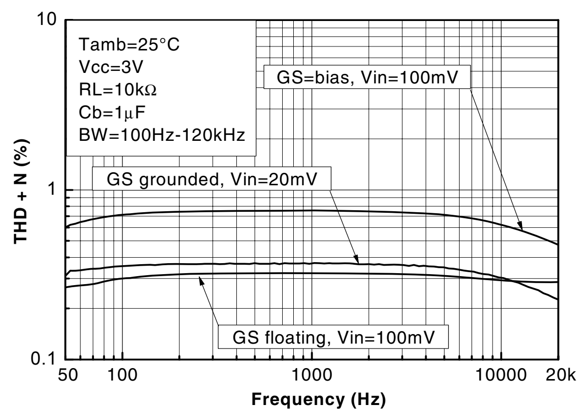


Figure 29. THD+N vs. frequency

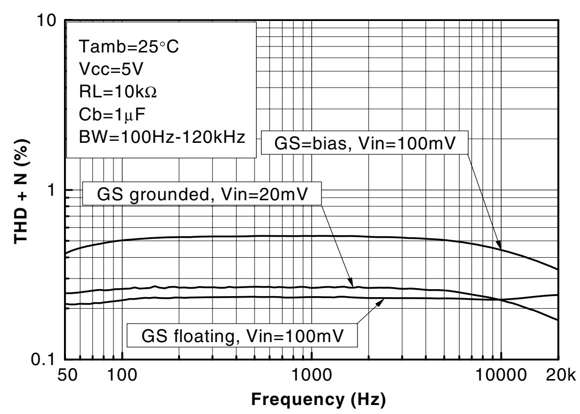


Figure 30. Transient response

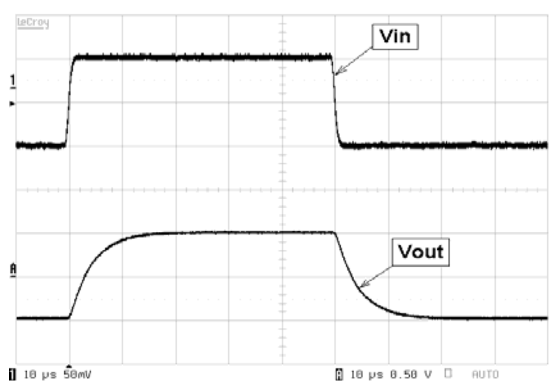
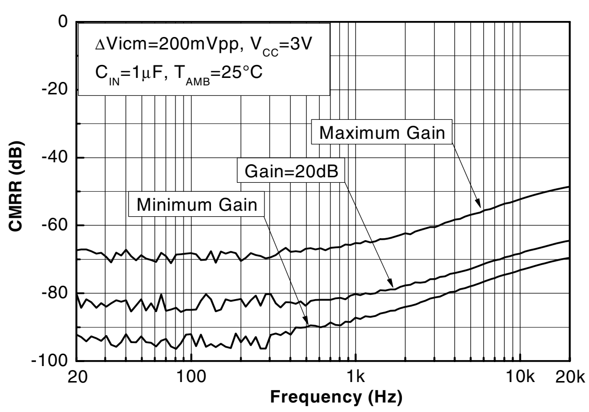


Figure 31. Common mode rejection ratio (CMRR) vs frequency



4 Application information

4.1 Differential configuration principle

The TS472 is a fully-differential input/output microphone preamplifier. The TS472 also includes a common-mode feedback loop that controls the output bias value to average it at $V_{CC}/2$. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the input dynamic voltage range.

The **advantages** of a fully-differential amplifier are:

- Very high PSRR (power supply rejection ratio).
- High common mode noise rejection.
- In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. However, to reach maximum performance in all tolerance situations, it is better to keep this option.

4.2 Higher cut-off frequency

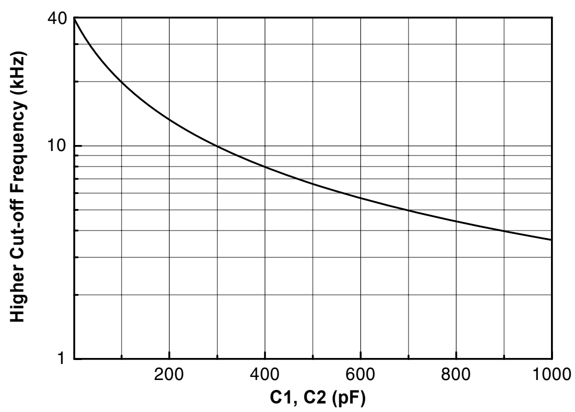
The higher cut-off frequency F_{CH} of the microphone preamplifier depends on the external capacitors C_1, C_2.

TS472 has an internal first order low-pass filter (R = 40 kΩ, C = 100 pF) to limit the highest cut-off frequency on 40 kHz (with a 3 dB attenuation). By connecting C_1, C_2 you can decrease F_{CH} by applying the following formula.

$$F_{CH} = \frac{1}{2\pi \cdot 40\times 10^3 \cdot (C_{1,2} + 100\times 10^{-12})}$$

Figure 32 represents the higher cut-off frequency in Hz versus the value of the output capacitors C_1, C_2 in nF.

Figure 32. Higher cut-off frequency vs. output capacitors



For example, F_{CH} is almost 20 kHz with $C_{1,2}$ = 100 pF.

4.3 Lower cut-off frequency

The lower cut-off frequency F_{CL} of the microphone preamplifier depends on the input capacitors C_{in} and output capacitors C_{out}. These input and output capacitors are mandatory in an application because of DC voltage blocking.

The input capacitors C_{in} in series with the input impedance of the TS472 (100 kΩ) are equivalent to a first order high-pass filter. Assuming that F_{CL} is the lowest frequency to be amplified (with a 3 dB attenuation), the minimum value of C_{in} is:

$$C_{in} = \frac{1}{2\pi \cdot F_{CL} \cdot 100 \times 10^3}$$

The capacitors C_{out} in series with the output resistors R_{out} (or an input impedance of the next stage) are also equivalent to a first order high-pass filter. Assuming that F_{CL} is the lowest frequency to be amplified (with a 3 dB attenuation), the minimum value of C_{out} is:

$$C_{out} = \frac{1}{2\pi \cdot F_{CL} \cdot R_{out}}$$

Figure 33. Lower cut-off frequency vs. input capacitors

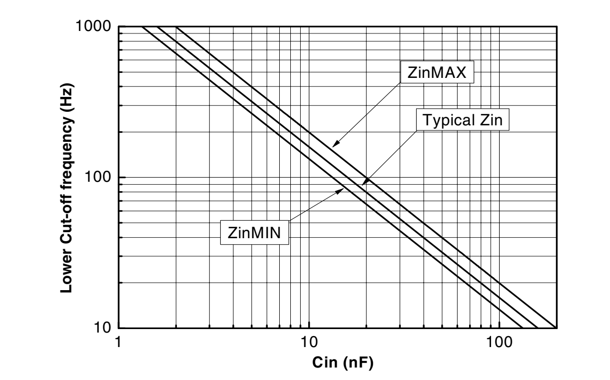


Figure 34. Lower cut-off frequency vs. output capacitors

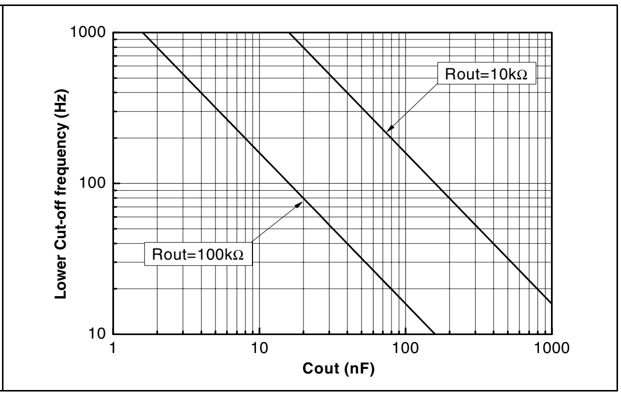


Figure 33 and *Figure 34* give directly the lower cut-off frequency (with 3 dB attenuation) versus the value of the input or output capacitors.

Note: If F_{CL} is kept the same for calculation purposes, take into account that the 1st order high-pass filter on the input and the 1st order high-pass filter on the output create a 2nd order high-pass filter in the audio signal path with an attenuation of 6 dB on F_{CL} and a roll-off of 40 dB/decade.

4.4 Low-noise microphone bias source

The TS472 provides a very low noise voltage and power supply rejection BIAS source designed for biasing an electret condenser microphone cartridge. The BIAS output is typically set at 2.0 V_{DC} (no load conditions), and can typically source 2 mA with respect to drop-out, determined by the internal 100 Ω resistance (for detailed load regulation curves see *Figure 8*).

4.5 Gain settings

The gain in the application depends mainly on:

- the sensitivity of the microphone,
- the distance to the microphone,
- the audio level of the sound,
- the desired output level.

The sensitivity of the microphone is generally expressed in dB/Pa, referenced to 1 V/Pa. For example, the microphone used in testing had an output voltage of 6.3 mV for a sound pressure of 1 Pa (where Pa is the pressure unit, Pascal). Expressed in dB, the sensitivity is:

20Log(0.0063) = -44 dB/Pa

To facilitate the first approach, *Table 10* gives voltages and gains used with a low-cost omni-directional electret condenser microphone of -44 dB/Pa.

Table 10. Typical TS472 gain vs. distance to the microphone (sensitivity -44 dB/Pa)

Distance to microphone	Microphone output voltage	TS472 gain
1 cm	30 mV_{RMS}	20
20 cm	3 mV_{RMS}	100

The gain of the TS472 microphone preamplifier can be set as follows.

1. From -1.5 dB to 41 dB by connecting an external grounded resistor R_{GS} to the GS pin. This enables the gain to be adapted more precisely to each application.

Table 11. Selected gain vs. gain select resistor

Gain (dB)	0	10	20	30	40
R_{GS} (Ω)	470k	27k	4k7	1k	68

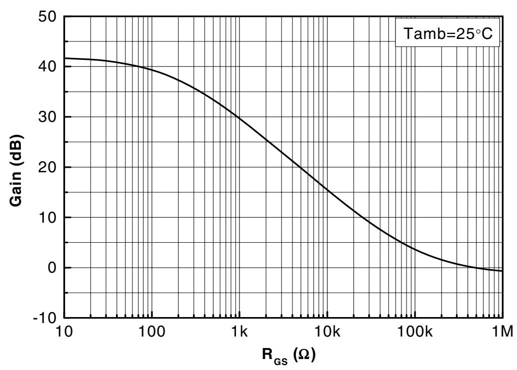


Figure 35. Gain in dB vs. gain select resistor

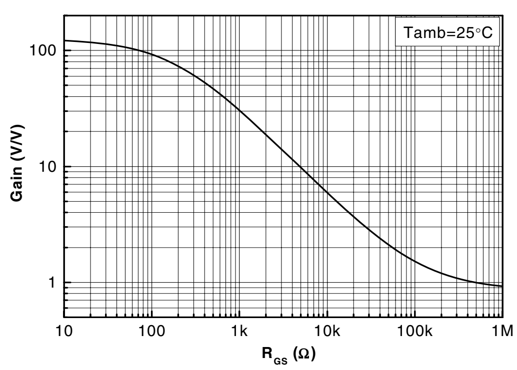
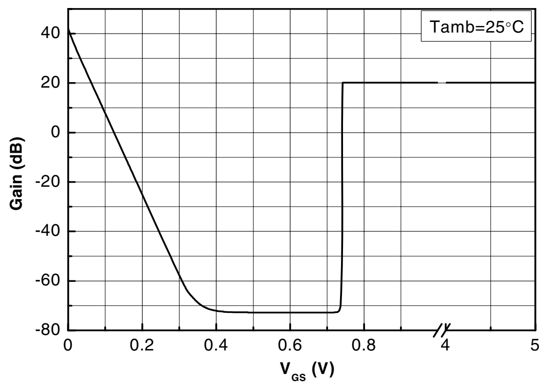


Figure 36. Gain in V/V vs. gain select resistor

2. To 20 dB by applying $V_{GS} > 1V_{DC}$ on the gain select (GS) pin. This setting can help to reduce a number of external components in an application, because 2.0 V_{DC} is provided by the TS472 itself on the BIAS pin.

Figure 37 gives other values of the gain vs. voltage applied on the GS pin.

Figure 37. Gain vs. gain select voltage



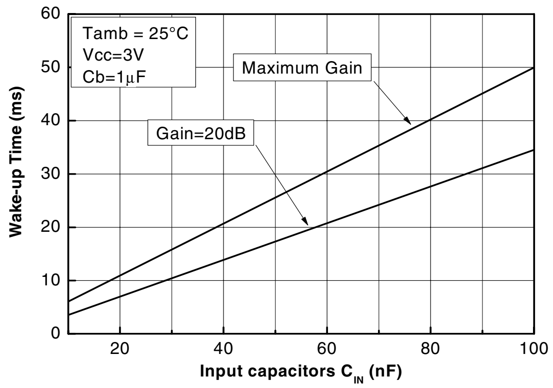
Note: In the case of a single-ended output configuration (either positive or negative output is used for the following signal processing) the overall gain is half. One must also take into account that all advantages of the differential configuration principles are lost (see the difference in PSRR in Table 5).

4.6 Wake-up time

When the standby mode is released to switch the device to ON, a signal appears on the output a few microseconds later, and the bypass capacitor C_b is charged within a few milliseconds. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct.

In a typical application, when a biased microphone is connected to the differential input via the input capacitors (C_{in}), (and the output signal is in line with the specification), the wake-up time will depend upon the values of the input capacitors C_{in} and the gain. When the gain is lower than 0 dB, the wake-up time is determined only by the bypass capacitor C_b, as described above. For a gain superior to 0 dB, refer to *Figure 38*.

Figure 38. Wake-up time in a typical application vs. input capacitors



4.7 Standby mode

When the standby command is set, it takes a few microseconds to set the output stages (differential outputs and 2.0 V bias output) to high impedance and the internal circuitry to shutdown mode.

4.8 Layout considerations

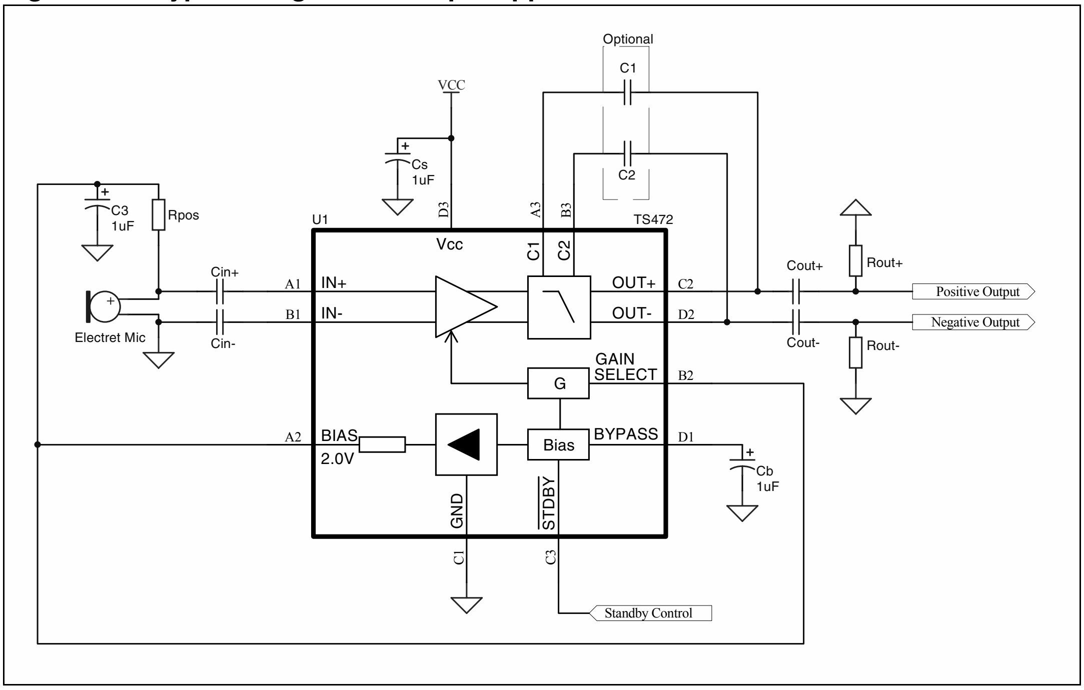
The TS472 has sensitive pins to connect C1, C2 and Rgs. To obtain high power supply rejection and low noise performance, it is mandatory that the layout track to these components be as short as possible.

Decoupling capacitors on V_{CC} and bypass pin are needed to eliminate power supply drops. In addition, the capacitor location for the dedicated pin should be as close to the device as possible.

4.9 Single-ended input configuration

It is possible to use the TS472 in a single-ended input configuration. The schematic in *Figure 39* provides an example of this type of configuration.

Figure 39. Typical single-ended input application



4.10 Demonstration board

A demonstration board for the TS472 is available. For more information about this demonstration board, refer to **application note AN2240** on **www.st.com.**

Figure 40. PCB top layer

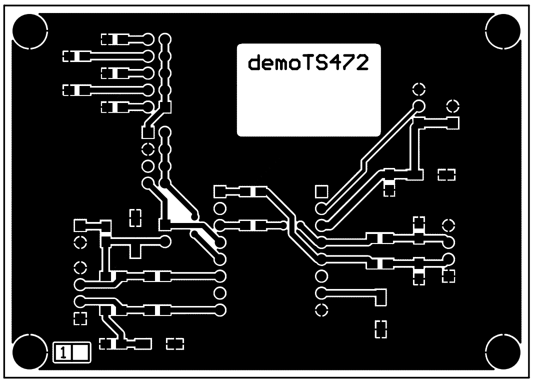


Figure 41. PCB bottom layer

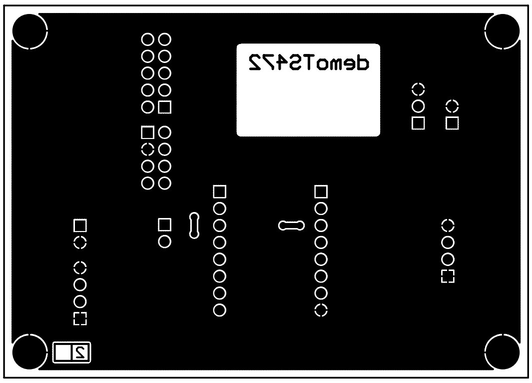
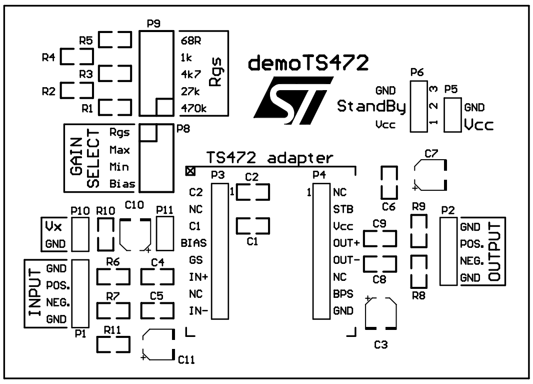


Figure 42. Component location



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 Flip-chip package information

Figure 43. TS472 footprint recommendation

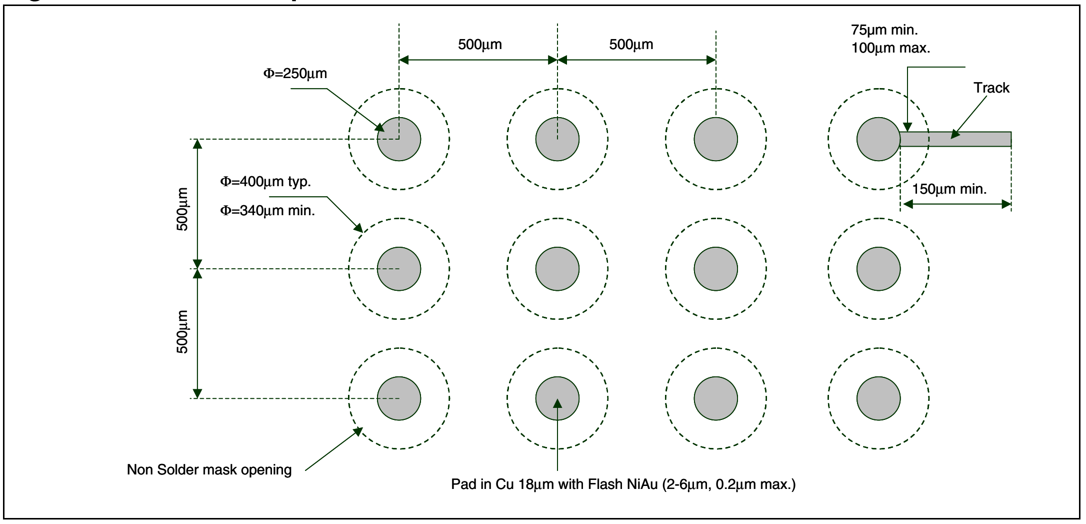


Figure 44. Pinout (top view)

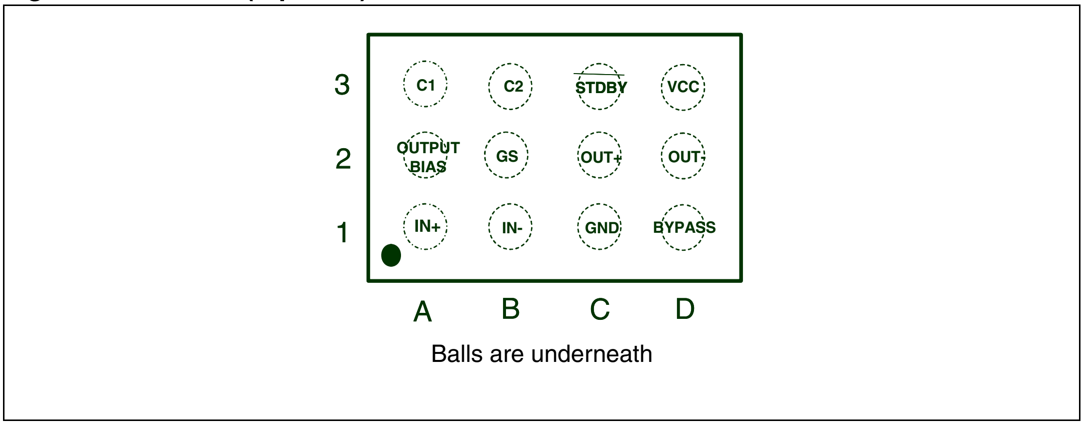


Figure 45. Marking (top view)

- ST logo
- Part number: 472
- E Lead free bumps
- Three digits datecode: YWW
- The dot indicates pin A1

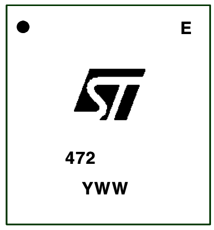
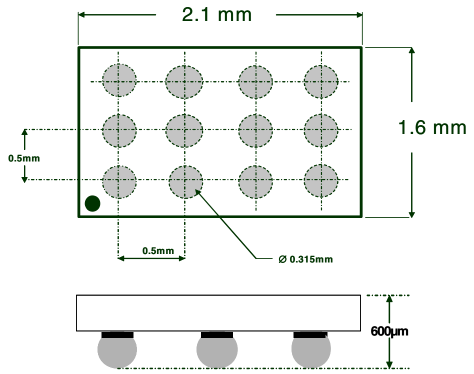
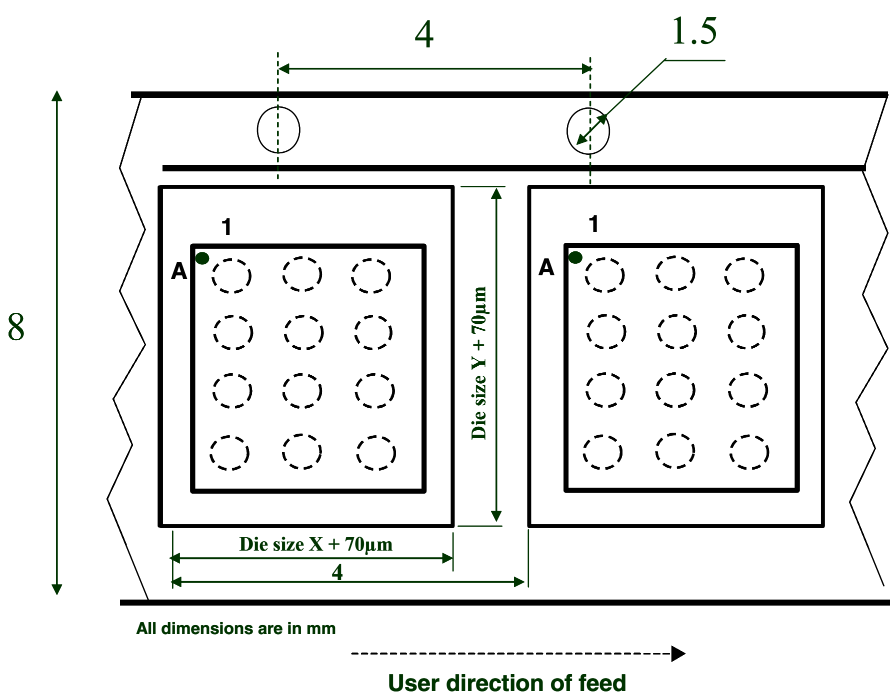


Figure 46. Flip-chip - 12 bumps



- Die size: **2.1 mm x 1.6 mm** ± 30 µm
- Die height (including bumps): **600 µm**
- Bumps diameter: **315 µm** ±50 µm
- Bump diameter before reflow: **300 µm** ±10 µm
- Bump height: **250 µm** ±40 µm
- Die height: **350 µm** ±20 µm
- Pitch: **500 µm** ±50 µm
- Coplanarity: **50 µm max**

Figure 47. Tape & reel specification (top view)



5.2 QFN24 package information

Figure 48. QFN24 package mechanical drawing

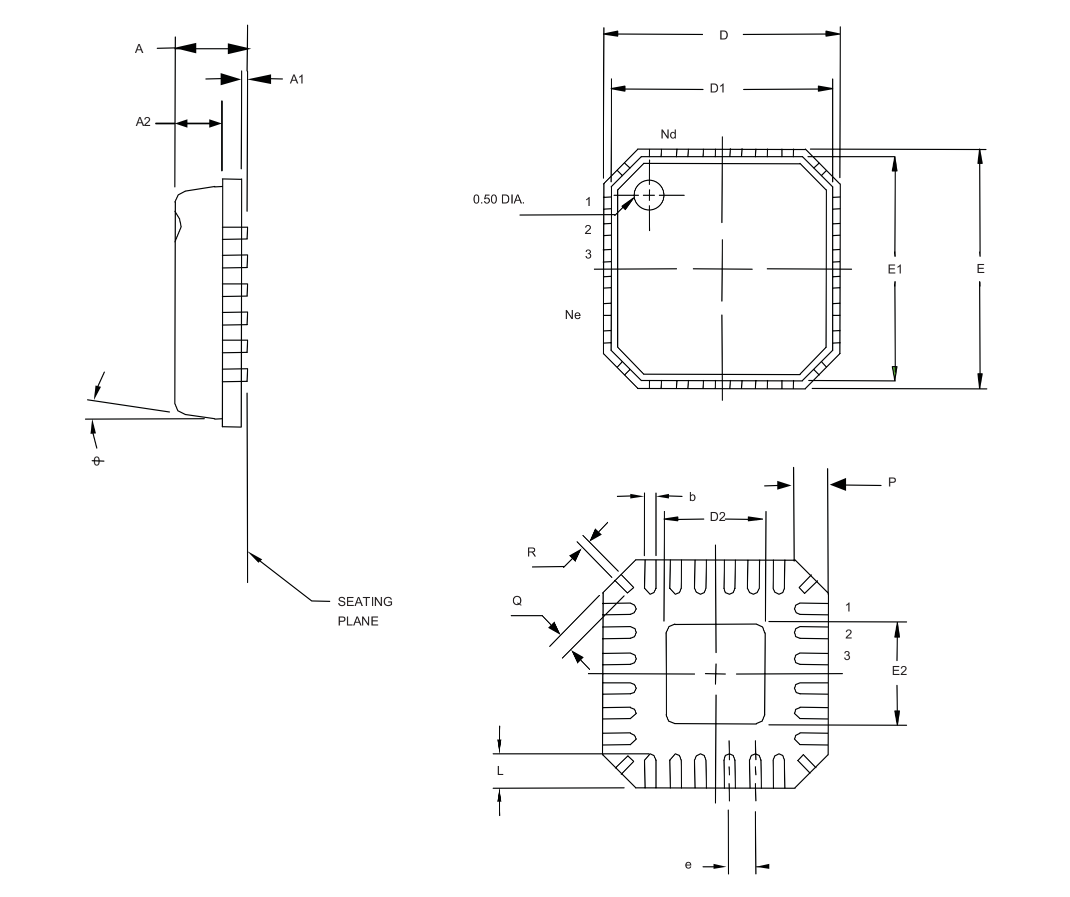


Table 12. QFN24 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.031		0.040
A1			0.05			0.002
A2		0.65	0.80		0.026	0.031
D		4.00			0.158	
D1		3.75			0.148	
E		4.00			0.158	
E1		3.75			0.148	
P	0.24	0.42	0.60	0.009	0.017	0.024
R	0.13	0.17	0.23	0.005	0.007	0.009
e		0.50			0.020	
N		24.00			0.945	
Nd		6.00			0.236	
Ne		6.00			0.236	
L	0.30	0.40	0.50	0.012	0.016	0.020
b	0.18		0.30	0.007		0.012
Q		0.20	0.45		0.008	0.018
D2	1.95	2.10	2.25	0.077	0.083	0.089
E2	1.95	2.10	2.25	0.077	0.083	0.089
Ø			12°			

6 Ordering information

Table 13. Order codes

Order code	Temperature range	Package	Packing	Marking
TS472EIJT	-40°C, +85°C	Flip-chip	Tape & reel	472
TS472IQT	-40°C, +85°C	QFN24 4x4mm	Tape & reel	K472

7 Revision history

Table 14. Document revision history

Date	Revision	Changes
01-Jul-05	1	Initial release corresponding to product preview version.
01-Oct-05	2	First release of fully mature product datasheet.
01-Dec-05	3	Added single-ended input operation in *Section 4: Application information*.
12-Sep-2006	4	Added QFN package information. Updated curves, added new ones in *Section 3: Electrical characteristics*.
02-Mar-2009	5	Corrected error on C1 and C2 caps. Added *Table 2: Pin descriptions*. Updated QFN24 package information in *Section 5.2*.
25-Aug-2009	6	Corrected QFN package pinout on cover page.