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National Semiconductor

October 16, 2009

ADC12EU050

Ultra-Low Power, Octal, 12-bit, 40-50 MSPS Sigma-Delta Analog-to-Digital Converter

General Description

The ADC12EU050 is a 12-bit, ultra-low power, octal A/D converter for use in high performance analog to digital applications. The ADC12EU050 uses an innovative continuous time sigma delta architecture offering ultra low power consumption and an alias free sample bandwidth up to 25MHz. The input stage of each channel features a proprietary system to ensure instantaneous recovery from overdrive. Instant overload recovery (IOR) with no memory effect guarantees the elimination of phase errors resulting from out of range input signals. The ADC12EU050 reduces interconnection complexity by using programmable serialized outputs which offer the industry standard LVDS and SLVS modes. Power consumption of only 48mW per channel @ 50MSPS gives a total chip power consumption of 384mW. The ADC12EU050 can operate entirely from a 1.2V supply, although a separate output driver supply of up to 1.8V can be used. The device operates from -40 to +85 °C and is supplied in a 10 x 10 mm^2, 68 pin package.

Features

- Xignal™ CT∑Δ ADC technology
- 40-50MSPS sampling rate
- Anti-alias filter free Nyquist sample range
- Unique Instant Overload Recovery (IOR)
- Wide 2.10 V_{PP} input range
- 1.2V supply voltage
- Integrated precision LC PLL
- Serial control via SPI compatible interface

Key Specifications

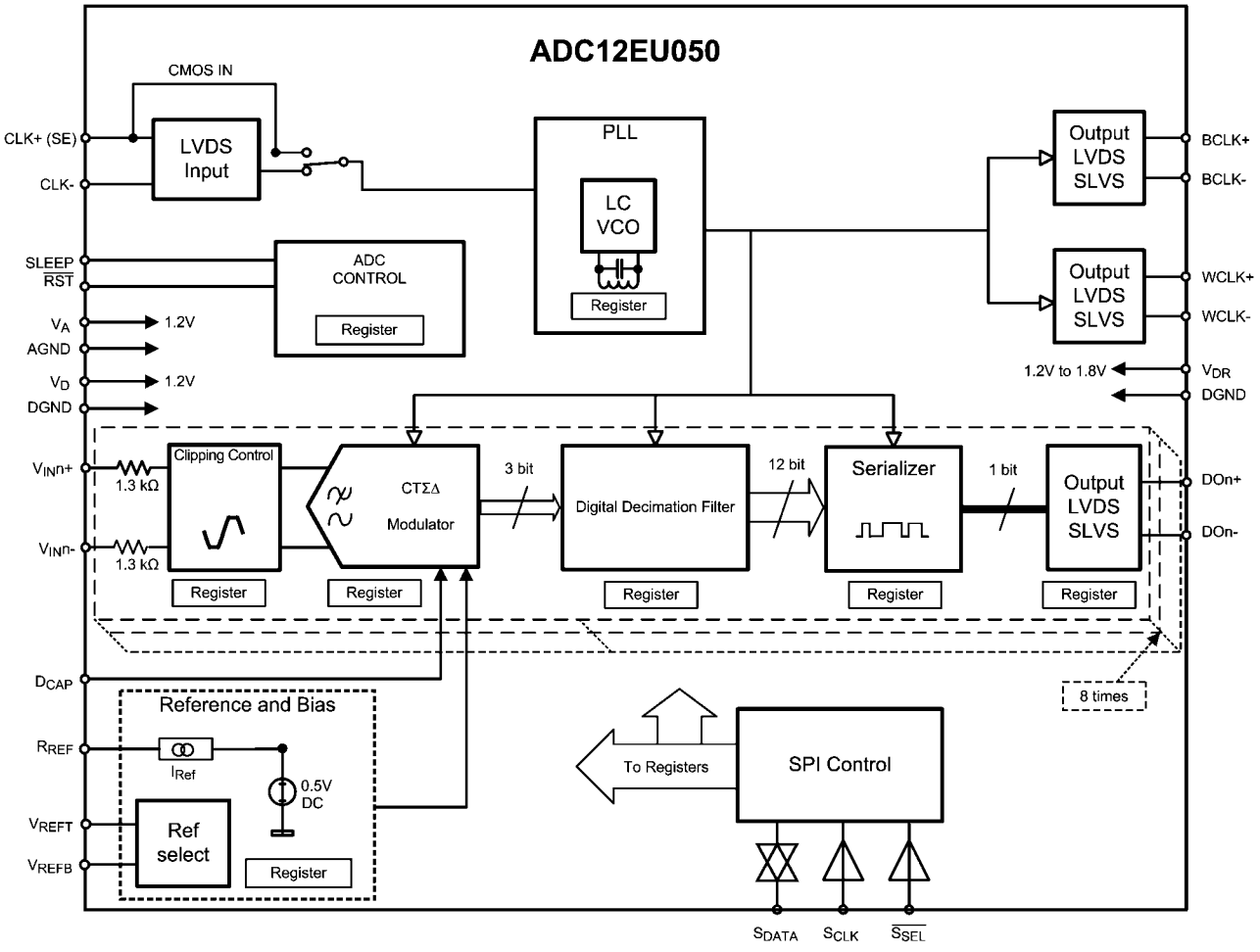
■ Resolution	12 Bits
■ Conversion Rate	40 to 50 MSPS
■ SNR	69.3 dBFS (typ) @ 50 MSPS, f_{IN} = 4.4MHz
■ THD	–76.6 dB (typ) @ 50 MSPS, f_{IN} = 4.4MHz
■ Per Channel Power	48 mW/ch (typ) @ 50MSPS
■ Total Active Power	385 mW (typ) @ 50MSPS
■ Inter-Channel Isolation	>110 dB @ f_{IN} = 4.4MHz
■ Operating Temp. Range	-40 to +85 °C

Applications

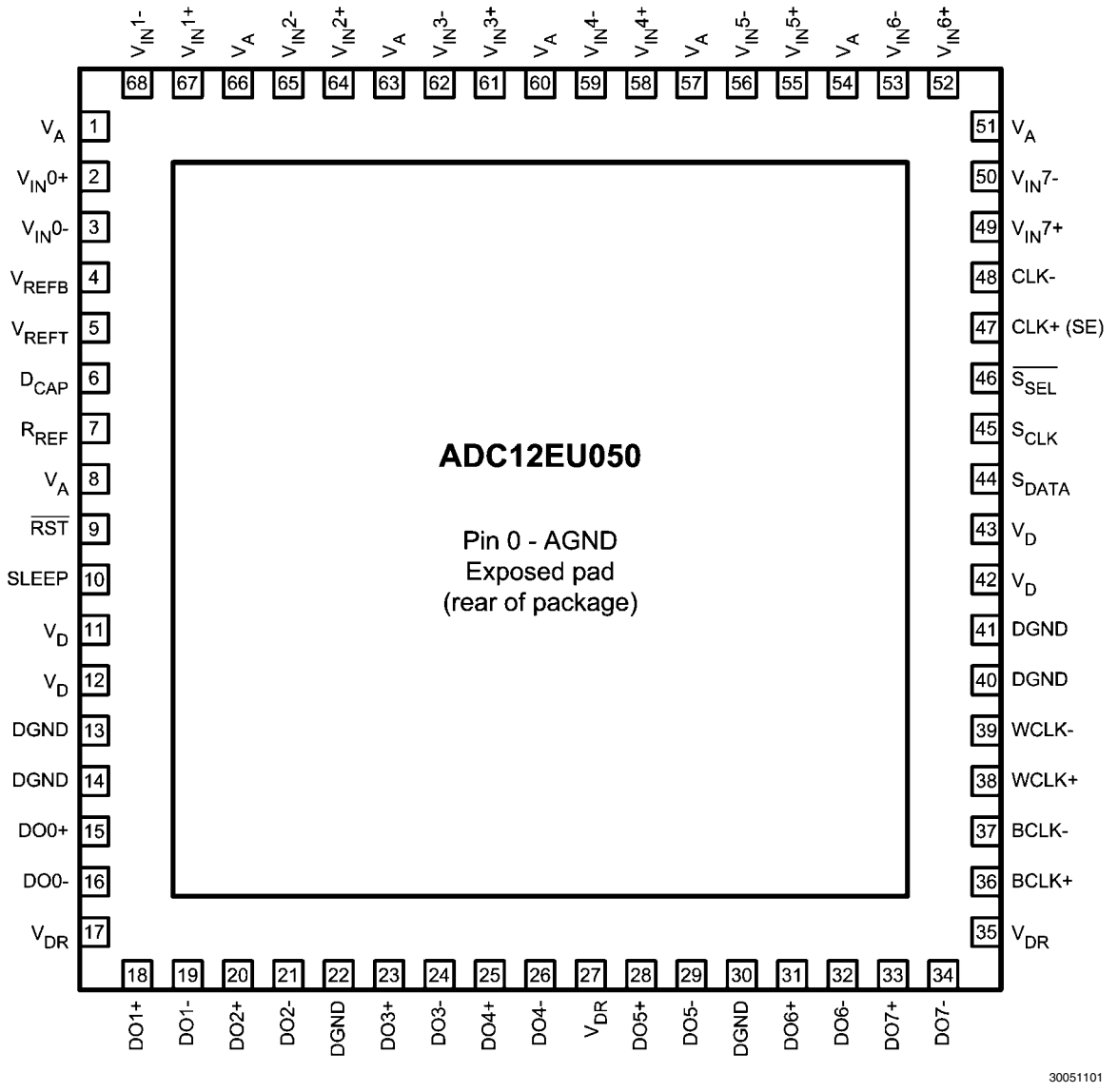
- Medical imaging, ultrasound
- Industrial ultrasound, such as non-destructive testing
- Communications
- Battery powered portable systems

ADC12EU050 Ultra-Low Power, Octal, 12-bit, 40-50 MSPS Sigma-Delta Analog-to-Digital Converter

Block Diagram



Connection Diagram



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Ordering Information

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC12EU050CIPLQ	68 Pin LLP
ADC12EU050EB	Evaluation Board

Pin Descriptions

Pin No.	Name	Type	Function and Connection
ANALOG I/O			
2 3 67 68 64 65 61 62 58 59 55 56 52 53 49 50	$V_{IN}0+$ $V_{IN}0-$ $V_{IN}1+$ $V_{IN}1-$ $V_{IN}2+$ $V_{IN}2-$ $V_{IN}3+$ $V_{IN}3-$ $V_{IN}4+$ $V_{IN}4-$ $V_{IN}5+$ $V_{IN}5-$ $V_{IN}6+$ $V_{IN}6-$ $V_{IN}7+$ $V_{IN}7-$	Input	Differential analog inputs to the ADC, for channels 0 to 7. The negative input pin may be connected via a capacitor to AGND or the inputs may be transformer coupled for single ended operation. Differential inputs are recommended for best performance.
4	V_{REFB}		Optional negative reference voltage to improve multi-channel ADC matching. This pin must be connected to AGND.
5	V_{REFT}		Optional positive reference voltage to improve multi-channel ADC matching. If using the internal reference, this pin should be left tied to AGND through a 100nF capacitor. If using an external reference voltage, this pin should be connected to the positive reference voltage, which must lie in the range specified in the Electrical Characteristics table.
6	D_{CAP}	Input	This pin provides the capacitance for the low pass filter in the modulator's DAC. It must be connected to AGND through a minimum 100nF capacitor. It is possible to decrease the noise close to the carrier by increasing this capacitor, up to a maximum of 10µF. See Applications Information for further information on the selection of this capacitor.
7	R_{REF}	Input/Output	External bias reference resistor. This pin must always be connected to AGND through a resistor, whether the internal reference or an external reference voltage is used. The resistor value must be 10kΩ ±1%.
DIGITAL I/O			
9	$\overline{RST}$	Input	This pin is an active low reset for the entire ADC, both analog and digital components. The pin must be held low for 500ns then returned to high in order to ensure that the chip is reset correctly.
10	SLEEP	Input	Sleep mode. Toggling this pin to high will cause the ADC to enter the low power sleep mode. When the pin is returned to low, the chip will, after the specified time to exit sleep mode, return to normal operation.

Pin No.	Name	Type	Function and Connection
15 16 18 19 20 21 23 24 25 26 28 29 31 32 33 34	DO0+ DO0- DO1+ DO1- DO2+ DO2- DO3+ DO3- DO4+ DO4- DO5+ DO5- DO6+ DO6- DO7+ DO7-	Output	Differential Serial Outputs for channels 0 to 7. Each pair of outputs provides the serial output for the specific channel. The default output is reduced common mode LVDS format, but by programming the appropriate control registers, the output format can be changed to SLVS or LVDS. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100 ohm resistors.
36 37	BCLK+ BCLK-	Output	Bit clock. Differential output clock used for sampling the serial outputs. Information on timing can be seen in the Electrical Specifications section of the datasheet. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100 ohm resistors.
38 39	WCLK+ WCLK-	Output	Word Clock. Differential output frame clock. Information on timing can be seen in the Electrical Specifications section of the datasheet. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100 ohm resistors.
44	S_{DATA}	Input/Output	SPI data input and output. This pin is used to send and receive SPI address and data information. The direction of the pin is controlled internally by the ADC based on the SPI protocol.
45	S_{CLK}	Input	SPI clock. In order to use the SPI interface, a clock must be provided on this pin. See Electrical Specifications for SPI clock and timing information.
46	$\overline{S_{SEL}}$	Input	SPI chip select. This active low pin is used to enable the serial interface.
47 48	CLK+ (SE) CLK-	Input	Differential Input Clock. The input clock must lie in the range of 40MHz to 50MHz. It is used by the PLL to generate the internal sampling clocks. A single ended clock can also be used, and should be connected to pin 47.
POWER SUPPLY			
1, 8, 51, 54, 57, 60, 63, 66	V_A	Power	Analog Power Supply. All pins should be connected to the same 1.2V supply, with voltage limits as in the Electrical Specification.
0	AGND	Ground	Analog Ground Return.
11, 12, 42, 43	V_D	Power	Digital Power Supply. Connect to 1.2V, with voltage limits as in the Electrical Specification.
13, 14, 22, 30, 40, 41	DGND	Ground	Digital and Output Driver Ground Return.
17, 27, 35	V_{DR}	Power	Output Driver Power Supply. Can be connected to 1.2V – 1.8V, depending on application requirements. Voltage limits are described in more detail in the Electrical Specification.

Absolute Maximum Ratings (Note 1, Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_D)	−0.3V to 1.4V
IO Supply Voltage (V_{DR})	-0.3 to 2.0V
Voltage at Analog Inputs	-0.3 to 1.4V
Voltage at SPI Inputs	-0.3 to 2.5V
Input Current, V_{IN}+, V_{IN}-	±1mA
Input Current, other pins	±10mA
ESD Susceptibility	
Human Body Model	2000V
Machine Model	200V
Charged Device Mode	1,000V
Soldering Temperature	
Infrared, 10 seconds	235°C
Storage Temperature Range	−65°C to +125°C

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging.

Operating Ratings (Note 2, Note 3)

Operating Temperature Range	−40°C to +85°C
Supply Voltage (V_A=V_D)	+1.14 to +1.26V
IO Supply Voltage (V_{DR})	+1.14 to +1.89V
Minimum rise time on V_A, V_D, V_{DR} at power-up	40µs
Analog Inputs (V_{IN}N+, V_{IN}N-)	-0.10 to V_A
SPI Inputs (S_{DATA}, S_{SEL}, S_{CLK})	+1.14 to +2.50V
V_{REFT} (When using external reference)	475mV to 525mV
V_{REFB}	AGND
V_{CM} Input Common Mode Range (Differential Input)	0.4V to 1.2V
Ground Difference |AGND-DGND|	<50mV

Electrical Characteristics

Unless otherwise specified, the following conditions apply: V_A = V_D = 1.2V; V_{DR} = 1.2V; V_{REF} = internal; R_{REF} = 10kohm ±1%; C_L = 5pF; 100Ω terminated at the receiver; f_{CLK} = 50MHz; f_S = 50MSPS. **Boldface limits** apply for T_A = T_{MIN} to T_{MAX}; All other limits apply for T_A = +25°C.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits	Units
Static Converter Characteristics					
	Resolution (No missing codes guaranteed)			**12**	Bits
INL	Integral Non Linearity		±0.75	**±3.0**	LSB
DNL	Differential Non Linearity		±0.35	**±0.75**	LSB
PSE	Positive Full Scale Error		±0.66	**±3**	%FS
NSE	Negative Full Scale Error		±0.58	**±3**	%FS
GE	Gain Error		±1.23		%FS
Dynamic Converter Characteristics – Instant Overload Recovery (IOR) Off					
SNR	Signal to Noise Ratio(Note 5)	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	69.3	**67.0**	dBFS (min)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	69.0		dBFS
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	69.9		dBFS
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	69.6		dBFS
SINAD	Signal to Noise and Distortion(Note 5)	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	68.5	**62.5**	dBFS (min)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	68.5		dBFS
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	69.3		dBFS
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	69.2		dBFS
ENOB	Effective Number of Bits	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	11.1	**10.1**	Bits (min)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	11.1		Bits
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	11.2		Bits
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	11.2		Bits
THD	Total Harmonic Distortion	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-76	**-65**	dBc (max)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-78		dBc
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-77		dBc
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-79		dBc

Symbol	Parameter	Conditions	Typical (Note 4)	Limits	Units
H2	Second Harmonic Distortion	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-81	**-66**	dBc (max)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-79		dBc
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-82		dBc
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-80		dBc
H3	Third Harmonic Distortion	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-83	**-67**	dBc (max)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-97		dBc
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-84		dBc
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-108		dBc
SFDR	Spurious Free Dynamic Range	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	77	**66**	dBc (min)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	78		dBc
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	78		dBc
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	79		dBc
IMD	Intermodulation Distortion	f_1 = 9.6MHz, V_{IN} = -6dBFS f_2 = 10.1MHz, V_{IN} = -6dBFS	-70		dBFS
Dynamic Converter Characteristics – Instant Overload Recovery (IOR) On					
SNR	Signal-to-Noise Ratio(Note 5)	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	67.6	**65.5**	dBFS (min)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	67.4		dBFS
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	68.4		dBFS
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	68.2		dBFS
SINAD	Signal-to-Noise and Distortion(Note 5)	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	67.0	**61.5**	dBFS (min)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	67.0		dBFS
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	67.9		dBFS
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	67.8		dBFS
ENOB	Effective Number of Bits	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	10.8	**9.9**	Bits (min)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	10.8		Bits
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	11.0		Bits
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	11.0		Bits
THD	Total Harmonic Disortion	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-76	**-64**	dBc (max)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-77		dBc
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-77		dBc
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-78		dBc
H2	Second Harmonic Distortion	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-80	**-65**	dBc (max)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-78		dBc
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-81		dBc
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-79		dBc
H3	Third Harmonic Distortion	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-83	**-67**	dBc (max)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-96		dBc
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	-85		dBc
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	-107		dBc
SFDR	Spurious Free Dynamic Range	f_{CLK} = 50MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	76	**65**	dBc (min)
		f_{CLK} = 50MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	77		dBc
		f_{CLK} = 40MHz, f_{IN} = 4.4MHz, V_{IN} = -0.5dBFS	78		dBc
		f_{CLK} = 40MHz, f_{IN} = 9.5MHz, V_{IN} = -0.5dBFS	78		dBc
IMD	Intermodulation Distortion	f_1 = 9.6MHz, V_{IN} = -6dBFS f_2 = 10.1MHz, V_{IN} = -6dBFS	-70		dBFS

Symbol	Parameter	Conditions	Typical (Note 4)	Limits	Units
Inter-channel Characteristics					
	Channel to channel gain match		±0.1	**±0.5**	dB
	Inter-channel Isolation	f_{IN} = 4.4MHz @ -0.1dBFS Adjacent channel terminated	110		dB
Reference And Analog Input Characteristics					
V_{IN}	Full Scale Analog Input Voltage	IOR mode off	2.10		V_{PP}
		IOR mode on	1.56		V_{PP}
	Maximum Input for Instantaneous Recovery from Overload	IOR mode on, f_{IN} < 12MHz		2.75	V_{PP} (max)
R_{IN}	Differential Input Impedance		2.61	**2.4** **2.8**	kΩ (min) kΩ (max)
V_{CM}	Internal Input Common Mode	Generated internally	605	**574** **637**	mV (min) mv (max)
	Input Impedance of V_{Reft}		20		kΩ
V_{REFOUT}	Internal Reference Voltage	Generated internally	502	**480** **520**	mV (min) mV (max)
Power Characteristics					
I_A	Analog Supply Current	f_{CLK} = 50 MHz	152	**163**	mA (max)
I_D	Digital Supply Current	f_{CLK} = 50 MHz	130	**147**	mA (max)
I_{DR}	Output Driver Supply Current	LVDS, V_{DR} = 1.8V, f_{CLK} = 50 MHz	38	**45**	mA (max)
	Power consumption	f_{CLK} = 50 MHz, Equalizer off	385	**412**	mW (max)
		f_{CLK} = 50 MHz, Equalizer on	435	**470**	mW (max)
		f_{CLK} = 40 MHz, Equalizer off	343		mW
		f_{CLK} = 40 MHz, Equalizer on	383		mW
		Sleep	40	**50**	mW (max)
		Power Down	5	**15**	mW (max)
	Per channel power consumption	f_{CLK} = 50 MHz, Equalizer off	48		mW
		f_{CLK} = 40 MHz, Equalizer off	43		mW
PSRR	Power supply rejection ratio	100mV, 100kHz to 1MHz sinusoid on V_A	65		dB
CMRR	Common mode rejection ratio	100mV, 1MHz sinusoid on V_{IN}+ and V_{IN}-	60		dB
	Recovery time from sleep			12	µs (max)
	Recovery time from power down			18	ms (max)
	Recovery time from single channel power down			6	µs (max)

Digital Decimation Filter Characteristics

Unless otherwise specified, the following conditions apply: $V_A = V_D = 1.2V$; $V_{DR} = 1.2V$; V_{REF} = internal; R_{REF} = 10kohm ±1%; C_L = 5pF; 100Ω terminated at the receiver; f_{CLK} = 50MHz; f_S = 50MSPS. **Boldface limits** apply for $T_A = T_{MIN}$ to T_{MAX}; All other limits apply for T_A = +25°C.

Symbol	Parameter	Conditions(Note 6)	Typical (Note 4)	Limits	Units
	Pass Band	f_{CLK} = 50MHz	22		MHz
		f_{CLK} = 40MHz	17.6		MHz
	Pass Band Transition	f_{CLK} = 50MHz, -3dB attenuation	25		MHz
		f_{CLK} = 40MHz, -3dB attenuation	20		MHz
	Pass Band Ripple	f_{IN} < 22MHz		**±0.01**	dB
	Stop Band Begin	f_{CLK} = 50MHz	34.5		MHz
		f_{CLK} = 40MHz	27.6		MHz
	Stop Band Attenuation			**72**	dB (min)
	Group Delay Ripple (peak to peak)	f_{IN} < 22MHz, Equalizer on		**0.05**	Samples (max)

External Input Clock and PLL Characteristics

Unless otherwise specified, the following conditions apply: $V_A = V_D = 1.2V$; $V_{DR} = 1.2V$; V_{REF} = internal; R_{REF} = 10kohm ±1%; C_L = 5pF; 100Ω terminated at the receiver; f_{CLK} = 50MHz; f_S = 50MSPS. **Boldface limits** apply for $T_A = T_{MIN}$ to T_{MAX}; All other limits apply for T_A = +25°C.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits	Units
External Input Clock					
f_{CLK}	Allowed input clock frequency			40 50	MHz (min) MHz (max)
t_{CLK}	Allowed input clock period		$1/f_{CLK}$		ns
f_{CLK} DC	Allowed input clock duty cycle		50	20 80	% (min) % (max)
t_{JIN}	Allowed RMS clock jitter on input clock. (Note 9)	Integrated from 10Hz to BW_{loop}	300		fs rms
V_{CMCLK}	Allowed input clock common mode	(Note 8)		400 VDR	mV (min) mV (max)
V_{ICLK}	Allowed input clock voltage swing	Differential clock input.(Note 8)	400	200 VDR	mV peak-peak (min) mV peak-peak (max)
PLL					
f∑Δ	Over-sampling frequency			640 800	MHz (min) MHz (max)
BW_{loop}	PLL Loop filter bandwidth	Low Bandwidth	400		kHz
		High Bandwidth	1.4		MHz
t_J	RMS Clock Jitter on Bit Clock output			2	ps peak

Digital Input and Output Characteristics

Unless otherwise specified, the following conditions apply: $V_A = V_D = 1.2V$; $V_{DR} = 1.2V$; V_{REF} = internal; R_{REF} = 10kohm ±1%; C_L = 5pF; 100Ω terminated at the receiver; f_{CLK} = 50MHz; f_S = 50MSPS. **Boldface limits** apply for $T_A = T_{MIN}$ to T_{MAX}; All other limits apply for T_A = +25°C.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits	Units
Digital Inputs (S_{DATA}, S_{SEL}, S_{CLK}, SLEEP, RST)					
V_{IH}	Logical input “1” voltage	Test run at 2MHz		900	mV (min)
V_{IL}	Logical input “0” voltage	Test run at 2MHz		300	mV (max)
I_{IN1}	Logical "1" Input current			**1**	µA (max)
I_{IN0}	Logical "0" Input current			**-1**	µA (min)
C_{IN}	Input Capacitance	Guaranteed by design	5		pF
Digital Outputs (S_{DATA})					
V_{OH}	Logical output “1” voltage	Test run at 2MHz, V_{DR} = 1.2V	V_{DR}	**850**	mV (min)
V_{OL}	Logical output “0” voltage	Test run at 2MHz, V_{DR} = 1.2V	DRGND	**250**	mV (max)
I_{OH}	Logical "1" Output Current			**-0.75**	mA (min)
I_{OL}	Logical "0" Output Current			**1**	mA (max)
Output Drive Capability (S_{DATA})					
C_{LOAD}	Load capacitance	R = 4.7 kohm, V_{DR} > 1.8V	50		pF
		R = 4.7 kohm, V_{DR} = 1.2V	50		pF
Open Drain Mode					
V_{EXT}	Maximum allowed external voltage on S_{DATA}	Open Drain mode activated		2.5	V
R_{SDATA}	Recommended S_{DATA} external pull-up resistor	Open Drain mode activated	4.7		kΩ

AC and Timing Characteristics

Unless otherwise specified, the following conditions apply: $V_A = V_D = 1.2V$; $V_{DR} = 1.2V$; V_{REF} = internal; R_{REF} = 10kohm ±1%; C_L = 5pF; 100Ω terminated at the receiver; f_{CLK} = 50MHz; f_S = 50MSPS. **Boldface limits** apply for $T_A = T_{MIN}$ to T_{MAX}; All other limits apply for T_A = +25°C.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits	Units
General ADC Output Timing Parameters					
f_s	Sample Rate			40 50	MSPS (min) MSPS (max)
	Conversion Latency		19		Samples
t_{BCLK}	Bit clock period	f_{CLK} = 50MHz	3.33		ns
		f_{CLK} = 40MHz	4.16		ns
t_{WCLK}	Word clock period	f_{CLK} = 50MHz	20		ns
		f_{CLK} = 40MHz	25		ns
t_S	Outputs Data Edge to Output Clock Edge Setup Time	f_{CLK} = 50MHz	800	**325**	ps (min)
		f_{CLK} = 40MHz (Note 7)	900	480	ps (min)
t_H	Output Data Edge to Output Clock Edge Hold Time	f_{CLK} = 50MHz	850	**470**	ps (min)
		f_{CLK} = 40MHz (Note 7)	1150	770	ps (min)
t_{DV}	Output Data Valid Window	f_{CLK} = 50MHz (Note 7)	1380	885	ps (min)
		f_{CLK} = 40MHz (Note 7)	1820	1410	ps (min)
t_R, t_F	Output Rise/Fall time	f_{CLK} = 50MHz	320		ps (min)
t_{DFS}	Data Edge to Word Edge Skew	f_{CLK} = 50MHz	-295	**-720** **220**	ps (min) ps (max)
LVDS Output Parameters, OCM = 0 (V_{DR} = 1.2V)					
V_{OD}	Differential Output Voltage	LVDS mode, I_drive[1:0] = 00 (2.5mA), R_L = 100Ω	270		mV
		LVDS mode, I_drive[1:0] = 01 (3.5mA), R_L = 100Ω	370	**318** **428**	mV (min) mV (max)
		LVDS mode, I_drive[1:0] = 11 (5.0mA), R_L = 100Ω	520		mV
V_{OCM}	Output Common Mode Voltage	LVDS mode, OCM = 0 (for V_{DR} = 1.2V)	945	**895** **1000**	mV (min) mV (max)
LVDS Output Parameters, OCM = 1 (V_{DR} = 1.8V)					
V_{OD}	Differential Output Voltage	LVDS mode, I_drive[1:0] = 00 (2.5mA), R_L = 100Ω	265		mV
		LVDS mode, I_drive[1:0] = 01 (3.5mA), R_L = 100Ω	350	**280** **417**	mV (min) mV (max)
		LVDS mode, I_drive[1:0] = 11 (5.0mA), R_L = 100Ω	485		mV
V_{OCM}	Output Common Mode Voltage	LVDS mode, OCM = 1	1265	**1200** **1340**	mV (min) mv (max)
SLVS Output Parameters					
V_{OD}	Differential Output Voltage	SLVS mode, I_drive[1:0] = 00 (2.5mA), R_L = 100Ω	245		mV
		SLVS mode, I_drive[1:0] = 01 (3.5mA), R_L = 100Ω	330	**262** **393**	mV (min) mV (max)
		SLVS mode, I_drive[1:0] = 11 (5.0mA), R_L = 100Ω	475		mV
V_{OCM}	Output Common Mode Voltage	SLVS mode	225	**185** **270**	mV (min) mV (max)

AC and Timing Characteristics (Serial Interface)

Unless otherwise specified, the following conditions apply: $V_A = V_D = 1.2V$; $V_{DR} = 1.2V$; V_{REF} = internal; R_{REF} = 10kohm ±1%; C_L = 5pF; 100Ω terminated at the receiver; f_{CLK} = 50MHz; f_S = 50MSPS. **Boldface limits** apply for $T_A = T_{MIN}$ to T_{MAX}; All other limits apply for T_A = +25°C.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits	Units
Serial Interface					
t_{SSELS}	S_{SEL} setup time		250		ns
t_{SSELH}	S_{SEL} hold time		250		ns
t_{WS}	S_{DATA} setup time, write transaction		250	**15**	ns (max)
t_{WH}	S_{DATA} hold time, write transaction		250	**10**	ns (max)
t_{SCLK}	S_{CLK} period		1	**0.2**	µs (min)
t_{SCLKL}	S_{CLK} low time		450		ns (min)
t_{SCLKH}	S_{CLK} high time		450		ns (min)
t_{SCLKR}	S_{CLK} rise time		50		ns
t_{SCLKF}	S_{CLK} fall time		50		ns
t_{SSELHI}	S_{SEL} high time	Applies to read and write transactions	500		ns
t_{RS}	S_{DATA} valid setup time, read transaction		100	**-5**	ns (min)
t_{RH}	S_{DATA} valid hold time, read transaction		250	**10**	ns (min)

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. Guaranteed specifications and test conditions are specified in the Electrical Characterisitcs section. Operation of the device beyond the Operating Ratings is not recommended as it may degrade the device lifetime.

Note 3: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

Note 4: Typical figures are at TA = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 5: This parameter is specified in dBFS. This indicates the value which would be obtained with a full-scale input.

Note 6: As the filter is a digital circuit, Digital Decimation Filter Characteristics scale with input clock frequency, f_{CLK}.

Note 7: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 8: The combination of common mode and voltage swing on the clock input must ensure that the positive voltage peaks are not above VDR and the negative votlage peaks are not below AGND.

Note 9: See the "Clock Conditioner Owner's Manual", Chapter 2 (www.national.com/appinfo/interface/files/clk_conditioner_owners_manual.pdf) for a discussion on jitter.

Timing Diagrams

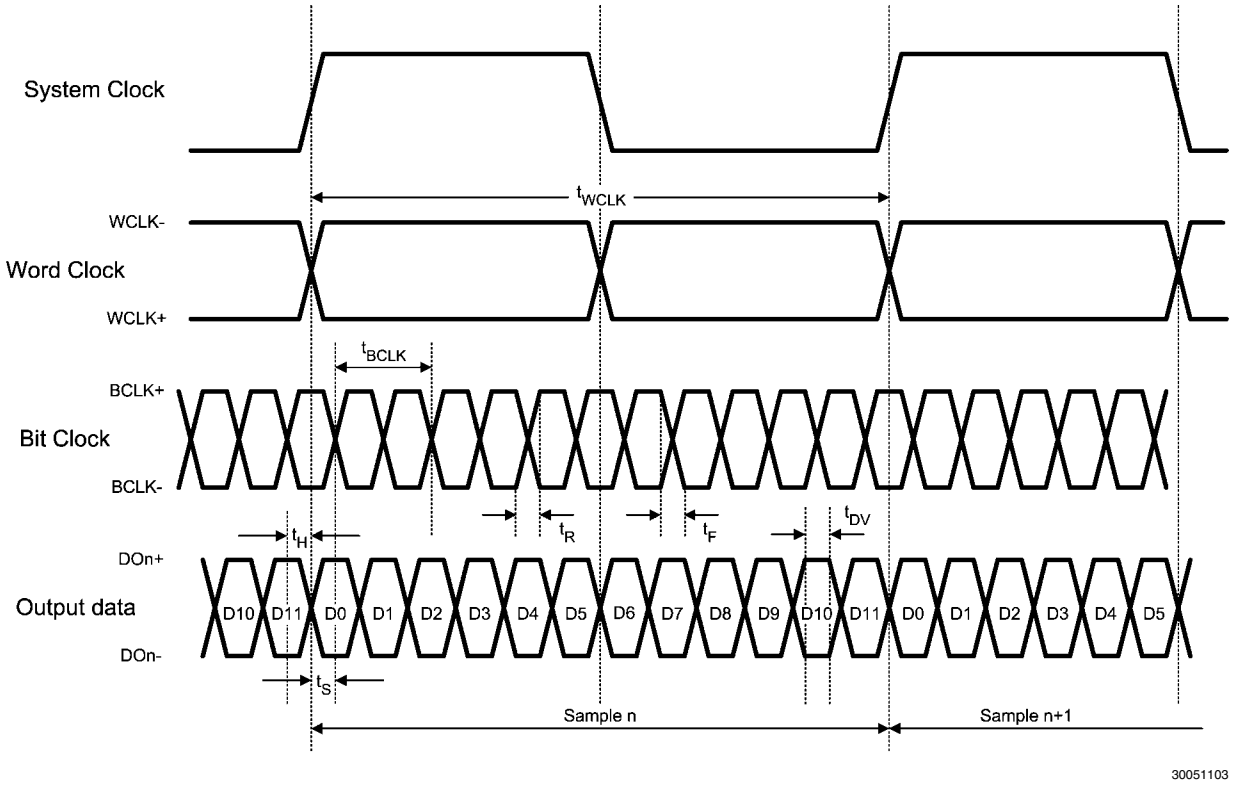


FIGURE 1. LVDS/SLVS Output Timing

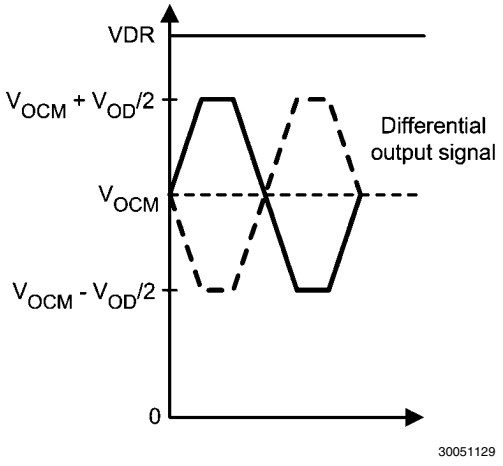


FIGURE 2. Output Level Definitions

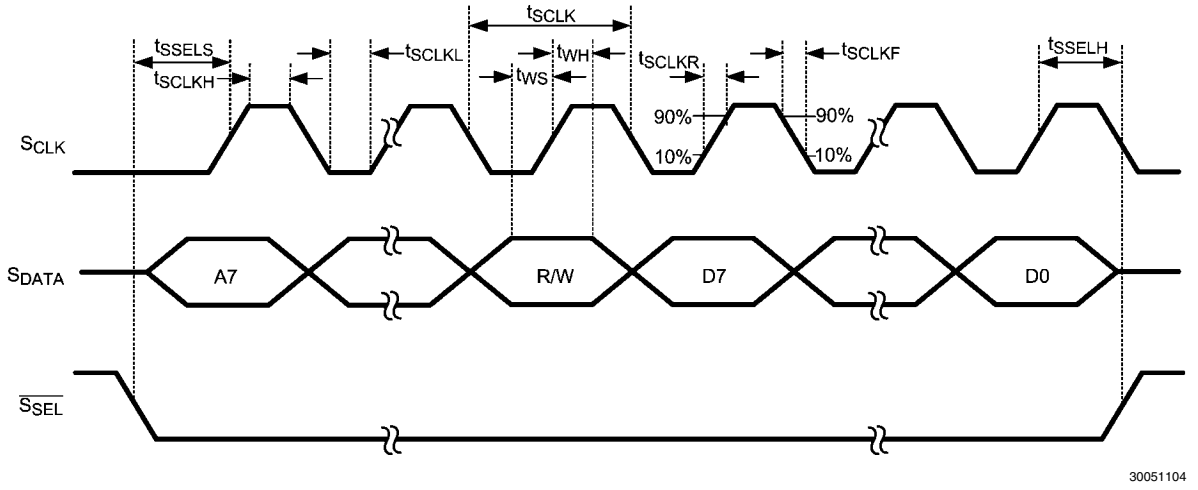


FIGURE 3. SPI Write Timing

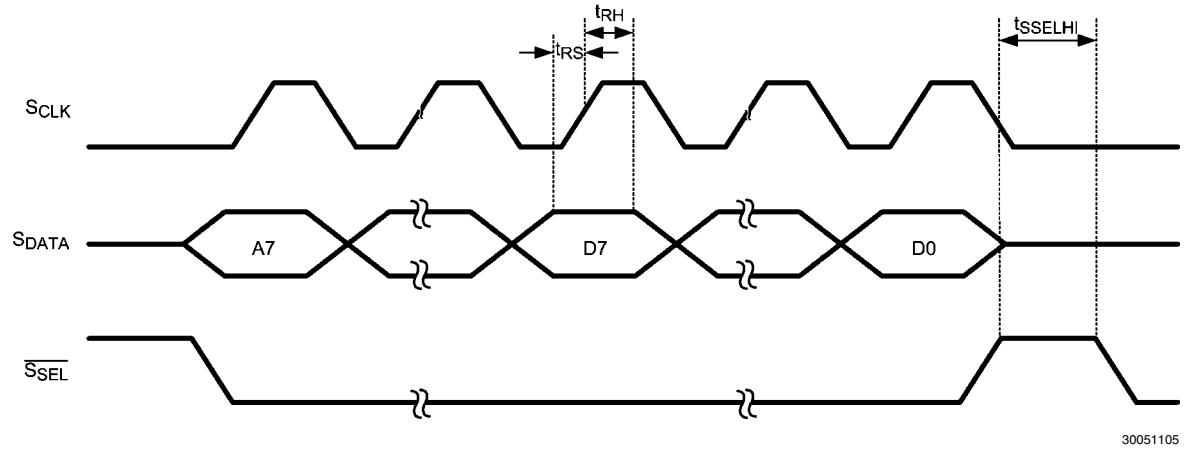
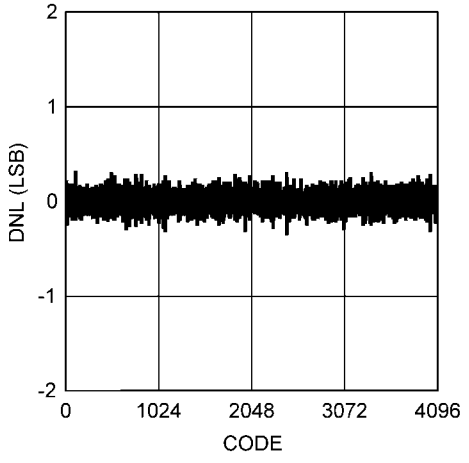


FIGURE 4. SPI Read Timing

Typical Performance Characteristics

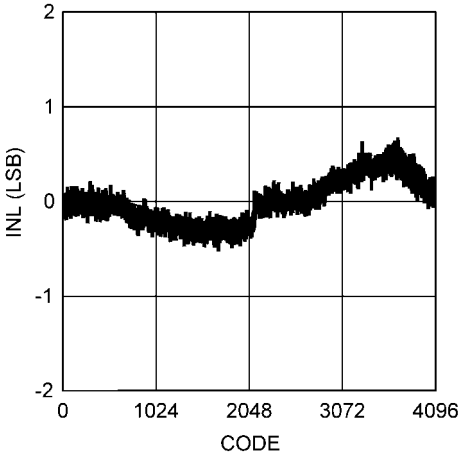
Unless otherwise specified, the following conditions apply: V_A = V_D = 1.2V; V_{DR} = 1.2V; V_{REF} = internal; C_L = 5pF; f_{CLK} = 50MHz; f_S = 50MSPS; f_{IN} = 10MHz. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc.

DNL



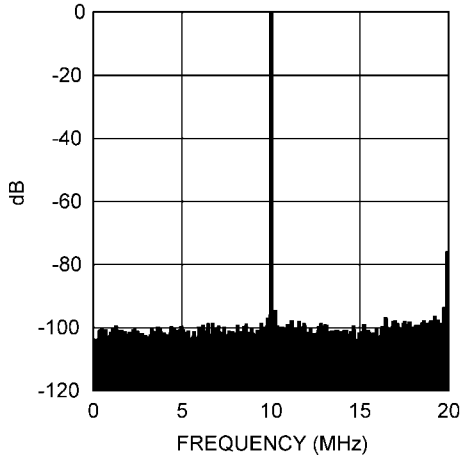
30051130

INL



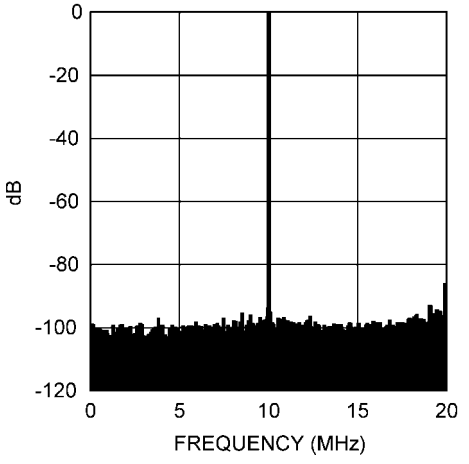
30051131

Spectral Response @ f_{IN}=10MHz, f_{CLK}= 40MHz, IOR off



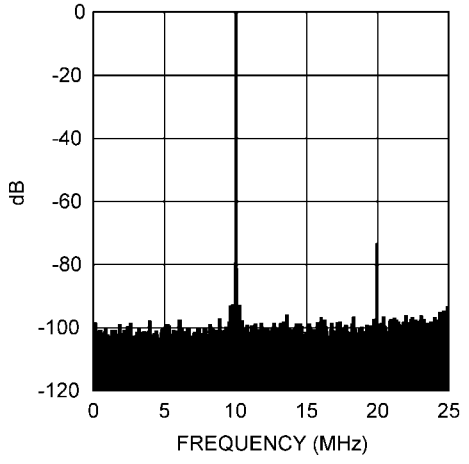
30051132

Spectral Response @ f_{IN}=10MHz, f_{CLK}= 40MHz, IOR on



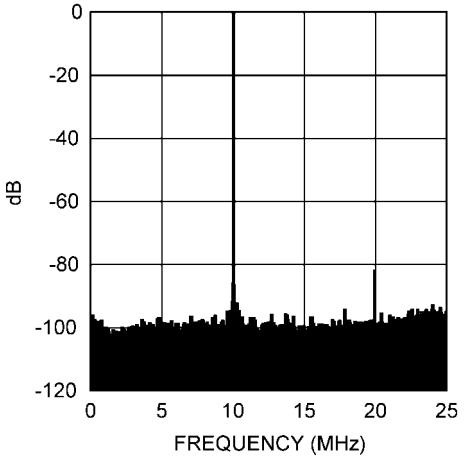
30051133

Spectral Response @ f_{IN}=10MHz, f_{CLK}= 50MHz, IOR off



30051134

Spectral Response @ f_{IN}=10MHz, f_{CLK}= 50MHz, IOR on

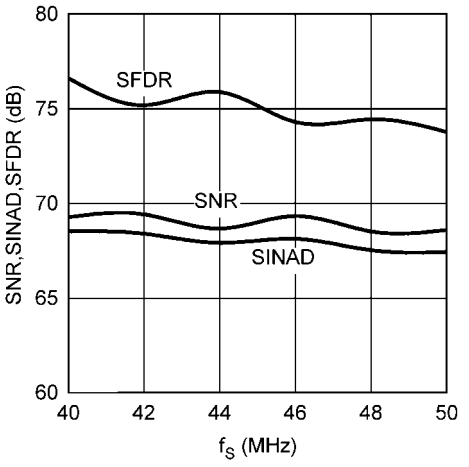


30051135

Typical Performance Characteristics

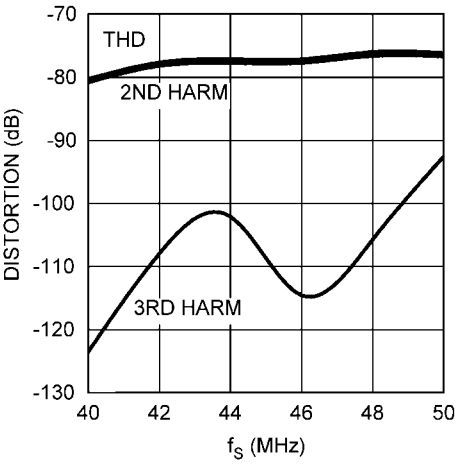
Unless otherwise specified, the following conditions apply: V_A = V_D = 1.2V; V_{DR} = 1.2V; V_{REF} = internal; C_L = 5pF; f_{CLK} = 50MHz; f_S = 50MSPS; f_{IN} = 10MHz. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc.

SNR, SINAD, SFDR vs f_{CLK}, IOR off



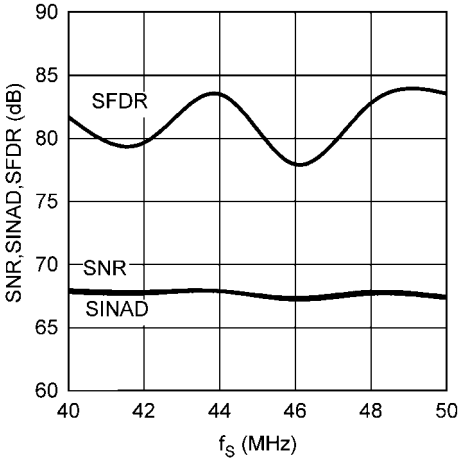
30051139

Distortion vs f_{CLK}, IOR off



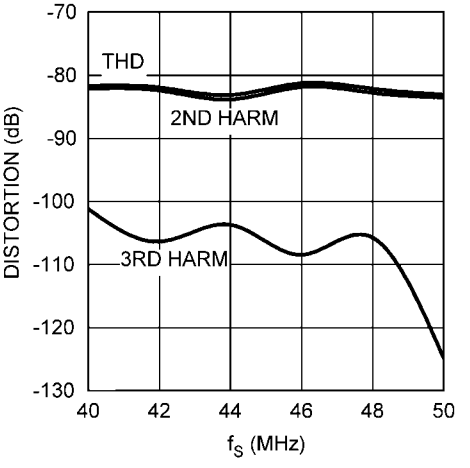
30051140

SNR, SINAD, SFDR vs f_{CLK}, IOR on



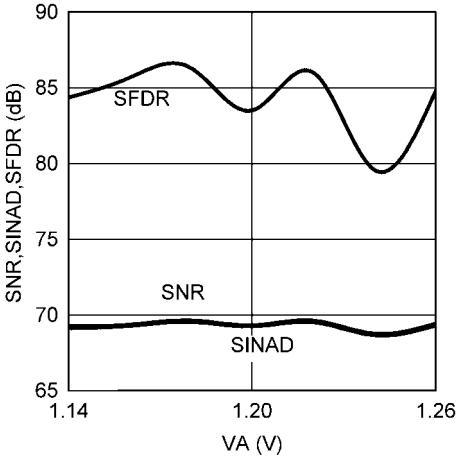
30051141

Distortion vs f_{CLK}, IOR on



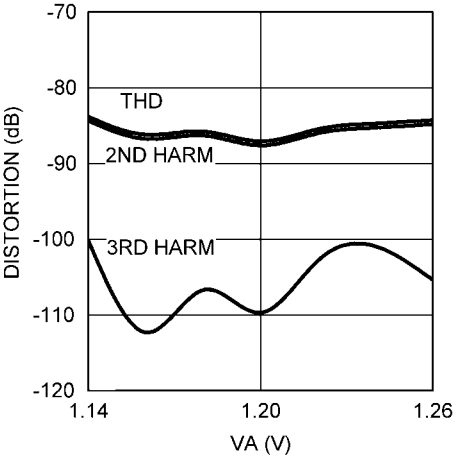
30051142

SNR, SINAD, SFDR vs VA, f_{CLK} = 40MHz, IOR off



30051143

Distortion vs VA, f_{CLK} = 40MHz, IOR off

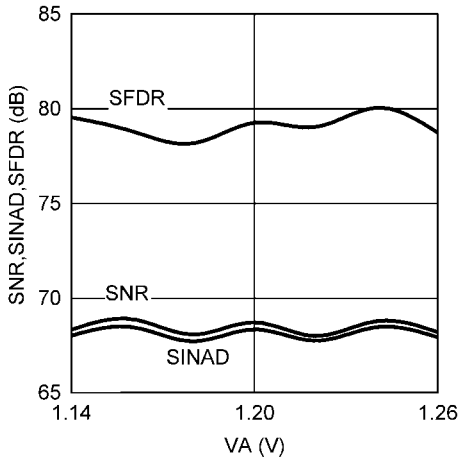


30051153

Typical Performance Characteristics

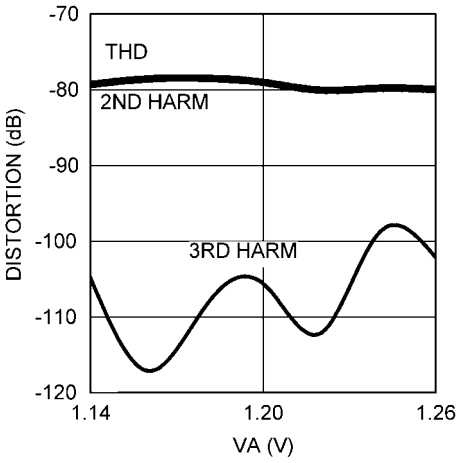
Unless otherwise specified, the following conditions apply: V_A = V_D = 1.2V; V_{DR} = 1.2V; V_{REF} = internal; C_L = 5pF; f_{CLK} = 50MHz; f_S = 50MSPS; f_{IN} = 10MHz. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc.

SNR, SINAD, SFDR vs VA, f_{CLK} = 50MHz, IOR off



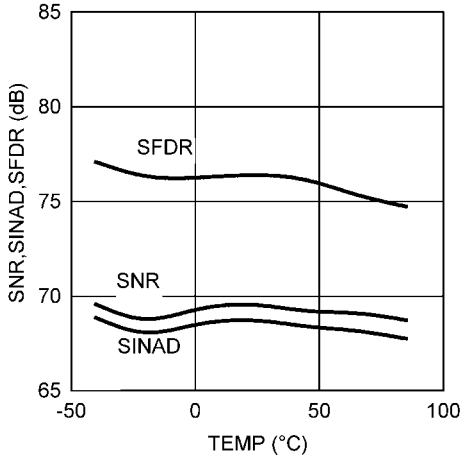
30051144

Distortion vs VA, f_{CLK} = 50MHz, IOR off



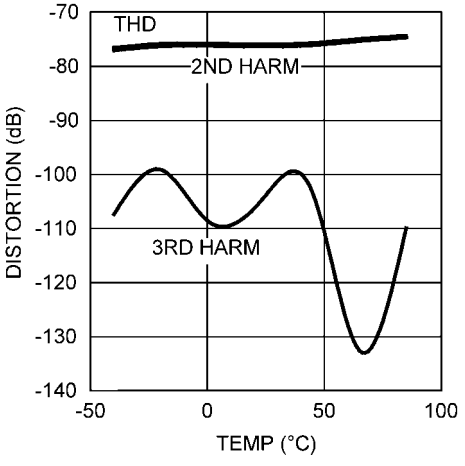
30051154

SNR, SINAD, SFDR vs Temperature, f_{CLK} = 40MHz, IOR off



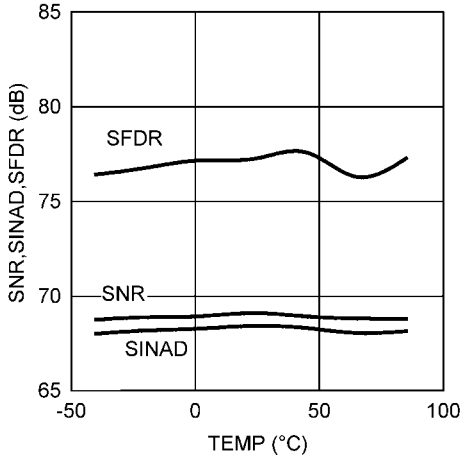
30051156

Distortion vs Temperature, f_{CLK} = 40MHz, IOR off



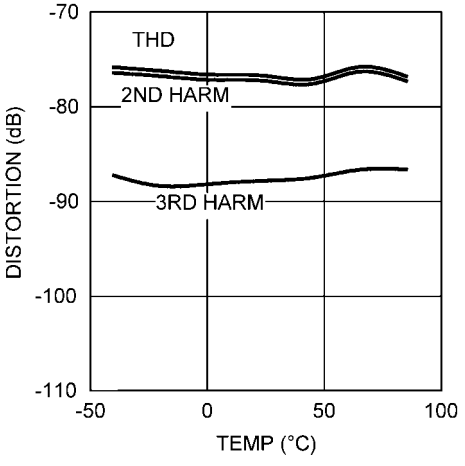
30051157

SNR, SINAD, SFDR vs Temperature, f_{CLK} = 50MHz, IOR off



30051160

Distortion vs Temperature, f_{CLK} = 50MHz, IOR off

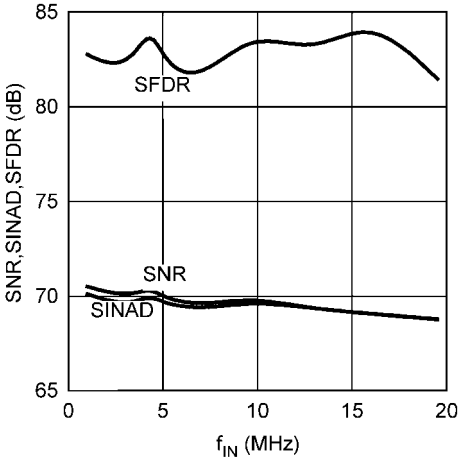


30051161

Typical Performance Characteristics

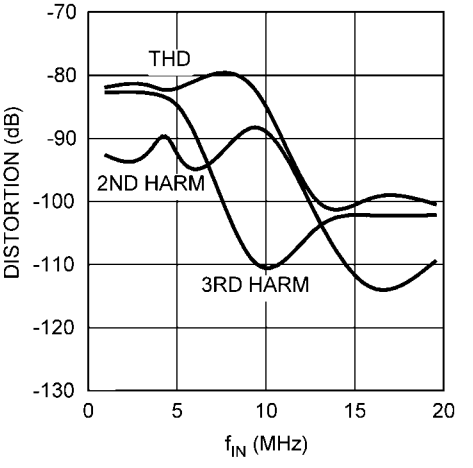
Unless otherwise specified, the following conditions apply: V_A = V_D = 1.2V; V_{DR} = 1.2V; V_{REF} = internal; C_L = 5pF; f_{CLK} = 50MHz; f_S = 50MSPS; f_{IN} = 10MHz. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc.

SNR, SINAD, SFDR vs f_{IN}, f_{CLK} = 40MHz, IOR off



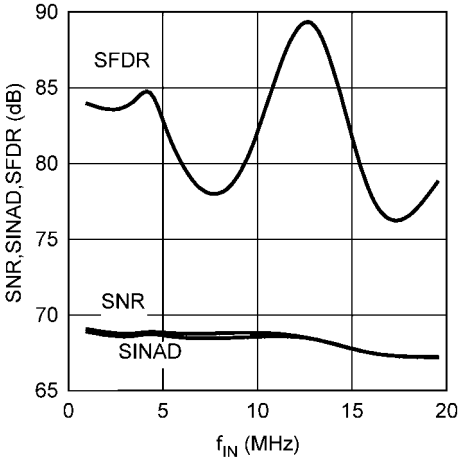
30051145

Distortion vs f_{IN}, f_{CLK} = 40MHz, IOR off



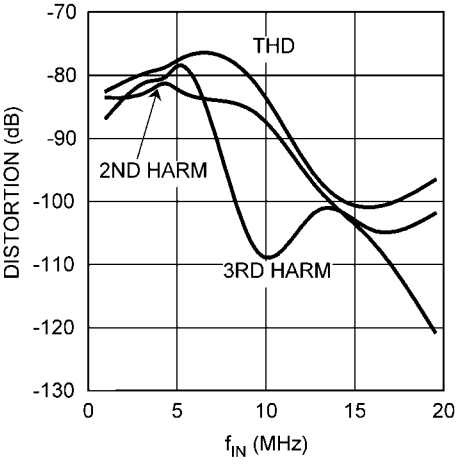
30051146

SNR, SINAD, SFDR vs f_{IN}, f_{CLK} = 40MHz, IOR on



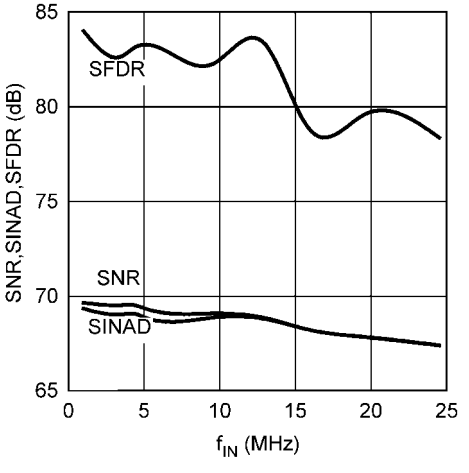
30051149

Distortion vs f_{IN}, f_{CLK} = 40MHz, IOR on



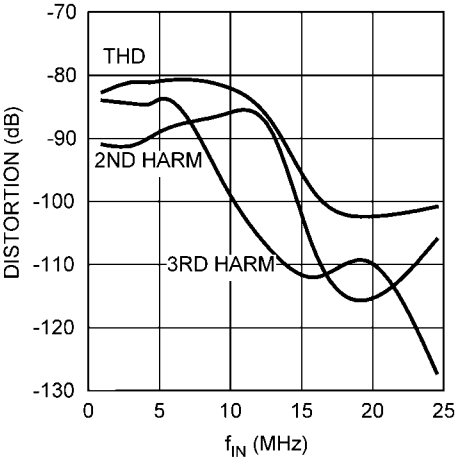
30051148

SNR, SINAD, SFDR vs f_{IN}, f_{CLK} = 50MHz, IOR off



30051147

Distortion vs f_{IN}, f_{CLK} = 50MHz, IOR off

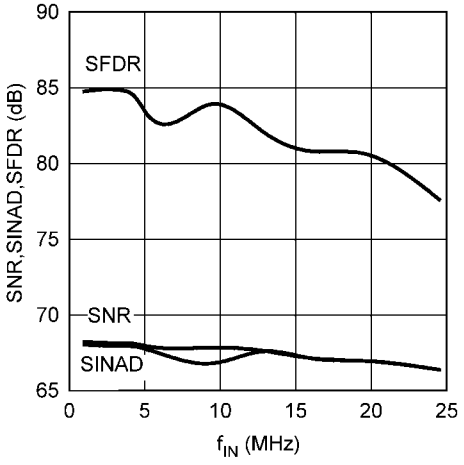


30051150

Typical Performance Characteristics

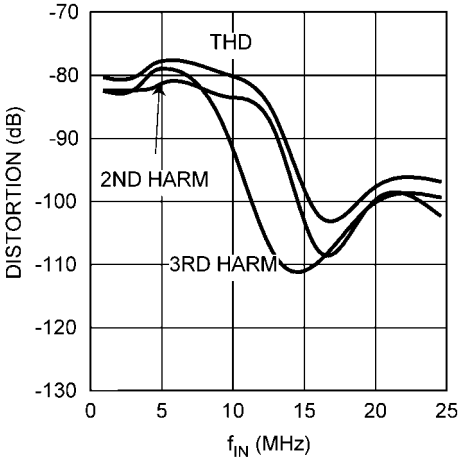
Unless otherwise specified, the following conditions apply: V_A = V_D = 1.2V; V_{DR} = 1.2V; V_{REF} = internal; C_L = 5pF; f_{CLK} = 50MHz; f_S = 50MSPS; f_{IN} = 10MHz. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc.

SNR, SINAD, SFDR vs f_{IN}, f_{CLK} = 50MHz, IOR on



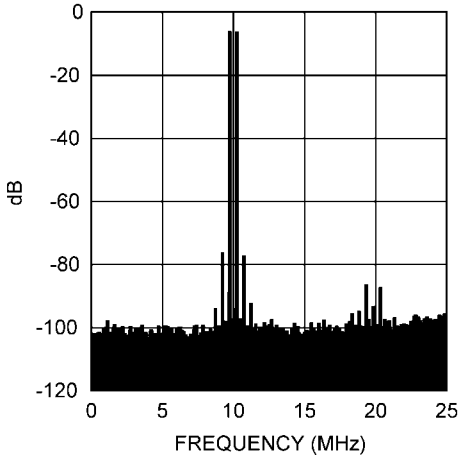
30051151

Distortion vs f_{IN}, f_{CLK} = 50MHz, IOR on



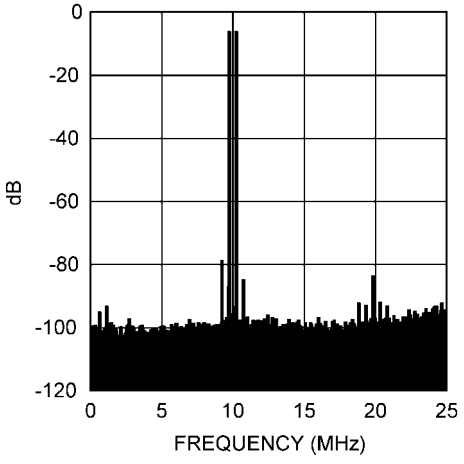
30051152

Spectral Response @ f_{IN1}= 9.6MHz, f_{IN2}= 10.1MHz, IOR off



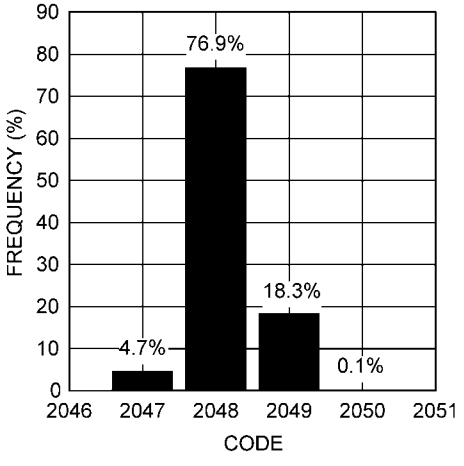
30051136

Spectral Response @ f_{IN1}= 9.6MHz, f_{IN2}= 10.1MHz, IOR on



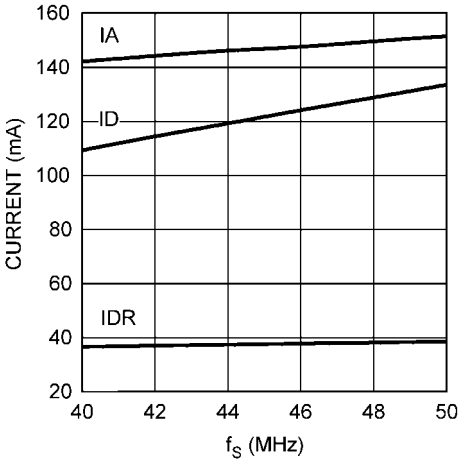
30051137

Histogram of output code for zero input



30051138

Current vs f_{CLK}, Equalizer off, LVDS output



30051155

Functional Description

The ADC12EU050 employs a number of unique strategies to provide a high performance multi-channel ADC that offers a significant power consumption reduction when compared to compteting architectures, as well as easing system level design. The ultra-low power performance of the ADC12EU050 is derived from the implementation of a fast continuous time sigma delta (CT∑Δ) modulator. Other features of this technology are:

- Intrinsic anti-alias filter – the digital decimating filter provides an intrinsic anti-alias filter, eliminating external analog filter components, and simplifying multi-channel designs.
- Instant overload recovery (IOR) system guarantees extremely fast recovery from overload (<1ps), and no settling errors on return from overload.
- Ultra-low inter-channel crosstalk.
- Digital Equalizer provides low group delay and hence minimizes signal path delay variation.

The major signal path blocks are: clipping control; CT∑Δ modulator; digital decimation filter; 12 bit serializer; and finally the LVDS/SLVS outputs. The PLL is critical to the operation of the ADC12EU050, and the PLL also provides the bit and word clock outputs. The SPI Control Interface gives uncomplicated user access to the ADC registers.

1.0 12-BIT SIGMA DELTA ADC CORE

The ADC12EU050 comprises eight analog ADC channels using a CT∑Δ architecture, which provides very high dynamic performance with ultra-low power, while operating from a minimal 1.2V supply.

The CT∑Δ ADC architecture uses a third order sigma delta modulator operating at a nominal 16 times over-sampling rate in combination with a 3-bit quantizer. The modulator output is coupled to a power efficient digital decimation filter that decimates the high rate modulator output (640 to 800MHz) to provide output data at a sample rate between 40 MSPS and 50 MSPS.

A benefit of the CT∑Δ design is that the ADC requires no external anti-alias filters for most applications. This benefit is derived from a combination of the design of the analog sigma delta modulator and digital decimation filter. The digital filter achieves a steep transition band, and provides 72 dB of attenuation in the stop band. Using the digital equalizer, the signal transfer characteristics including phase performance can be optimized so as to minimise group delay variation. In applications where it is not required, the digital equalizer can be disabled to further save power.

1.1 DIFFERENTIAL INPUT STAGE

The ADC can capture high speed analog signals without resorting to a complex fast sample-and-hold amplifier (SHA) as used in pipeline ADCs. This is where CT∑Δ technology derives much of its power and performance benefits. This feature also assists external circuit design. In the case of the SHA inputs of pipeline ADCs, the effective input capacitance is time variant, requiring a powerful input buffer to drive to the resolution limits of the system. The input stage of the ADC is purely resistive (1.3kΩ single ended) driving into virtual earth. As a result the ADC12EU050 is extremely easy to drive as its input impedance is not complex. It also means that external lower power input buffering circuitry can used, and can be completely eliminated in some cases.

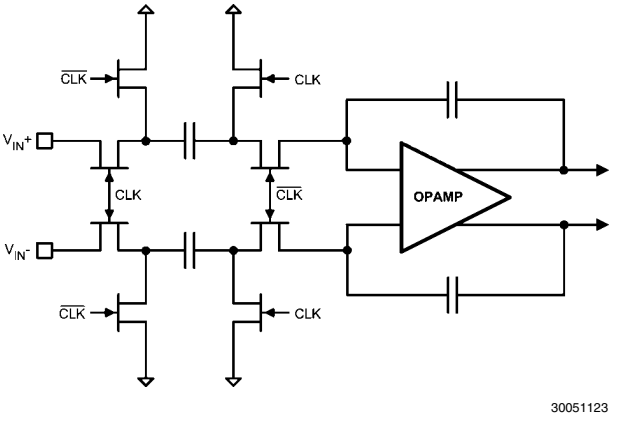


FIGURE 5. SHA Input Stage

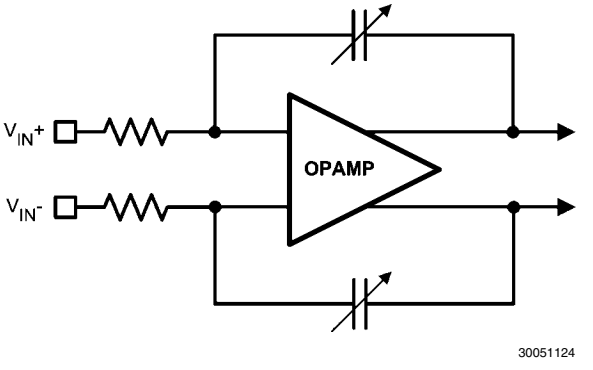


FIGURE 6. Continuous Time Sigma Delta Input Stage

1.2 INSTANT OVERLOAD RECOVERY

The ADC12EU050 features an overload handling system which provides instantaneous recovery from signals driving the ADC inputs beyond the full-scale input range. The ADC can operate in two different modes. In the default ADC mode (IOR mode off) a full-scale input range of 2.10 V_{PP} is supported, here the ADC operates with some inherent overload recovery time, similar to a conventional ADC.

In the IOR mode, the ADC has a reduced 1.56 V_{PP} full scale input range, but provides a significant benefit in that the ADC can now be driven by input voltages as high as 5 dB beyond the nominal full-scale (f_{IN} < 12MHz), that is 2.75 V_{PP}, and will recover instantaneously. In a number of applications this feature can help simplify input stage design and manufacturing set-up and calibration. The ADC12EU050 recovers immediately from overload with no missing codes and no settling time.

The proprietary strategy used within the ADC12EU050 uses high speed patented clamp techniques to limit the input signal and keep it within the stable input range of the ADC. This process happens at a speed equivalent to the on-chip oversampling rate of 640 to 800 MHz. The advantage of this system is that it responds immediately to out of range signals. While the inputs are over-range the ADC outputs a full scale result. As the over-range input is removed the ADC adjusts to the input signal level and is able to provide sampled data instantaneously. The ADC's behaviour on emerging from overload is repeatable and independent of whether the input signal was positive or negative going at the point of overload. The diagram below shows a 5dB overloaded input (2.75 V_{PP} versus 1.56 V_{PP} Full scale), with 240,000 sample periods

overlaid. There is no ringing and recovery from overload is instantaneous.

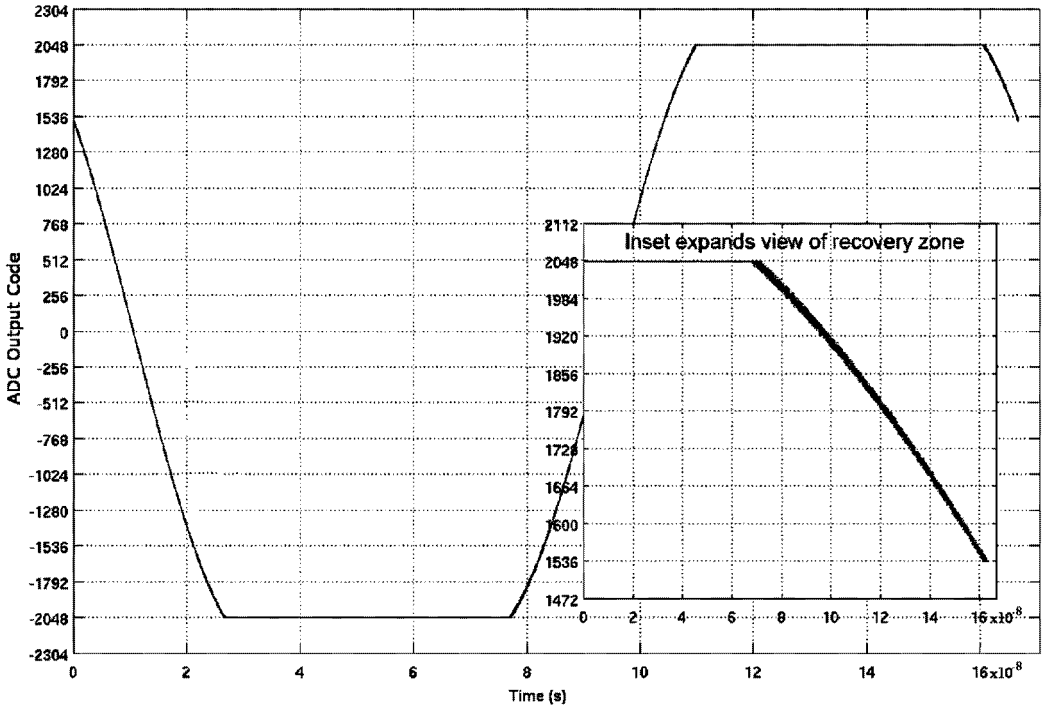


FIGURE 7. Instant Overload Recovery

1.3 INTEGRATED PRECISION LC PLL

The ADC12EU050 family includes an integrated high performance “clean up” phase locked loop (PLL), simplifying the need for a low jitter external clock. The PLL serves three important functions; it generates a highly accurate internal sampling clock source of up to 800 MHz; a clock for the LVDS serializers at 600 MHz; and it provides a low jitter clock for other internal components. With its jitter clean-up capability this PLL allows lower performance system clocks to be used.

1.4 DIGITAL DECIMATION FILTER AND EQUALIZER

The digital decimation filter is an integral part of the sigma delta architecture. It decimates the over-sampled data from the modulator down to the sample rate, and its extremely sharp low pass characteristic combined with the modulator’s broad band response provides the intrinsic anti-alias filter. The digital low pass filter exhibits 72dB of attenuation in the stop band. The following diagram shows the digital filter transfer function at 40MSPS, compared to a third order Butterworth transfer function. Due to the digital implementation of the filter, the filter parameters automatically scale with the ADC sampling frequency.

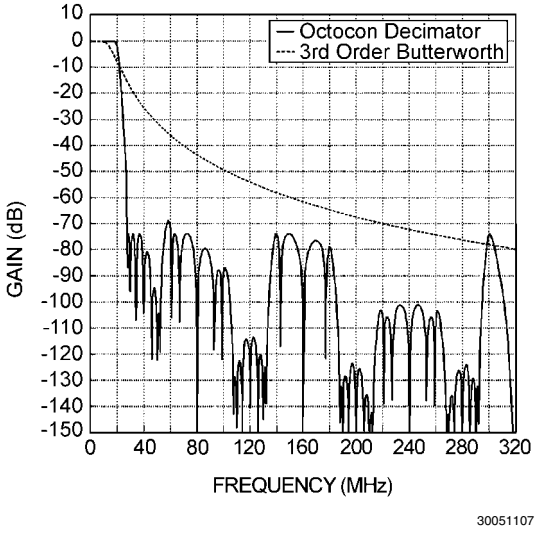


FIGURE 8. Digital Filter Transfer Function

Such steep digital filters introduce group delay problems, but the ADC12EU050 includes a digital equalizer, which reduces group delay ripple variation to less than 0.05 samples. In applications where group delay is not of concern, the equalizer can be turned off through the SPI interface in order to save power.

The following two diagrams show the group delay ripple of the digital decimation filter at 50MSPS, firstly with the equalizer disabled, and secondly with the equalizer enabled.

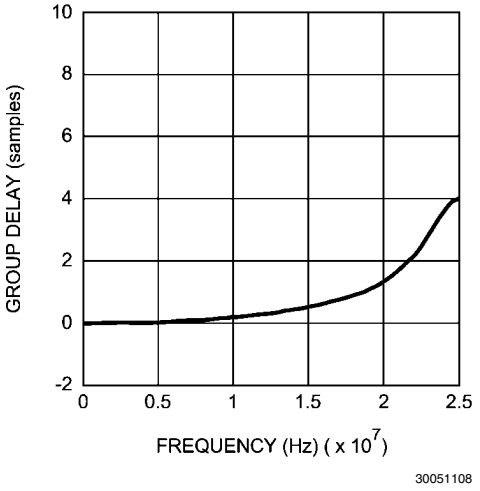


FIGURE 9. Group Delay with Equalizer Off

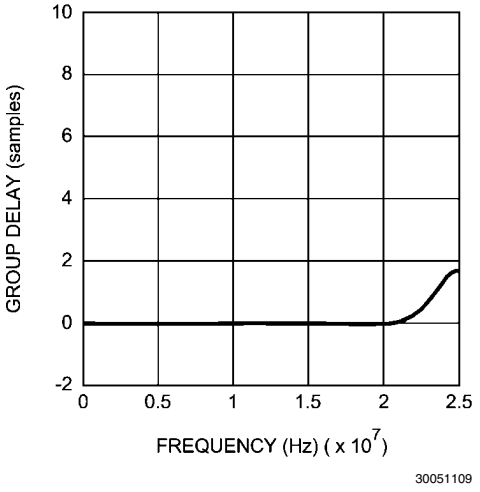


FIGURE 10. Group Delay with Equalizer On

1.5 SERIAL DATA OUTPUTS

Sampled data is transformed into high speed serial LVDS/SLVS output data streams. The low amplitude differential signal swings of LVDS/SLVS help to reduce digital system noise.

It is possible to select between LVDS and SLVS modes by simple programming through the SPI control interface. The output common mode can also be programmed through the SPI control interface, allowing it to be adjusted based on the value of V_{DR}.

1.6 POWER MANAGEMENT MODES

The ADC12EU050 operates normally at ultra-low power levels. In addition, several power management modes are provided:

- Power Down (accessible through PD bit of Top Control Register)
- Sleep (SLEEP pin, or SLEEP bit of Top Control Register)
- Single channel power down (PD0-7 of ADC/LVDS Channel Power Down Register)

Power Down is the lowest power consumption mode, but with a longer wake-up time than Sleep mode. In power down mode, all circuits in the chip are turned off, including the PLL, reference and bias circuits.

Power consumption in Sleep mode is higher than in Power Down mode, but pin access (SLEEP pin) and fast wake-up enables duty cycle powering of the ADC.

The device also allows channel by channel power-down through the ADC/LVDS Channel Power Down register. When a single channel is powered down, the sigma delta modulator, digital decimating filter and LVDS outputs for that channel will be shut off, with the corresponding single channel reduction in power consumption.

1.7 SPI CONTROL INTERFACE

The ADC12EU050 provides configurability via the serial control interface. This provides IOR mode control power management control, output configuration control, data output test patterns to provide LVDS/SLVS training sequences, as well as many other user configurable options. Full details of the SPI registers can be found in the Programming Guide section of this datasheet.

The SPI pins (S_{DATA}, S_{CLK}, S_{SEL}), as well as the pins RST and SLEEP, have been designed to operate with voltage levels up to 2.5V, despite the low 1.2V core voltage. As a result, no external level shift components are required for this control interface.

1.8 UNCORRELATED NOISE REFERENCE FOR EACH CHANNEL

In many early multi-channel ADC designs, a single voltage reference was used to provide the reference level for each channel. Unfortunately, this ensures that the noise at each ADC's reference terminal is cross correlated. Multi-channel systems often make use of a 3 dB processing gain increase that results from each channel doubling. Without a specific technique to prevent the reference terminals seeing correlated noise the expected 3 dB gain is compromised. In the case of the ADC12EU050, a unique system has been implemented to de-correlate the noise at each ADC channel.

Application Information

2.0 POWER-UP SEQUENCE

The ADC12EU050 has three separate power supplies: Analog (V_A), Digital (V_D) and the output drive voltage (V_{DR}). The ADC contains a power on reset circuit, connected to VA, and so to ensure correct reset of both analog and digital logic of the ADC, the power supplies should be provided in the following order:

1. V_{DR}
2. V_D
3. V_A

If this order is not followed, then the user should issue a reset via the reset pin (RST) immediately after power up.

Additionally, it is required that the rise time for each voltage supply is longer than the minimum rise time stated in the Electrical Specifications section of this data sheet.

There is no required sequence for powering down the ADC.

2.1 ADC START-UP SEQUENCE

After any reset, either power-on reset, software reset via SPI or hardware reset via the RST pin, the chip undergoes a series of internal calibrations and the PLL/VCO will lock to the external clock.

After reset, the ADC12EU050's registers have the default values shown in register tables. The registers can be programmed via the SPI after reset, even during the period while the chip is performing the internal calibrations mentioned in the previous paragraph.

During reset and until the PLL is locked, the LVDS outputs will not provide valid data. Furthermore, the ADC has an inherent data conversion latency, which is related to the pipeline stages of the digital decimating filter. Until the data conversion latency has passed, the data outputs will be invalid.

Thus the maximum time until valid sampled data is received at the outputs is:

PLL lock time + ADC Latency

Specific values for these times can be found in the Electrical Specifications section of this datasheet.

2.2 USING ADC LOW POWER MODES

As explained previously in the Functional Description, the ADC12EU050 offers several power management modes.

Sleep mode offers the fastest wake-up time, and should be used in applications where duty cycle powering of the ADC is required. In this case it is recommended to toggle sleep mode via the SLEEP pin, which will give a faster cycle time than programming the SLEEP bit through the SPI, due to the extra time required to send a command through the SPI port.

The Power Down mode is accessible via the SPI port. Due to the power-up time of the ADC coupled with the programming time of the SPI port, this mode should be used to power the chip down for longer time periods.

Channel power down allows one or more channels to be turned off independently, with the corresponding power saving.

2.3 CLOCK SELECTION CONSIDERATIONS

The ADC12EU050 has an on-chip PLL, which simplifies the task of clock source selection and clock network design.

Clock Input Connection

The ADC is designed to accept either single ended or differential clock inputs. Furthermore, the clock source can be a sine or square wave. In order to obtain the best performance, a differential square wave clock should be used. When using a differential clock, the clock traces should be routed as 100Ω differential pairs, and terminated with a 100Ω resistor close to the chip. A single ended clock input should be connected to pin 47 (CLK+/SE), and pin 48 (CLK-) should be grounded.

On-chip PLL

The benefit of having an on chip PLL is that in most applications a high precision clock source is not required. The external clock's contribution to aperture jitter is reduced dramatically by the jitter clean-up properties of the PLL, which ensures that any RMS jitter outside of the PLL bandwidth is attenuated. The PLL also significantly relaxes the input clock duty cycle requirements, accepting input clock duty cycles of 20% to 80%.

The PLL offers two choices of bandwidth. For the majority of systems, the default bandwidth of 400kHz is suitable. If the system already contains a high performance clock, with excellent RMS jitter performance up to a 1.4MHz bandwidth, then the PLL's high bandwidth mode may be used.

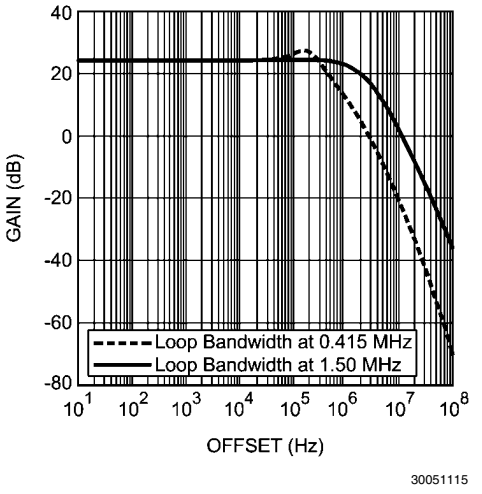


FIGURE 11. PLL Phase Noise Transfer Function: f_s = 40MHz

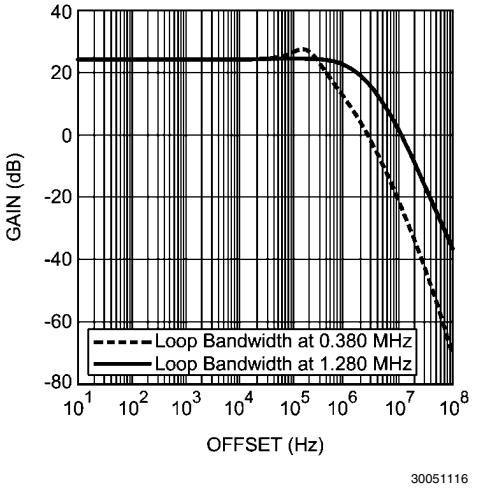


FIGURE 12. PLL Phase Noise Transfer Function: f_s = 50MHz

On the input clock, excessive RMS jitter within the PLL bandwidth will be seen in the output spectrum as sidebands, or close in phase noise, around the fundamental signal.

Input Clock Selection

For systems which do not have a requirement for a high performance clock, any standard product 40MHz – 50MHz crystal oscillator will allow the ADC12EU050 to perform to specifications. If the system requires high performance clocks for other system components, then National Semiconductor's LMK family of clock conditioners are recommended.

Output Clock Synchronization Across Multiple Chips

In systems containing more than one ADC12EU050, it is often required that the timing of output samples is synchronized across the multiple chips. The PLL in the ADC12EU050 takes care of this automatically by aligning the output clocks with the input clock. The user must ensure, using correct board layout and clock buffering techniques, that the input clock to each ADC12EU050 is synchronized. If this is the case, then the output frame clocks will also be synchronized. This means that output samples are aligned.

2.4 ADC INPUT CONSIDERATIONS

The ADC12EU050's sigma delta architecture offers many flexible options for connecting input signals.

In order to obtain maximum performance from the device, it is recommended to use a differential input connection. The device, however, also supports single ended analog input.

Differential Input Configurations

The ADC12EU050 can be driven either actively or passively.

Transformer coupling provides another possibility for converting a single ended signal into a differential signal. The diagram below shows a transformer coupled input configuration.

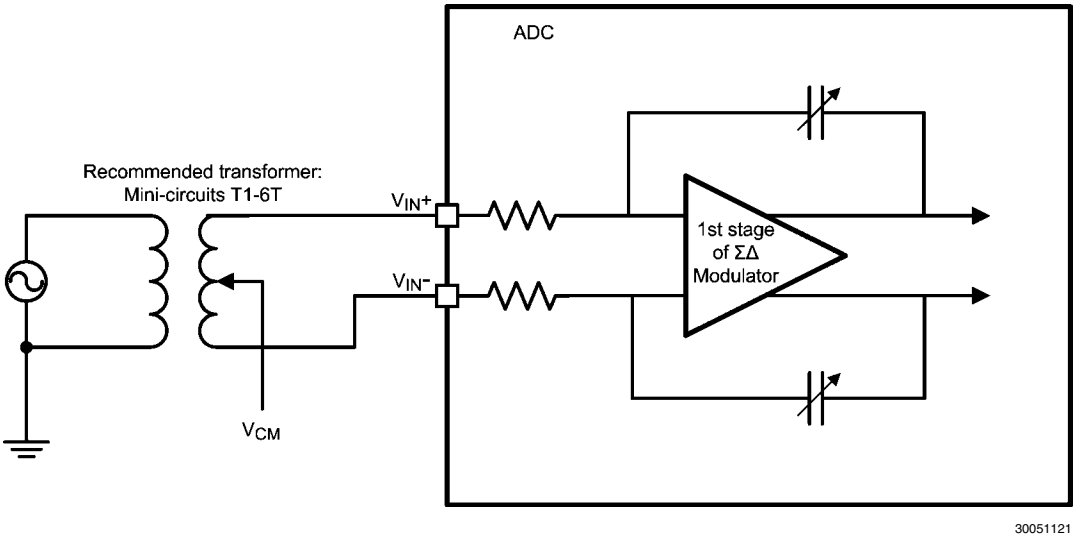


FIGURE 13. Transformer Coupled Input

Single Ended Input Configurations

In cost sensitive applications, a single ended input may provide adequate performance, however ADC performance will degrade slightly. When using single ended inputs, the maximum input voltage allowed is 3dB less than the 2.10V full scale input. The diagram below shows a single ended input configuration.

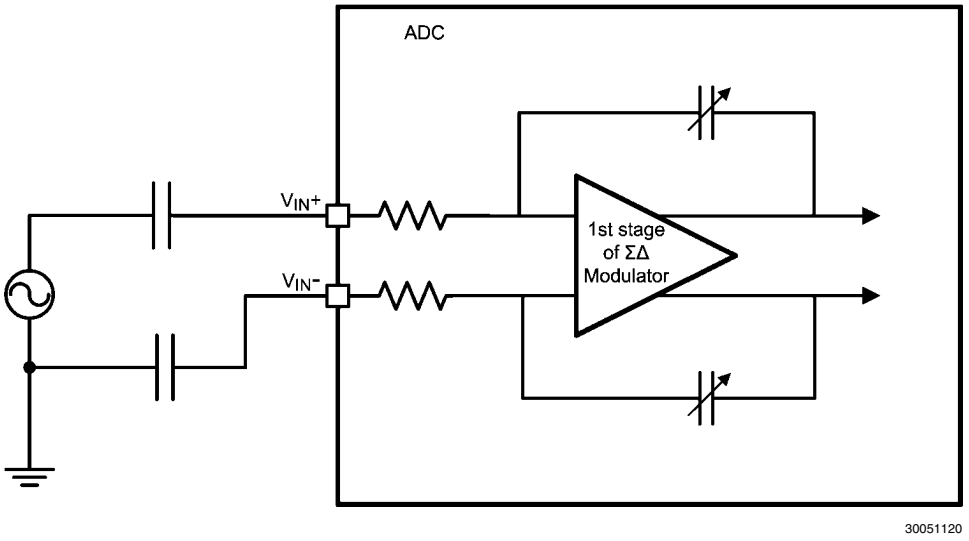


FIGURE 14. Single Ended Input

Input Coupling and Common Mode

The ADC12EU050 internally generates a common mode of 0.62V. It is possible to provide input signals with other common modes however, the full scale input range of the ADC must be kept in mind.

For this reason, it is recommended that the device inputs are AC coupled. The recommended capacitor value is 100nF.

External Series Resistance

Due to the purely resistive input circuit of the sigma delta architecture, the ADC12EU050 allows the user to scale down large input signals by adding external series resistors. The gain achieved by adding external resistors can be calculated as a simple voltage divider, as follows:

$$V_{FS}/V_{IN} = 20 * \log (R_{ADC} /(R_{ADC} + R_{EXT})) \text{ dB}$$

The diagram below shows this configuration, and defines the values in the equation above.

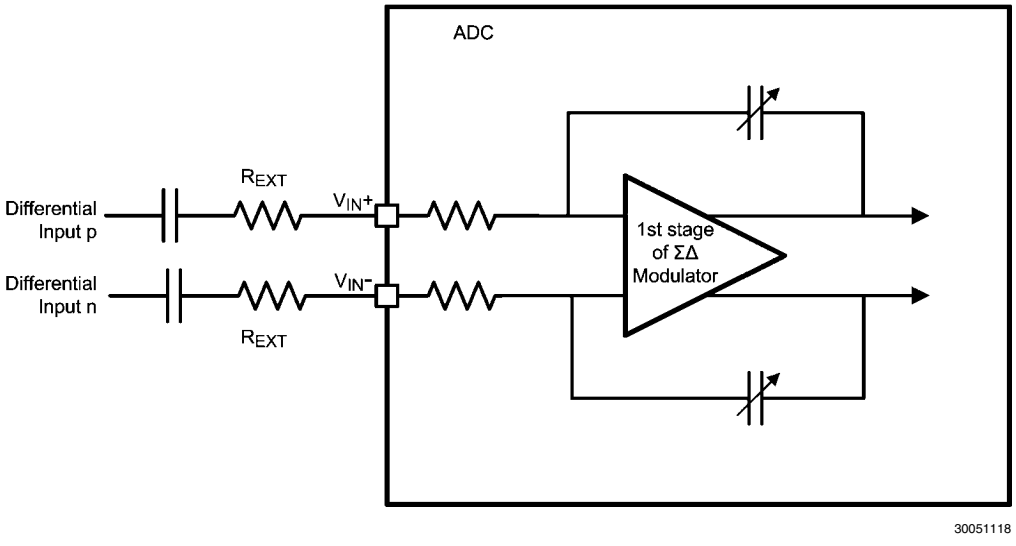


FIGURE 15. External Series Resistance

R_{ADC}, the input resistance of the ADC, is nominally 1.3kΩ. Due to manufacturing the value of this resistance can vary by up to 15%. This is not important for the operation of the ADC, since the ADC depends only on internal resistors being matched, but it should be taken into account when performing calculations.

2.5 ADC OUTPUT CONSIDERATIONS

The ADC12EU050 offers a variety of output settings in order to cater for different system design and integration needs.

Output Driver Voltage, VDR

The ADC output driver voltage, VDR, can be set between 1.2V and 1.8V. A VDR of 1.2V will offer the lowest power consumption. Because VDR can be varied, the ADC12EU050 provides, via the SPI registers, the ability to adjust the output common mode voltage.

Output Modes And Output Common Mode

Three different output modes are also supported: SLVS, LVDS and reduced common mode LVDS. SLVS and LVDS modes output data according to their respective specifications.

Reduced common mode LVDS must be used when the output driver voltage, VDR, is 1.2V. The standard LVDS common mode voltage is 1.2V, which is obviously not feasible if VDR is 1.2V. Therefore, the output common mode voltage must be set to 1.0V by setting the bit OCM in the LVDS Control Register to 0.

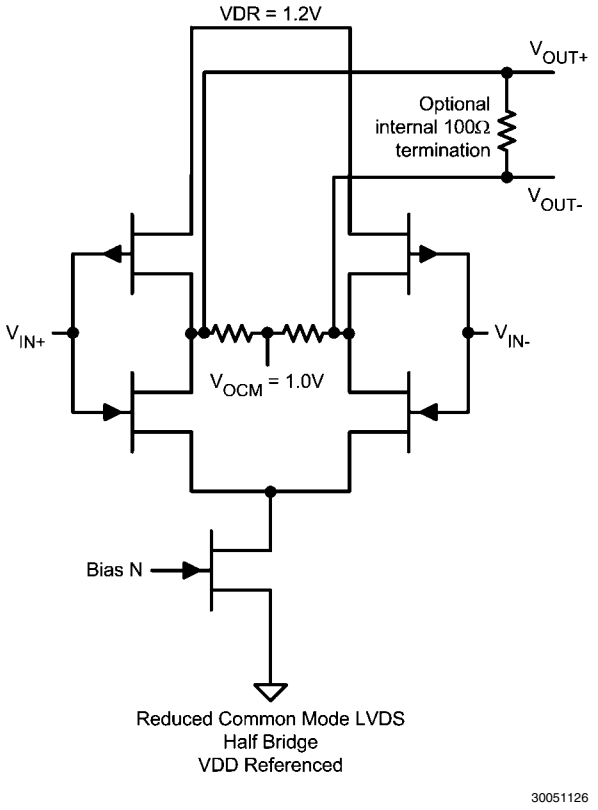


FIGURE 16. Output Driver Circuit: Reduced Common Mode LVDS

When VDR is 1.8V, the standard LVDS common mode voltage of 1.2V must be used, by setting OCM equal to 1.

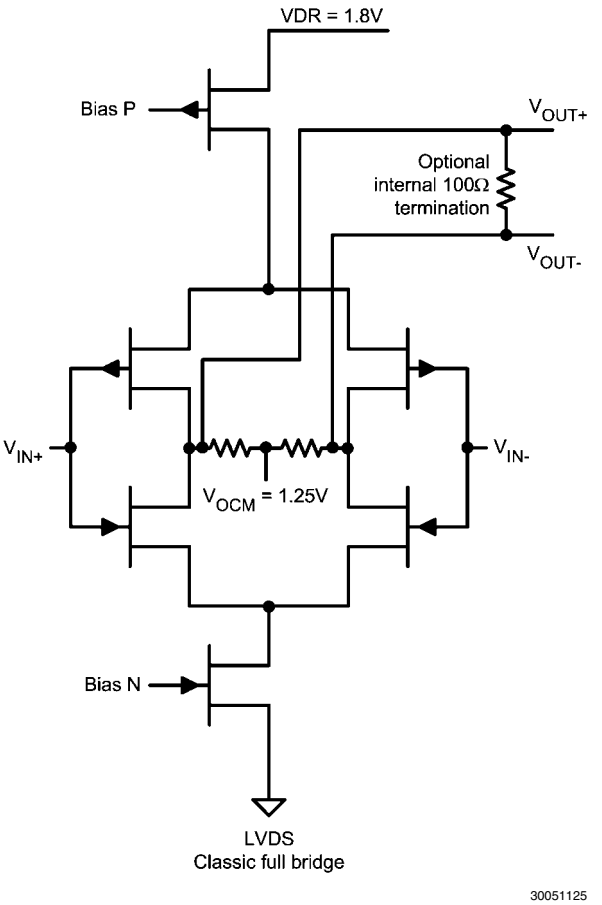


FIGURE 17. Output Driver Circuit: LVDS

SLVS mode offers the lowest power consumption, followed by reduced common mode LVDS then standard LVDS.

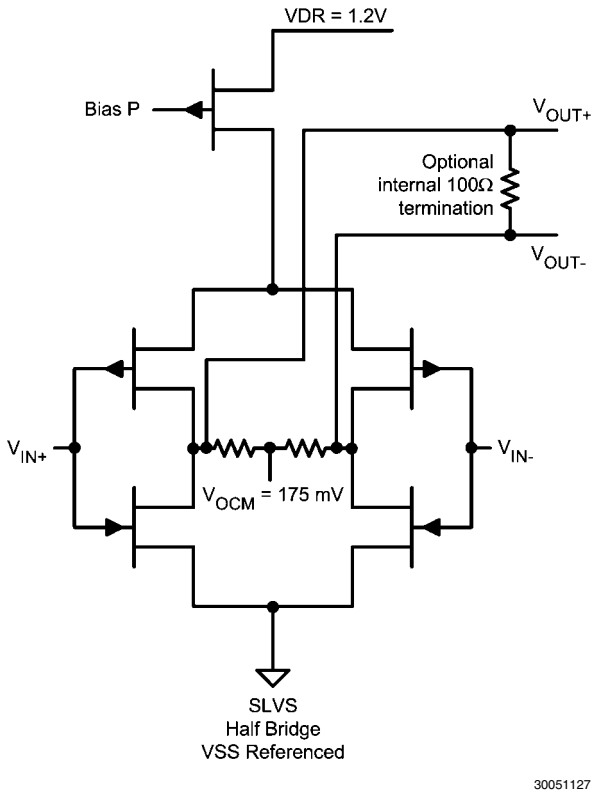


FIGURE 18. Output Driver Circuit: SLVS

As well as the different output modes, the output drive current can also be controlled via the LVDS Control Register. The default output drive current is 2.5mA, but this can be increased to 3.5mA or 5mA, depending on output trace routing and receiver requirements. Power consumption of the ADC12EU050 will increase slightly as the output driver current is increased.

Termination

The final control feature available in the LVDS Control Register is the choice between internal and external 100Ω termination. Although the termination is recommended to be as close to the receiver as possible, in some cases it may be necessary or desirable to perform this termination at the transmitter. Internal 100Ω termination at the transmitter (the ADC12EU050) is enabled by setting the bit TX_term to 1.

LVDS Output Training Sequences

Often it is necessary to calibrate the LVDS receiver, for example an FPGA or DSP, so that skew between the eight ADC output channels is minimized. In order to simplify this process, the ADC12EU050 provides three LVDS training modes, where a pre-defined or custom pattern is output on all eight channels simultaneously. While a training mode is active, the word and bit clocks are output as usual. In order to select a training mode, the TSEL bits of the Decimator Control Register (16h) must be programmed via the SPI interface.

There are two pre-defined training patterns, or a custom pattern can be loaded via the SPI into the Serializer Custom Pattern 0 and 1 Registers (10h and 12h). In order to return to normal ADC operation after skew calibration, the TSEL bits should be returned to their default value of 00.

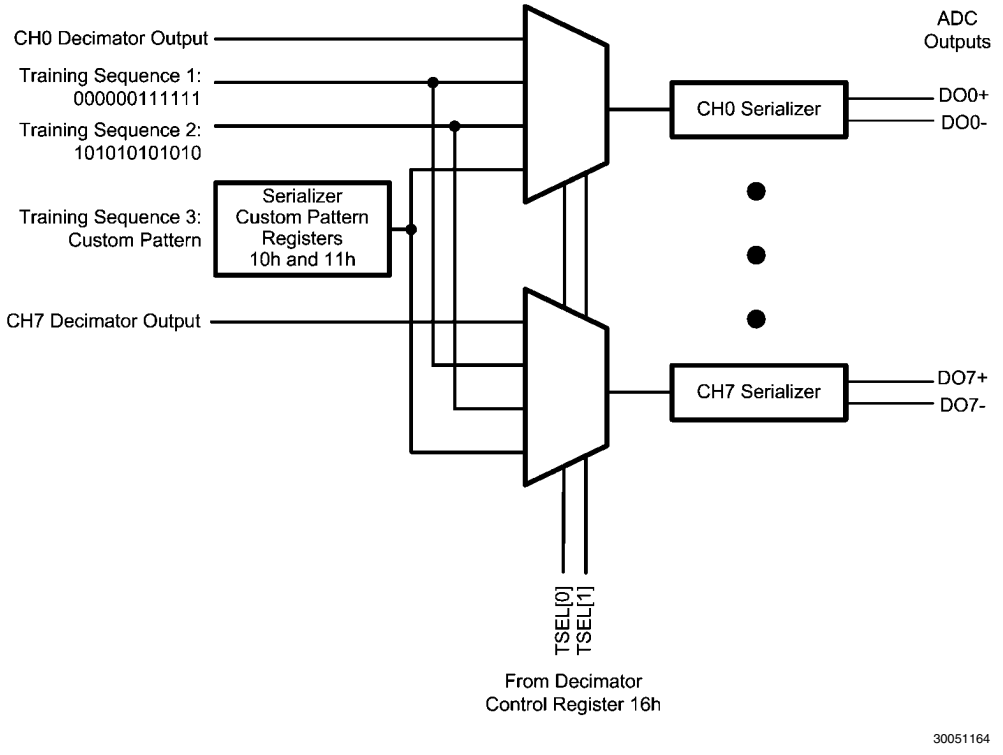


FIGURE 19. LVDS Training Select operation

2.6 USING IOR MODE

As discussed in the Functional Description, IOR mode provides instantaneous recovery from overload conditions, with no ringing and correct data output as soon as the input returns in range.

Standard Use of IOR Mode

The recommended way to enable IOR mode is by setting bit 4 (IOR) of the Modulator Overload Control register (04h). Setting this bit will enable IOR mode with the default settings for DGF in the Decimator Clipping Control register (14h) and OL in the Modulator Overload Control register (04h). Setting the IOR mode bit to 0 will restore DGF and OL to their default values, hence putting the chip back into ADC mode.

As can be seen in the Electrical Specifications, using IOR mode gives a slight reduction in SNR performance, and also a reduction of the full scale input range to 1.56Vpp differential.

Advanced Use of IOR Mode

The registers described above allow the user to customize IOR mode. In order to correctly set the DGF and OL values, it is necessary to understand how the IOR mode functions. The implementation of IOR mode in the ADC consists of analog and digital parts working in tandem.

The analog clipping circuitry, controlled by OL, is designed to protect the sigma delta modulator from large signal inputs. Using an analog clamp, signals are soft-limited to the less than the 2.10Vpp full scale range of the modulator. OL gives the value at which the circuit will begin to clamp.

The digital filter of the ADC12EU050 is where the full scale input range is selected and the hard limiting of the signal takes place. DGF selects the gain of the digital filter, and hence the new full scale input range of the ADC.

In order to set a custom value for DGF, CGS, bit 7 of the Decimator Clipping Control register, must be set. The DGF can then be set, based on the application requirements.

OL should then be set to a value approximately half-way between the new full scale input range (which was just selected by DGF) and the default full scale input range of 2.10Vpp. OL must be set to a value higher than DGF, otherwise the signal will be limited by the analog clipping circuitry, rather than the digtal circuitry, and overload recovery will be impacted.

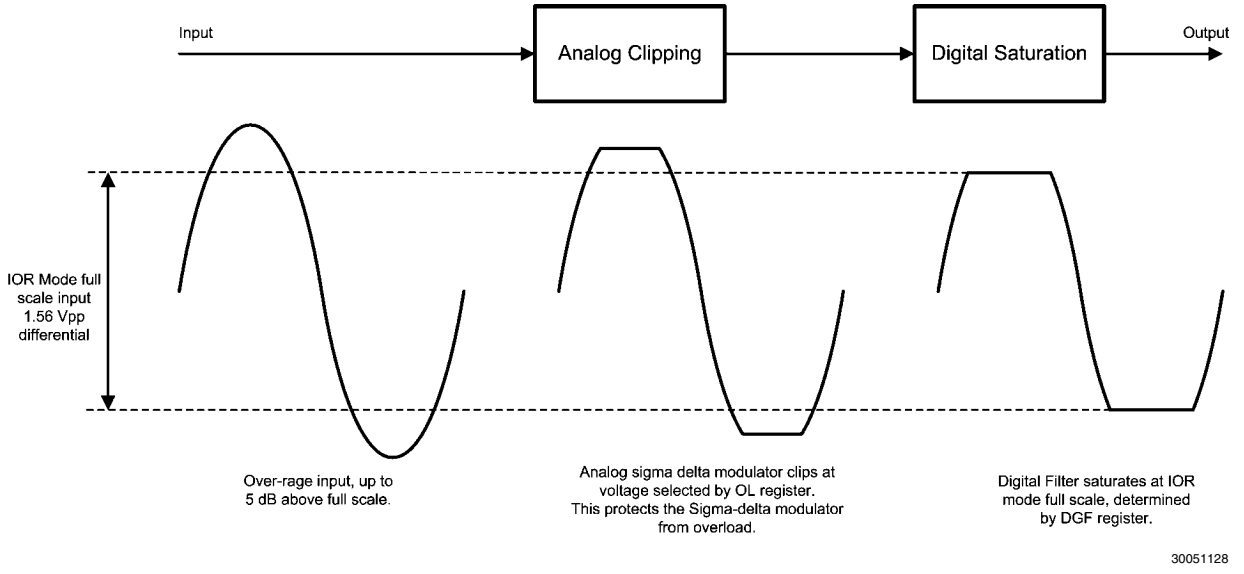


FIGURE 20. IOR Mode Signal Modification

2.7 THE VOLTAGE REFERENCE

The ADC provides an on chip, ±5% tolerance voltage reference, together with all necessary biasing circuits and current sources. A 10kΩ (±1%) resistor must be connected between R_{REF} and AGND in order to establish the biasing current of the ADC. The internal reference voltage, V_{REF}, is available at the R_{REF} pin.

When using the internal reference, V_{REFT} should be connected to AGND through a 100nF capacitor, while V_{REFB} must be connected to AGND.

Chip-to-chip gain matching between several ADC12EU050 ADCs can be improved by connecting the V_{REFT} pins of the ADCs. This is show in the figure below.

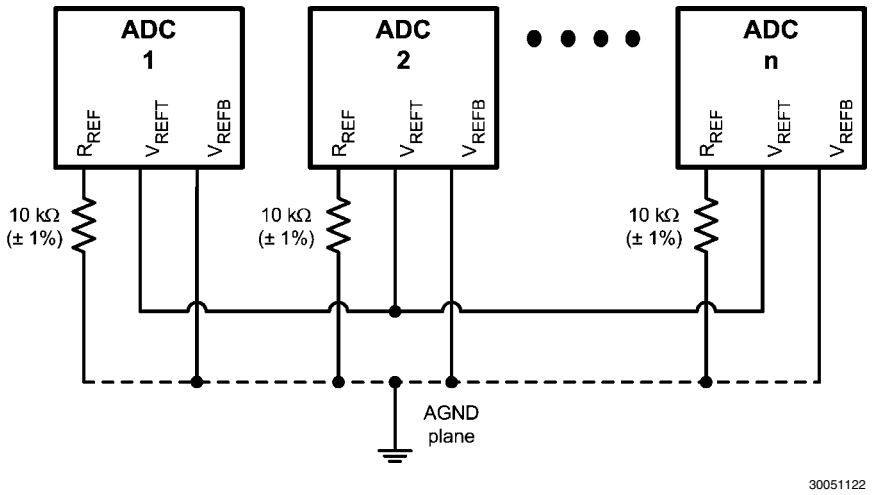


FIGURE 21. Reference Sharing

If a tighter tolerance reference is required for improved thermal stability, an external voltage reference can be connected between the V_{REFT} and V_{REFB} pins. The R_{REF} resistor must be connected even when using an external reference.

2.8 D_{CAP} CAPACITOR SELECTION

The D_{CAP} pin provides the capacitance for the low pass filter between the DAC bias block and the DAC in the sigma-delta modulator. The filter blocks noise from the DAC Bias block from entering the DAC. Any noise which passes through this filter will be seen in the spectrum as side skirts around the carrier. The filter circuit, which is a first order RC filter, is shown in the diagram below.

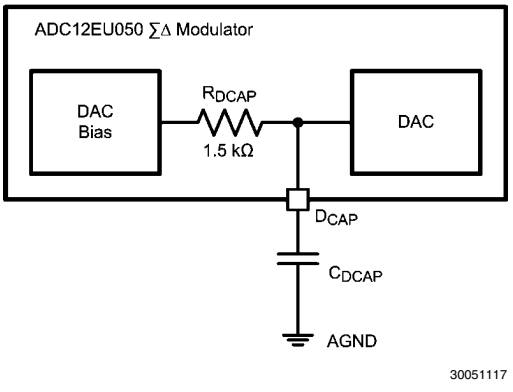


FIGURE 22. D_{CAP} RC Filter

The D_{CAP} pin must be connected to AGND through a low leakage, minimum 100nF capacitor. If the application is especially sensitive to close to the carrier phase noise, then it is recommended to increase D_{CAP}, up to a maximum of 10µF. For other applications where close to the carrier phase noise is not important, the capacitor can be kept small in order to reduce costs and minimise board space. The corner frequency of this filter is determined by the equation:

$$f = 1/(2\pi R_{DCAP} C_{DCAP})$$

2.9 BOARD LAYOUT CONSIDERATIONS

Proper grounding, layout and routing are essential to ensure accurate conversion in any high speed ADC.

Maintaining separate analog and digital areas of the board is recommended in order to achieve the specified performance. This includes using a split ground plane, since the significant digital portion of the chip can produce noise on the digital/IO ground (DGND).

When designing the ADC12EU050 into a system, It is critical that the exposed pad is connected to analog ground (AGND). The exposed pad provides the analog ground connection for the ADC12EU050, and so this connection is required for electrical rather than thermal reasons.

It is recommended to decouple the power supplies using a large capacitor (e.g. 47µF) for low frequency noise, and small capacitors (e.g. 100nF) placed close to each supply pin.

Analog and digital supplies (V_A and V_D) may be provided from the same supply, however in this case it is recommended that the supplies are isolated from each other with a ferrite bead or inductor. If the IO driver supply (V_{DR}) is 1.2V, then it may also be taken from the same supply, with isolation as described above.

The clock and data output traces, as well as the clock input trace (when using a differential input clock), should be routed as 100Ω impedance differential pairs. If not using the option for 100Ω internal termination, then the clock and data output trances should be terminated with a 100Ω resistor close to the receiver.

If the system requires regulators to provide the ADC12EU050 1.2V operating voltage, National Semiconductor recommends the LP3878SD-ADJ Low Noise “Ceramic Stable” Adjustable Regulator or the LP3879 Low Noise “Ceramic Stable” Regulator. Datasheets for both parts are available from the National Semiconductor website.

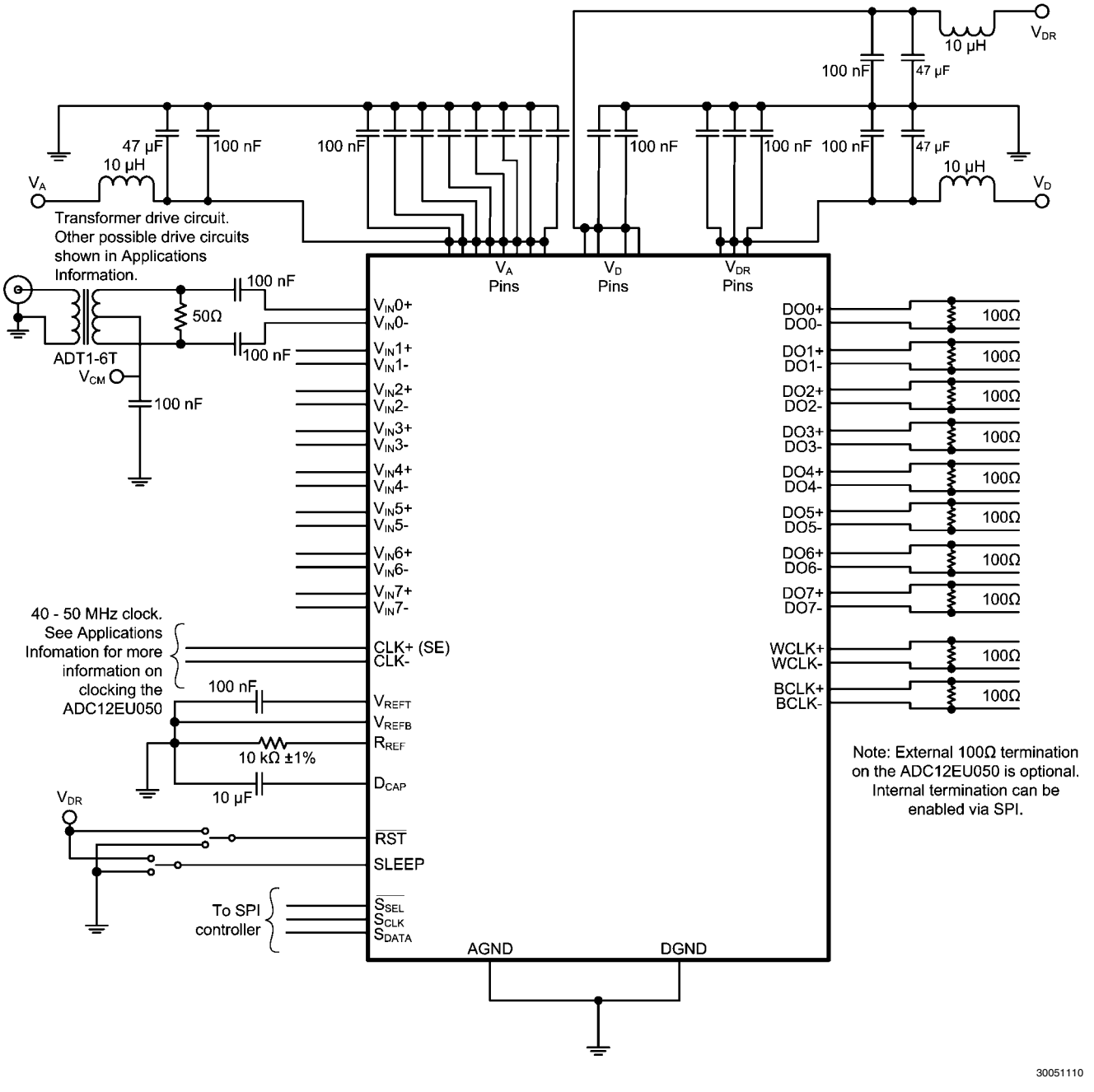


FIGURE 23. ADC12EU050 Application Diagram

Programming Guide

3.0 THE SERIAL CONTROL INTERFACE

The ADC12EU050 provides several user controlled functions which are accessed through a standard SPI compatible, 3 wire Serial Interface, as shown in the diagram below.

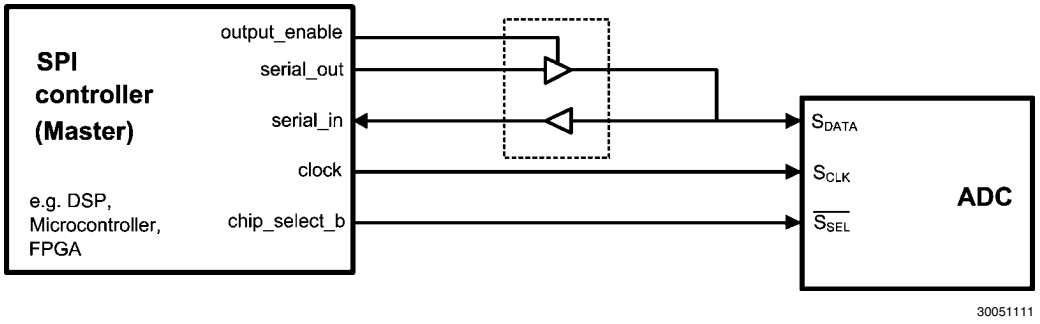


FIGURE 24. Three Wire Control Interface

Wired OR mode is supported in order to connect multiple ADC12EU050 devices to one SPI Master. The clock and data buses are common to all ADC devices, and the chip select S_{SEL} is used to control which SPI is currently active. The SPI master must have a unique pin available for each ADC's S_{SEL}. The diagram below illustrates the connection.

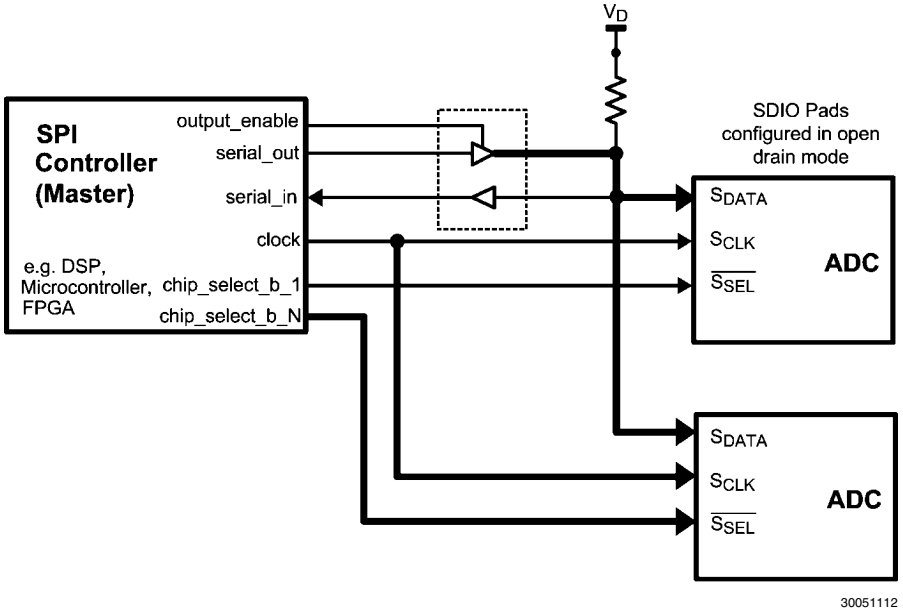


FIGURE 25. Multi-Wire Control Interface

When connecting multiple devices, the S_{DATA} pin must be set in Open Drain mode. Open Drain mode is enabled by setting the SPIOD bit in the Top Control Register of all connected ADC12EU050 devices. When S_{DATA} is in open drain mode, the user must ensure that a pull-up resistor is connected to the S_{DATA} bus. Further details on Open Drain mode are given in .

3.1 SERIAL CONTROL INTERFACE PROTOCOL

Both read and write transactions are made up of eight address bits and eight data bits. The final address bit of the address phase determines whether the transaction will be a read transaction or a write transaction – logic level low for write, logic level high for read. The following diagram shows the protocol.

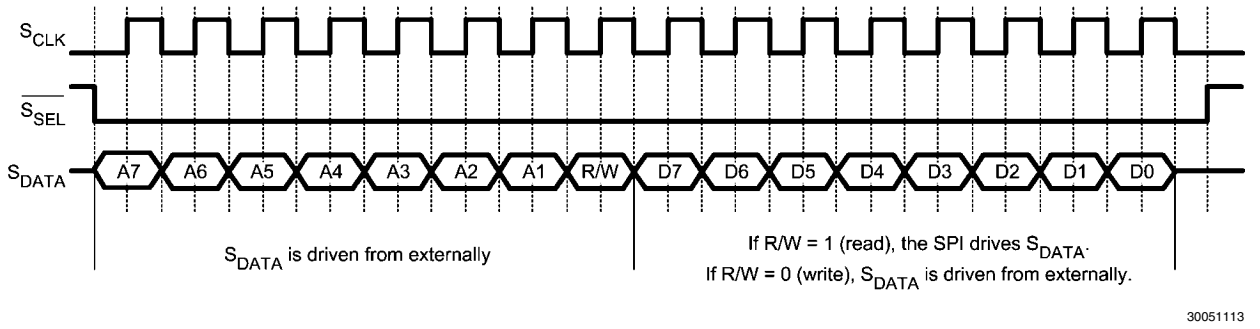


FIGURE 26. Serial Control Interface Protocol

The eight address bits, A[7:1] + R/W, are sent first. The data, D[7:0], is then sent for a write transaction, or D[7:0] is received for a read transaction. Address and data are sent and received with the most-significant-bit (MSB) first. The SPI is enabled using the active low input S_{SEL}. If S_{SEL} is high the SPI cannot be accessed, although S_{SEL} is not a reset signal and registers will maintain their value when S_{SEL} is toggled. S_{SEL} must be held low during the entire transaction.

Timing requirements for the Serial Interface are described in the Electrical Characteristics section of this document.

3.2 SERIAL INTERFACE TRANSACTION CANCELLATION

A transaction may be cancelled before the address and data stages are completed by toggling S_{SEL} to high at any stage during an SPI access. This action is not recommended, as transaction cancellation during a write transaction may corrupt register contents and during a read transaction will result in incorrect data.

After canceling a transaction with S_{SEL} the ADC may be in an unknown state due to an incomplete and hence corrupted write to a register. It is therefore recommended to reset the chip via Software Reset (SRES) after a cancelled transaction.

3.3 S_{DATA} PAD OPEN DRAIN MODE

If the S_{DATA} voltage at the board level is required to be higher than the ADC12EU050's V_{DR}, the Open Drain mode should be used. In Open Drain mode, the ADC's S_{DATA} will pull the output low, and S_{DATA} will be pulled up to the external level by a pull-up resistor connected to the board's positive voltage rail, VEXT.

The intended use of Open Drain mode is when the ADC, including V_{DR}, is running at 1.2V, and a VEXT of 1.8V is required.

Open Drain mode is enabled by setting the SPIOD bit in the Top Control Register via the Serial Interface. When in Open Drain mode, a pull-up resistor (RSDATA) must be connected between S_{DATA} and VEXT. The table of Electrical Specifications shows the required settings for VEXT and RSDATA.

3.4 SERIAL CONTROL INTERFACE READ AND WRITE SPEED

S_{CLK} (pin 45) controls the speed of interaction with the ADC. The SPI interface supports write to and read from speeds as defined in the Electrical Specifications section of this document.

3.5 SERIAL CONTROL INTERFACE REGISTER DESCRIPTIONS

The following tables show the complete set of user accessible SPI registers, with descriptions of the functionality of each bit.

Reset values of all registers are also described in the tables below.

Register Index

Address	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	Default
Top Control Register									
00h	Reserved	Reserved	CBR	40/50	SRES	SPIOD	SLEEP	PD	00h
ADC / LVDS Channel Power Down Register									
02h	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	00h
Modulator Overload Control Register									
04h	Reserved	Reserved	Reserved	IOR	OL[3]	OL[2]	OL[1]	OL[0]	00h
PLL Control Register									
08h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SHBW	STCAL	00h
LVDS Input Clock Hysteresis									
0Ah	Reserved	Reserved	INVCLK	100HYS	50HYS	20HYS	10HYSOFF	HYSOFF	00h
Serializer Custom Pattern 0 Register									
10h	Custom Pattern [7]	Custom Pattern [6]	Custom Pattern [5]	Custom Pattern [4]	Custom Pattern [3]	Custom Pattern [2]	Custom Pattern [1]	Custom Pattern [0]	00h
Serializer Custom Pattern 1 Register									
12h	Reserved	Reserved	Reserved	Reserved	Custom Pattern [11]	Custom Pattern [10]	Custom Pattern [9]	Custom Pattern [8]	00h
Decimator Clipping Control Register									
14h	Reserved	Reserved	a[2]	a[1]	a[0]	b[2]	b[1]	b[0]	00h
Decimator Control Register									
16h	Reserved	Reserved	Reserved	EQON	DFS	MSB	TSEL[1]	TSEL[0]	00h
LVDS Control Register									
18h	Reserved	Reserved	Reserved	TX_term	I_drive[1]	I_drive[0]	OCM	SLVS	00h
Chip ID Register									
1Eh	ID [7]	ID [6]	ID [5]	ID [4]	ID [3]	ID [2]	ID [1]	ID [0]	

Top Control Register

Address: 00h
Attributes Write Only.
Register 01h reads back contents of register 00h, if CBR is set.

The Top Control Register is the basic initialization and control register for the device.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	Reserved		CBR	40/50	SRES	SPIOD	SLEEP	PD	
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:6	**Reserved**. Write as zero for future compatibility.
5	**CBR: Control Bus Read**. When asserted register 00h (this register) can be read, but no other registers. When de-asserted all other registers can be read, but not register 00h. 0 Register 00h cannot be read from address 01h. All other registers can be read back. 1 Register 00h can be read from address 01h. All other registers cannot be read back.
4	**40/50:** Selects the ADC sample rate. This bit should be set according to the applied input clock to obtain optimal performance. 0 45-50MSPS 1 40-45MSPS
3	**SRES: Software Reset.** When asserted the software reset will reset the whole device. SRES performs the same function as the hardware reset (RST pin). The SRES is self clearing in approximately 2µs. 0 Software Reset Inactive 1 Software Reset Active
2	**SPIOD: SPI Open Drain mode.** 0 Digital Logic Output 1 Open Drain Mode. Enables SPI Driver to operate above V_{DR}
1	**SLEEP: Sleep Mode.** Powers down the device with the exception of the PLL and the reference blocks. The time to wake-up from sleep mode is < 10µs. 0 Sleep Mode Inactive 1 Sleep Mode Active
0	**PD: Power Down Mode.** Completely powers down the device. The power up time is approximately 20ms. 0 PD Mode Inactive, device operates normally 1 PD Mode Active, device powered down

ADC / LVDS Channel Power Down Register

Address:	02h
Attributes	Write Only.
	Register 03h reads back contents of register 02h.

The ADC/LVDS Channel Power Down Register provides the capability to independently power down each ADC channel.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7	**PD7: Power Down Channel 7** 0 Channel Active 1 Channel Power Down
6	**PD6: Power Down Channel 6** 0 Channel Active 1 Channel Power Down
5	**PD5: Power Down Channel** 0 Channel Active 1 Channel Power Down
4	**PD4: Power Down Channel 4** 0 Channel Active 1 Channel Power Down
3	**PD3: Power Down Channel 3** 0 Channel Active 1 Channel Power Down
2	**PD2: Power Down Channel 2** 0 Channel Active 1 Channel Power Down
1	**PD1: Power Down Channel 1** 0 Channel Active 1 Channel Power Down
0	**PD0: Power Down Channel 0** 0 Channel Active 1 Channel Power Down

Modulator Overload Control Register

Address: 04h
Attributes Write Only.
Register 05h reads back contents of register 04h.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	Reserved			IOR	OL[3:0]				
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:5	**Reserved.** Write as zero for future compatibility.
4	**IOR: Enable IOR Mode (Instant Overload Recovery)** This bit can be used to quickly enable IOR mode with the default IOR settings for DGF (see register 14h) and OL. 0 IOR Mode Disabled 1 IOR Mode Enabled
3:0	**OL[3:0]:** The bits define the differential peak voltage (in V_{PP}) at which the analog input signal is clipped when in IOR mode. In IOR mode the analog clipping is set to 1.746 V_{PP}. In the default ADC mode clipping of the analog input signal is disabled. Should it be decided to over-ride the default setting, it is important to follow the guidelines for setting OL, as described in the Applications Information section.

OL[3:0]	Clipping Voltage V_{PP}
0 (IOR Mode default)	1.746
0001	1.694
0010	1.64
0011	1.586
0100	1.534
0101	1.480
0110	1.426
0111	1.374
1000	2.172
1001	2.120
1010	2.066
1011	2.012
1100	1.960
1101	1.906
1110	1.852
1111	1.800

PLL Control Register

Address: 08h

Attributes Write Only.

Register 09h reads back contents of register 08h.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	Reserved						SHBW	STCAL	
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:2	**Reserved.** Write as zero for future compatibility.
1	**SHBW: Set PLL to High Bandwidth.** The selection of the PLL bandwidth permits to set the sensitivity of the PLL to input clock jitter. Less bandwidth decreases the sensitivity to input clock jitter. The PLL Bandwidth is related to the sampling frequency, the exact values of which can be found in the electrical specifications table. The PLL will pass any input clock jitter up to the PLL bandwidth, while jitter above the PLL bandwidth will be attenuated. Low bandwidth mode should be used for high jitter input clocks, while high bandwidth mode can be used for high-quality, low jitter input clocks. 0 PLL bandwidth is set to Low Bandwidth (400kHz). 1 PLL bandwidth is set to High Bandwidth (1.4MHz).
0	**STCAL: Start VCO calibration.** The calibration can be manually started in order to assure that the frequency tuning margin is maximum, for example, in case of large temperature change during operation it can be useful to restart the calibration. 0 The VCO calibration starts automatically if a Loss of Lock is detected 1 The VCO calibration is restarted.

LVDS Input Clock – Hysteresis

Address: 0Ah
Attributes: Write Only.
Register 0Bh reads back contents of register 0Ah.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	Reserved		INVCLK	100HYS	50HYS	20HYS	10HYS OFF	HYSOFF	
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:6	**Reserved.** Write as zero for future compatibility.
5	**INVCLK: Invert Input Reference Clock.** This bit is used to invert the input clock. 0 Reference input clock not inverted. 1 Reference input clock inverted.
4	**100HYS: Enable 100mV hysteresis**. This bit enables 100mV hysteresis. It should be used for a CMOS input clock only. 0 Normal operation (10mV hysteresis) 1 100mV hysteresis (CMOS input clock only)
3	**50HYS: Enable 50mV hysteresis.** This bit enables 50mV hysteresis. It should be used for a CMOS input clock only. 0 Normal operation (10mV hysteresis) 1 50mV hysteresis. (CMOS input clock only)
2	**20HYS: Enable 20mV hysteresis.** This bit enables 20mV hysteresis. It should be used for an LVDS input clock only. 0 Normal operation (10mV hysteresis) 1 20mV hysteresis. (LVDS input clock only)
1	**10HYSOFF: Disable 10mV hysteresis.** 10mV hysteresis is the default setting. This bit is used to disable 10mV hysteresis, in the case where another hysteresis setting is desired, for example when using a CMOS input clock. 0 10mV hysteresis. (LVDS input clock only) 1 10mV hysteresis disabled.
0	**HYSOFF: Disable all hysteresis settings.** This bit is used to disable all hysteresis settings. 0 Normal operation (10mV hysteresis) 1 All hysteresis settings disabled.

Serializer Custom Pattern 0 Register

Address: 10h
Attributes Write Only.
Register 11h reads back contents of Register 10h.

This register in conjunction with User Register 12 provides storage for the custom de-skew pattern. See User Register 16 for a description of how this training sequence is used.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	Custom Pattern [7:0]								
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:0	**Custom Pattern [7:0].** This pattern forms the lower byte of Custom Pattern [11:0] which is output by the serializer when the Training Sequence Select bits (bits 1:0) of the Decimator Control Register are set to select Training sequence 3.

Serializer Custom Pattern 1 Register

Address: 12h
Attributes Write Only.
Register 13h reads back contents of Register 12h.

This register in conjunction with User Register 10 provides storage for the custom de-skew pattern. See User Register 16 for a description of how this training sequence is used.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	Reserved				Custom Pattern [11:8]				
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:4	**Reserved.** Write as zero for future compatibility.
3:0	**Custom Pattern [11:8].** This pattern forms the upper 4 bits of Custom Pattern [11:0] which is output by the serializer when the Training Sequence Select bits (bits 1:0) of the Decimator Control Register are set to select Training sequence 3.

Decimator Clipping Control Register

Address: 14h
Attributes Write Only.
Register 15h reads back contents of Register 14h.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	CGS	Reserved	a[2:0]			b[2:0]			
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7	**CGS: Custom Gain Setting**. This bit is used to override the automatic gain settings for ADC and IOR modes. If the user wishes to write a custom digital gain coefficient using a[2:0] and b[2:0] of this register, then the CGS bit must be set. 0 Normal operation Automatic gain settings used 1 Custom Gain Setting Gain setting from a[2:0] and b[2:0] used.
6	**Reserved.** Write as zero for future compatibility.
5:3	**a[2:0]: Digital Gain Coefficient.** In clipping mode the input range of an ADC channel is limited to 1.56Vpp. In ADC mode the input range is 2.10Vpp. The output of the digital filter has to be scaled according to the selected mode (the filter data has to be mapped in to the 12bit output data), the difference between 1.6Vpp and 2.2Vpp is -2.6dB, hence the digital filter gain has to be set to 2.6dB when in IOR mode and to 0dB when in clipping mode (default mode) . This is performed by setting a Digital Gain Factor which is calculated using the following formula: $DGF = \frac{32 + 4 \times DGFa + DGFb}{26}$ The mapping of the coefficient values for a[2:0] is as follows: 011 = Not used. Defaults to 2 010 = 2 001 = 1 000 = 0 111 = -1 110 = -2 101 = Not used. Defaults to -2 100 = Not used. Defaults to -2 The mapping of the coefficient values for b[2:0] is shown below. The table on the following page shows the available Digital Gain Coefficient settings.
2:0	**b[2:0]: Digital Gain Coefficient.** The mapping of the coefficient values for b[2:0] is as follows: 011 = Not used. Defaults to 2 010 = 2 001 = 1 000 = 0 111 = -1 110 = -2 101 = Not used. Defaults to -2 100 = Not used. Defaults to -2

Coefficent a[2:0]	Coefficent b[2:0]	Digital Gain (dB)	Equivalent full scale input range (V_{PP})	
010	010	4.16	1.30	
010	001	3.95	1.33	
010	000	3.74	1.37	
010	111	3.52	1.40	
010	110	3.29	1.44	
001	001	3.06	1.48	
001	000	2.82	1.52	
001	**111**	**2.58**	**1.56**	**IOR Mode default setting**
001	110	2.33	1.61	
000	001	2.07	1.65	
000	000	1.80	1.71	
000	111	1.53	1.76	
000	110	1.24	1.82	
111	001	0.95	1.88	
111	000	0.64	1.95	
111	111	0.33	2.02	
111	**110**	**000**	**2.10**	**ADC mode default setting**
110	001	-0.34	2.18	
110	000	-0.70	2.28	
110	111	-1.07	2.38	
110	110	-1.45	2.48	

Decimator Control Register

Address: 16h
Attributes Write Only.
Register 17h reads back contents of register 16h.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	Reserved			EQON	DFS	MSB	TSEL[1:0]		
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:5	**Reserved.** Write as zero for future compatibility.
4	**EQON: Equalizer Enable.** This bit is used to enable or disable the digital equalizer. The equalizer can be switched on in order to reduce the group delay of the output data, at the cost of increased power. 0 Equalizer disabled 1 Equalizer enabled
3	**DFS: Data Format Select.** Selects the format, either Offset Binary or Twos Complement of the output data 0 2s Complement 1 Offset Binary
2	**MSB:** Select the bit order of the LVDS output data stream 0 LSB first 1 MSB first
1:0	**TSEL[1:0]: Training Sequence Select**. These bits select the LVDS output data. The default mode of operation is where the filter output data is serialized. In the remaining modes the selected training sequence is repeatedly output from the serializer this allows the receiving data capture circuitry to perform the de-skewing process. One of three known words can be selected, the first two words are hard-coded in the block, the third one, the custom pattern, is written into **User Registers 10h** and **12h** the **Serializer Custom Pattern Registers.** Note. The outputs bit-clock and word-clock are not affected by the value of the Training Sequence Select bits. 00 ADC data[11:0] 01 Training sequence 1: 000000111111 10 Training sequence 2: 101010101010 11 Training sequence 3: custom pattern

LVDS Control Register

Address: 18h
Attributes Write Only.
Register 19h reads back contents of register 18h.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	Reserved			TX_term	I_drive[1:0]		OCM	SLVS	
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:5	**Reserved.** Write as zero for future compatibility.
4	**TX_term:** Enable Internal 100 Ohm termination for data outputs. 0 Internal 100 ohm termination disabled 1 Internal 100 ohm termination enabled
3:2	**I_drive[1:0]:** Controls the current drive of the data outputs. 00 2.5 mA 01 3.5 mA 10 Reserved 11 5 mA
1	**OCM:** Output Common mode. Allows the output common mode to be shifted depending on the setting of V_{DR}. If bit 0 of this register, SLVS, is set to 1 then changing OCM will have no impact on the output common mode. The output common mode in SLVS mode is fixed, as described in the Electrical Specifications section of this datasheet. For V_{DR} = 1.2V, OCM must be set to 0. For V_{DR} = 1.8V, OCM must be set to 1. 0 Output Common Mode, V_{OCM} = 1.0V 1 Output Common Mode, V_{OCM} = 1.25V
0	**SLVS:** Select the format for output data, either LVDS or SLVS. The differences in timing and electrical specifications between the two modes can be seen in the Electrical Specifications section of the datasheet. If this bit is set to 1 (SLVS mode), OCM has no effect and the output common mode will be set for SLVS as described in the Electrical Specifications section of this datasheet. When LVDS mode is selected, the output common mode must be selected using the OCM bit of this register. 0 LVDS Mode 1 SLVS Mode

Chip ID Register

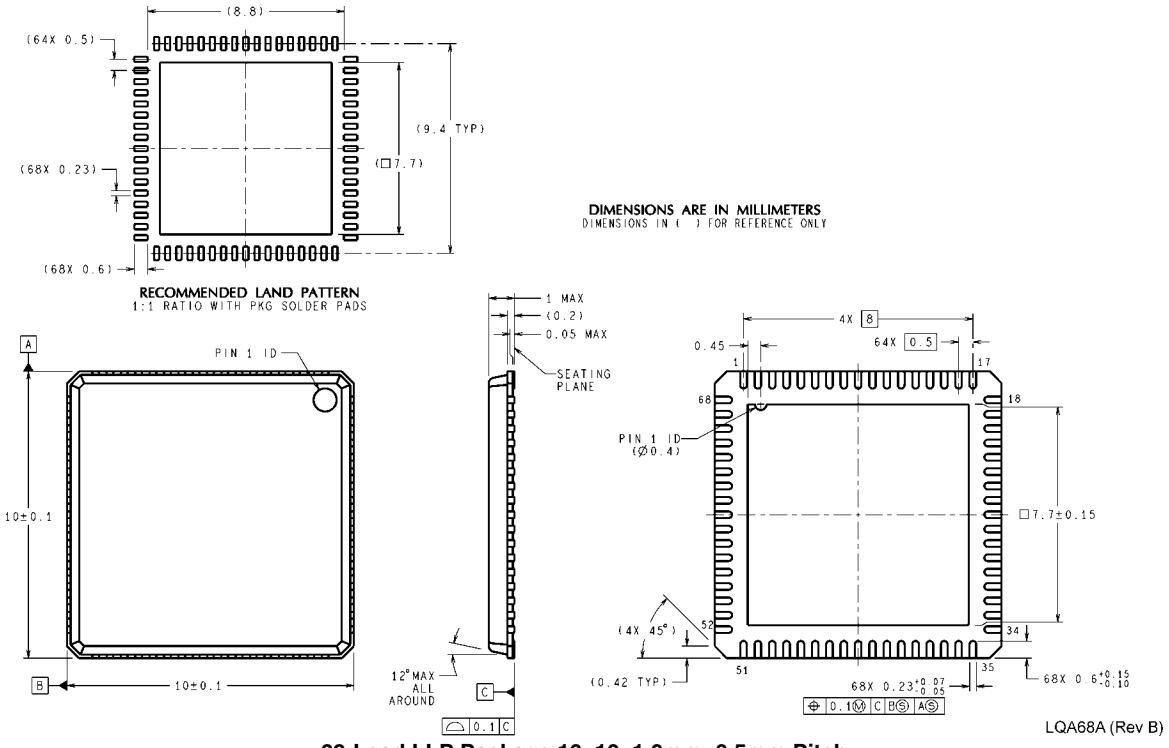
Address: 1Eh

Attributes Read Only.

	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	HEX
Description	ID [7:0]								
Default	0	0	0	0	0	0	0	0	00 h

Bit	Description
7:0	**ID[7:0]: Chip ID Register.** Reading from this register will provide the chip version. The expected Chip ID for the ADC12EU050 is 12.4. X = ID[7]*8 + ID[6]*4 + ID[5]*2 + ID[4] Y = ID[3]*8 + ID[2]*4 + ID[1]*2 + ID[0] Chip ID = Version X.Y

Physical Dimensions inches (millimeters) unless otherwise noted



68-Lead LLP Package 10x10x1.0mm, 0.5mm Pitch
Ordering Numbers ADC12EU050CIPLQ
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Notes

Notes

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