MP4655

Pure, Single-Stage, LLC, LED Current and System Voltage Controller

The Future of Analog IC Technology

DESCRIPTION

The MP4655 is a pure, single-stage, LLC, LED current and system voltage controller for LED backlighting, especially in larger TVs, and is located on the secondary side. The MP4655 uses an LLC power stage and an extra N-channel MOSFET to regulate both the LED current and the system supply voltage. The MP4655 is powered by input supplies ranging from 9V to 35V that output two 180 degree phase shifted driving signals for the external LLC power stages. Its enhanced 12V gate driver provides sufficient driving capability and can drive the external LLC MOSFETs directly through an external gate-driving transformer. The MP4655 also provides a direct driving signal to control the extra N-channel MOSFET and regulate the system supply voltage.

The MP4655 incorporates both PWM dimming and analog dimming for the LED current. A driving signal is output to directly drive the dimming MOSFET, which helps achieve fast and high-contrast ratio PWM dimming. The analog dimming can be achieved through a DC signal on ADIM or a pulse signal on ADIMP.

The MP4655 employs smart protection methods to protect the LED driver stage and system power stage in the event that a fault occurs, increasing system reliability.

Full protection features for the LED include open LED protection, short LED protection, over-LED current protection, feedback open loop protection, and protection for any point of the LED string shorting to ground.

Full protection features for the system supply voltage stage include over-voltage protection (OVP), over-current protection (OCP), and feedback open-loop protection. The MP4655 uses an extra individual capacitive mode protection to protect the LLC power stage in any condition system in the event it enters capacitive mode. The MP4655 also employs thermal shutdown and is available in a SOIC-28 package.

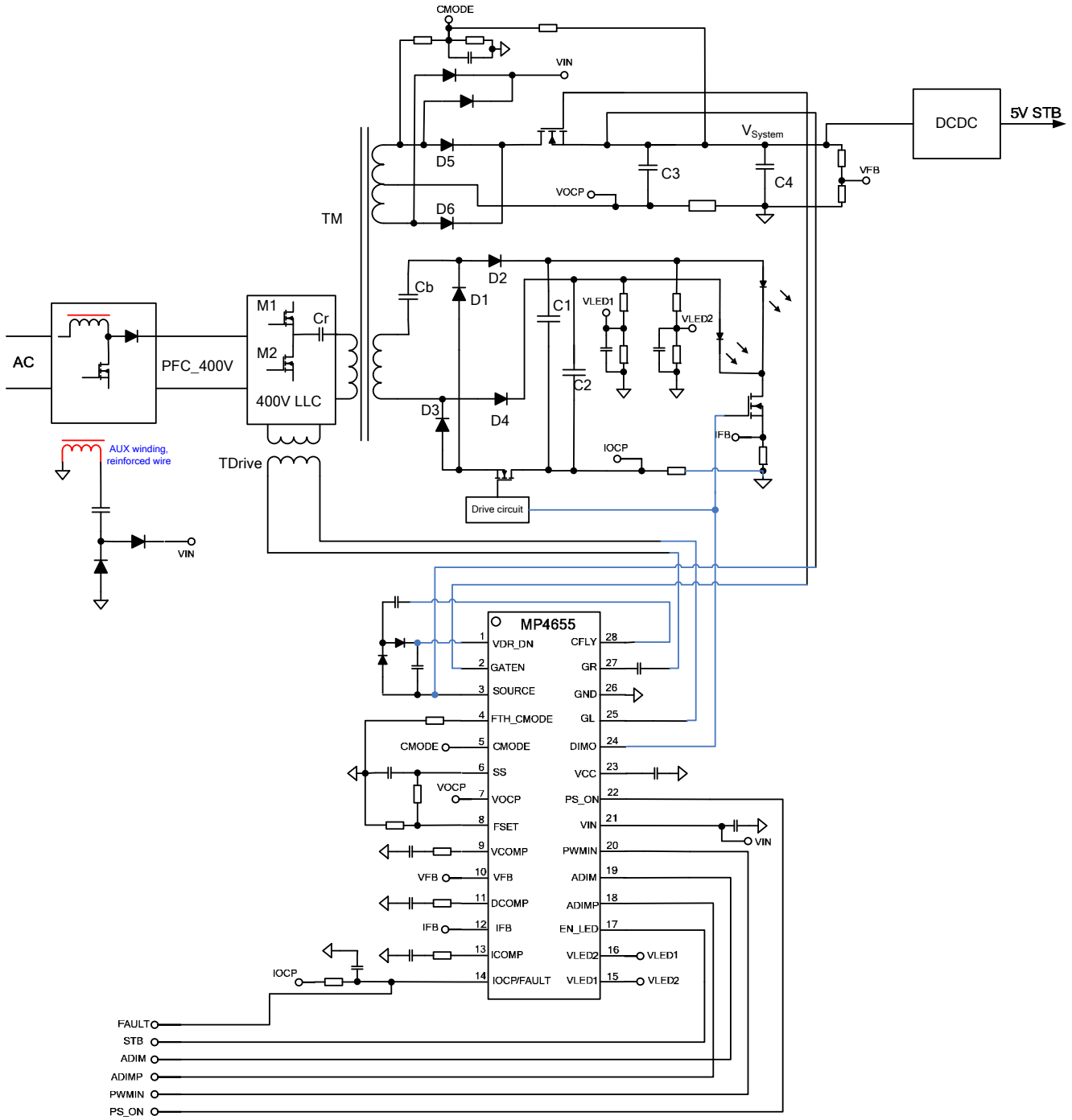
FEATURES

- Pure, 1-Stage LLC for LED Current and System Supply Voltage Regulation
- CC/CV Frequency Control Loop and Duty Cycle Control Loop
- Audible Noise Elimination
- 9V to 35V Input Voltage Range
- Deep and Fast PWM Dimming
- Analog Dimming with DC or Pulse Input Signal
- Input Under-Voltage Lockout (UVLO)
- System Supply Over-Voltage Protection (OVP)
- System Supply Short Protection
- LED Open, LED Short Protection
- LED String Short to GND Protection
- Open Feedback Loop Protection for System Bus Voltage and LED Driver
- Capacitive Mode Protection for LLC
- Soft Switching for the Extra N-Channel MOSFET
- Fault Indicator
- Available in a SOIC-28 Package

APPLICATIONS

- LCD TVs and Monitors
- Desktop LCD Flat Panel Displays
- Flat Panel Video Displays
- Street Lighting

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4655GY	SOIC-28	*See Below*

*For Tape & Reel, add suffix –Z (eg. MP4655GY–Z)

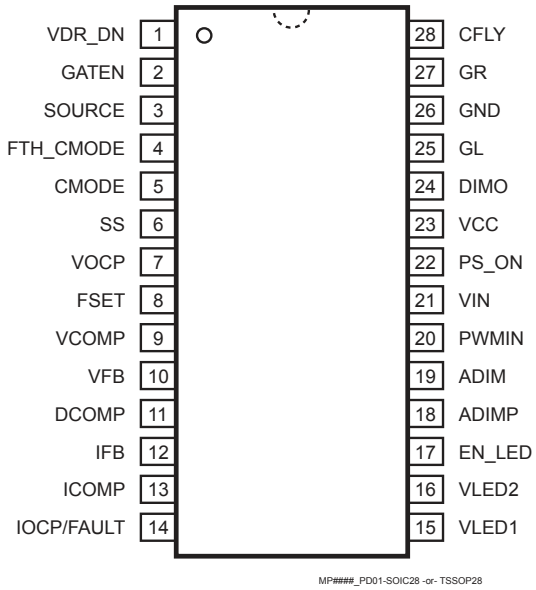
TOP MARKING

MPSYYWW
MP4655
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4655: Product code of MP4655GY
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



SOIC-28

ABSOLUTE MAXIMUM RATINGS (1)

VIN, PS_ON, PWMIN .....-0.3V to 40V
GL, GR, VCC, DIMO, CFLY.....-0.3V to 18V
SOURCE .....-0.3V to 30V
VDR_DN, GATEN.....-0.3V to 48V
VDR_DN - SOURCE, GATEN - SOURCE…….
.....-0.3V to 18V
IOCP/FAULT, VOCP, CMODE .....-6.5V to 6V
Other pins .....-0.3V to 6.5V
Junction temperature .....150°C
Continuous power dissipation (T_A = +25°C) (2)
SOIC-28 ..... 2.1W
Storage temperature ..... -65°C to +150°C
Operating frequency 400kHz

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....-0.3V to 35V
Operating frequency ..... 20kHz to 350kHz
Operating junction temp. ..... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOIC-28	60	30	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 13V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN Supply						
VIN supply range			9		35	V
Quiescent current	I_Q	PS_ON = 5V, no gate driver		1.6	1.9	mA
Shutdown current	$I_{shutdown}$	PS_ON = 1.5V		106	120	µA
Standby current	I_{STB}	PS_ON = 0V		0.6	0.8	mA
Gate Driver GL, GR (LLC Power Stage)						
Gate pull-down resistance	R_{GD}	I_{gate} = 20mA		2		Ω
Gate pull-up resistance	R_{GU}	I_{gate} = 20mA		8		Ω
Output source current	I_{SOURCE}	With 1nF load		0.5 (5)		A
Output sink current	I_{SINK}	With 1nF load		1 (5)		A
Dead time	t_{dead}		400	600	800	ns
Gate Driver Supply Voltage (VCC)						
Voltage	V_{VCC}	I_{VCC} = 0mA	11.5	12.5	13.5	V
		I_{VCC} = 30mA	11.3	12.3	13.3	V
		I_{VCC} = 50mA	11.2	12.2	13.2	V
Voltage dropout		I_{VCC} = 50mA, VIN = 10V		0.53		V
VCC UVLO threshold	$V_{TH\_UVLO\_VCC}$	VCC rising	7.2	7.74	8.2	V
VCC UVLO hysteresis	$V_{TH\_VCC\_HYST}$		1.8	2.05	2.3	V
Gate Driver (GATEN, for Extra MOSFET on V_{system})						
GATEN pull-down resistance	R_{GD}	I_{gate} = 20mA		2.5		Ω
GATEN pull-up resistance	R_{GU}	I_{gate} = 20mA		9		Ω
Output source current	I_{SOURCE_GATEN}	With 1nF load		0.5 (5)		A
Output sink current	I_{SINK_GATEN}	With 1nF load		1 (5)		A
GATEN Supply Voltage (VDR_DN)						
Charge pump pull-up resistor				13		Ω
Charge pump pull-down resistor				4		Ω
Charge pump frequency	$f_{chargepump}$			455		kHz
VDR_DN upper threshold to stop charge pump in standby mode	$V_{th\_upper\_STB}$	Detection circuit, very small leakage		VCC - 2.5		V
VDR_DN valley threshold to recover charge pump in standby mode	$V_{th\_valley\_STB}$	VCC - 5.5 > 5V		VCC - 5.5		V
		VCC - 5.5 < 5V		5		
Leakage current from SOURCE	I_{lkg_SOURCE}	V_{SOURCE} = 24V, charge pump disabled			0.2	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Analog Dimming						
Analog dimming full scale	V_{ADMAX}	VIFB = 200mV	2.32	2.39	2.46	V
Dimming linearity	VIFB_ADIM	VADIM = 1.2V		100		mV
Dimming linearity	VIFB_ADIM	VADIM = 0.8V		66.8		mV
Dimming linearity	VIFB_ADIM	VADIM = 0.3V		25		mV
Dimming linearity	VIFB_ADIM	VADIM = 0.1V		8.5		mV
ADIMP logic high	VADIM_PHI		1.8		3.5	V
ADIMP logic low	VADIM_PLO				0.9	V
ADIMP pull-up resistor	RADIM_P_UP			1.5		MΩ
ADIMP disable threshold			4.7			V
PWM Dimming						
PWM logic high threshold	V_{TH-PWM}	PWM dimming	1.4	17	2	V
PWM logic input hysteresis	$V_{TH-PWM-Hyst}$	PWM dimming		0.6		V
Operating Frequency						
Minimum frequency set voltage	V_{FSET}	IFB = 0.1V, PWMIN = high	1.65	1.73	1.83	V
Minimum operating frequency	F_{min_op}	R_{FSET} = R_{SS_FSET} = 300kΩ, IFB = 0.1V, PWMIN = high		42.5		kHz
Maximum operating frequency	F_{max_op}	R_{FSET} = R_{SS_FSET} = 300kΩ, IFB = 0.21V, PWMIN = high		130		kHz
Output PWM Dimming Signal for LED (DIMO)						
Logic high voltage	V_{H-DIMO}	Normal operation		12.5		V
Logic low voltage	V_{L-DIMO}	At fault condition, or PWMIN is low			0.1	V
DIMO up-side resistance		20mA drive source current for design		62		Ω
DIMO low-side resistance		100mA drive sink current for design		7		Ω
LED Stage Enable (EN_LED)						
EN_LED logic high threshold	V_{TH-EN_LED}	EN_LED rising	1.4	1.7	2	V
EN_LED logic input hysteresis	$V_{TH-ENLED-Hyst}$			0.6		V
IC Enable Signal (PS_ON)						
Threshold for IC standby	$V_{th\_PS\_ON\_STB}$	Rising edge	0.7	0.8	0.9	V
Duration time to shut down IC		$V_{th\_PS\_ON\_STB}$ < V_{PS_ON} < $V_{th\_PS\_ON}$		1		ms
Threshold to turn on IC to operate normally	$V_{th\_PS\_ON}$		1.9	2	2.1	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Capacitive Mode Detection (CMODE)						
CMODE detection high threshold	$V_{th\_Cmode\_H}$	At GL falling edge		0.97		V_{REF_VFB}
CMODE detection low threshold	$V_{th\_Cmode\_L}$	At GR falling edge		0.03		V_{REF_VFB}
FTH_CMODE voltage	V_{Fth_Cmode}		1.15	1.2	1.25	V
CMODE threshold frequency	F_{th_cmode}	150kΩ on FTH_CMODE		91		kHz
Soft Start (SS)						
Soft-start final voltage	V_{SS}	Normal operation after start-up	2.34	2.405	2.47	
Soft-start current	I_{SS}	V_{SS} = 1V		13		µA
Discharge current when capacitive mode detected	$I_{SS\_Discharge}$	V_{SS} = 2V		3		I_{SS}
Pull low resistor at latch-up				120		Ω
LED Current Feedback (IFB)						
Magnitude	$\|V_{IFB}\|$		0.188	0.199	0.21	V
LED short threshold for immediate action	V_{IFBS}		490	555	610	mV
LED short detection delay time	$T_{blankTdelay}$			6		us
LED short threshold for slow action	V_{IFBSC}		370	415	460	mV
Delay time for slow action	T_{delay_IFB}	400mV < V_{IFB} < 600mV	250	340	450	µs
Threshold for short protection		ICOMP saturated		50%		V_{IFB_REF} (6)
Duration for short protection				1024		cycle
Internal Current Loop Compensation Transconductance Op-Amp (ICOMP)						
Transconductance	Gm_I			840		µA/V
Saturated output current	I_{sat_I}		30	50	70	µA
Low-level clamp voltage	VICOMP_L	Normal operation	0.97	1.02	1.07	V
High-level clamp votlage	VICOMP_H	Normal operation	2.2	2.28	2.36	V
Output for System Voltage Feedback (VFB)						
Reference voltage	V_{REF_VFB}		1.17	1.2	1.23	V
Leakage current	I_{lkg_VFB}	Normal operation		0.33		µA
Internal Voltage Loop Compensation Transconductance Op-Amp (VCOMP)						
Low-level clamp voltage	V_{VCOMP_L}	Normal operation	0.97	1.02	1.07	V
High-level clamp votlage	V_{VCOMP_H}	Normal operation	2.2	2.28	2.36	V
Transconductance	Gm_V			150		µA/V
Saturated output current	I_{sat_V}		30	50	70	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal Voltage Loop Compensation Transconductance Op-Amp for Extra MOSFET Control (DCOMP)						
Low-level clamp voltage	V_{DCOMP_L}	Normal operation, VOCP = 0V		0.41		V
High-level clamp votlage	V_{DCOMP_H}	Normal operation, VOCP = 0V		2.1		V
Transconductance	G_{m_DCOMP}			150		μA/V
Saturated output current	I_{sat_DCOMP}		30	50	70	μA
Bus Voltage Stage Current Detection (VOCP)						
VOCP detection threshold	V_{TH_VOCP}		-230	-203	-176	mV
VOCP delay time	T_{D_VOCP}	OCP < -200mV		7		μs
Over LED Voltage Protection (VLED1, VLED2)						
Over LED voltage protection threshold	$V_{TH\_OVP\_LED}$		2.33	2.41	2.49	V
Over LED voltage delay time	T_{delay_VLED}			8		μs
Gain of differential voltage protection			14	16.	18	
Internal resistance	R_{VLED}		16	20	24	kΩ
Over LED voltage to latch up LLC	$V_{TH\_OVP\_LED\_latch}$		2.85	3	3.15	V
Duration time to latch up				7.6		μs
Burst Mode (Pulse Skipping) Threshold at Normal Operation (VCOMP, ICOMP, VFB, IFB)						
VCOMP threshold for burst mode	$V_{TH\_burst\_VCOMP}$	PS_ON = H, VFB > 1.05V_{REF_VFB}	1.05	1.1	1.15	V
VCOMP hysteresis for burst mode		PS_ON = H	80	100	120	mV
VFB threshold for burst mode	$V_{TH\_burst\_VFB}$	PS_ON = H		1.05		V_{REF_VFB}
VFB reset threshold for burst mode	$V_{TH\_reset\_burst\_VFB}$	PS_ON = H		0.95		V_{REF_VFB}
ICOMP threshold for burst mode	$V_{TH\_burst\_ICOMP}$	PS_ON = H, V_{IFB} > 1.08V_{IFB_REF}	1.05	1.12	1.18	V
ICOMP hysteresis for burst mode				100		mV
IFB threshold for burst mode	$V_{TH\_burst\_IFB}$	PS_ON = H		1.08		V_{IFB_REF} (6)
IFB reset threshold for burst mode	$V_{TH\_reset\_burst\_IFB}$	PS_ON = H		0.92		V_{IFB_REF} (6)

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 13V, T_A = +25°C, unless otherwise noted.

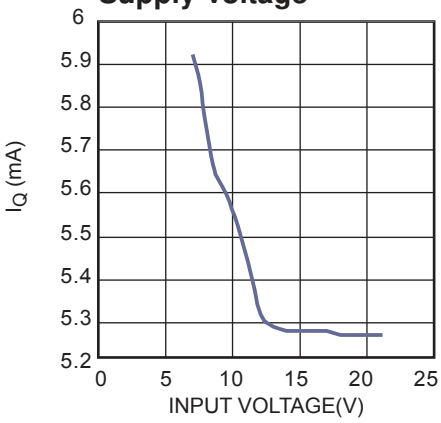
Parameter	Symbol	Condition	Min	Typ	Max	Units
Burst Mode (Pulse Skipping) Threshold in Standby Mode (VCOMP, VFB)						
VFB threshold to stop gate driver				1.05		V_{REF_VFB}
VFB threshold to recover gate driver				0.95		V_{REF_VFB}
FSET voltage at standby mode	VFSET _STB	PS_ON < 0.7V, VFB = 0.8 * VREF_VFB		2.1		V
VSS low clamp value				0.91		V
VSS soft-on recovery current				100		µA
VSS soft-off recovery current				100		µA
System Voltage Protection (VFB)						
Overbus voltage protection threshold	$V_{TH\_OVP\_VFB}$			1.25		V_{REF_VFB}
Delay time		VFB > 1.5V		7		µs
VFB open protection threshold	$V_{TH\_Open\_VFB}$			50%		V_{REF_VFB}
Duration time for VFB open protection		VCOMP saturated at PWM off or DCOMP saturated at PWM ON		512		cycles
LED Stage Over-Current Detection (IOCP/FAULT)						
IOCP threshold	V_{TH_IOCP}		-360	-320	-280	mV
IOCP detection delay time	T_{D_IOCP}	IOCP < -310mV		7		µs
IOCP duration time to latch up LLC		LED driver stage protection triggered and IOCP < -300mV		270		µs
Amplitude of output fault signal	V_{Fault}	Pin floated, fault condition I_{SOURCE} = 10mA	3.2	3.4	3.6	V
Pull-up resistance at fault condition					0.3	kΩ
Source current of ICOP at normal operation				5		µA

NOTES:

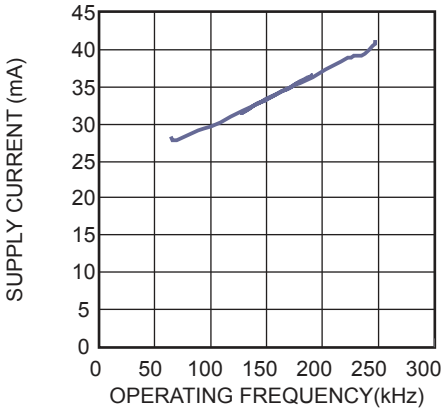
5) The parameters are tested on the bench with several parts.
6) VIFB_REF is the reference voltage for IFB. Its value changes according to the ADIM signal.

TYPICAL CHARACTERISTICS

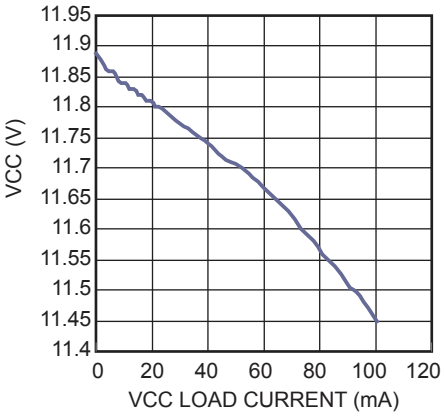
Quiescent Current vs. Supply Voltage



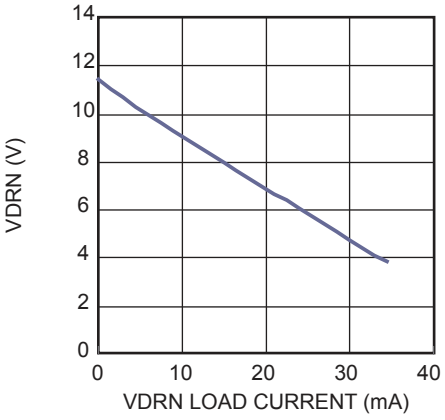
Supply Current vs. Operating Frequency



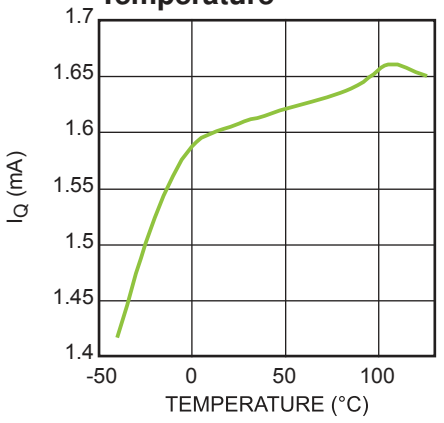
VCC Drive Capability



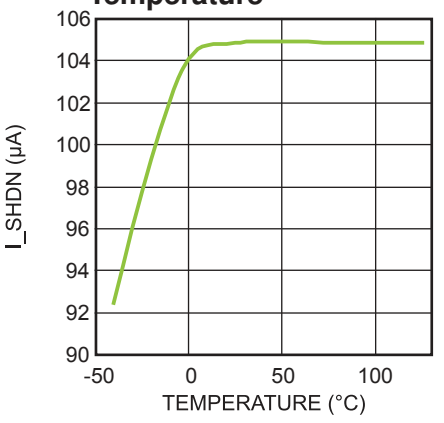
VDRN Drive Capability



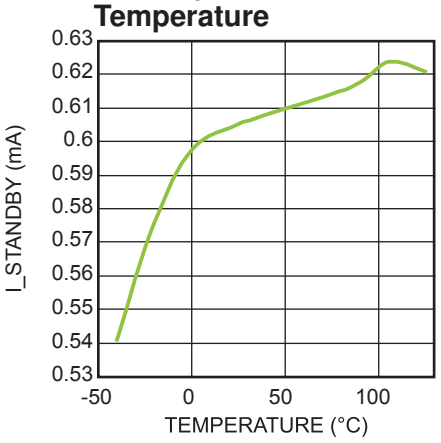
Quiescent Current vs. Temperature



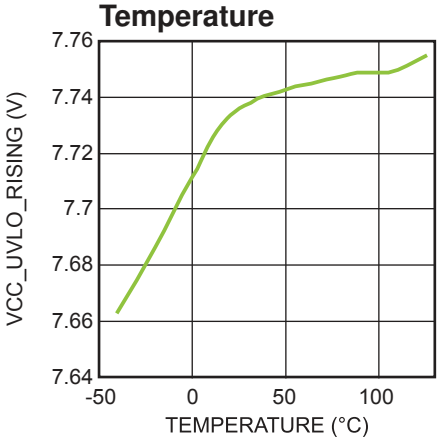
Shutdown Current vs. Temperature



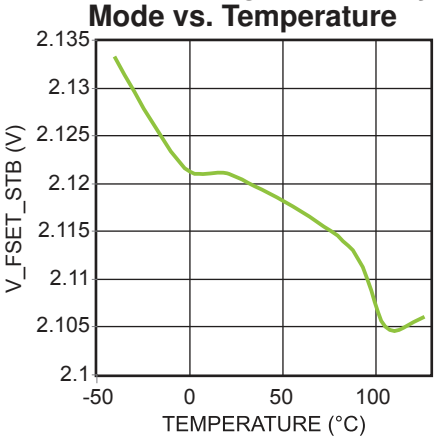
Standby Current vs. Temperature



VCC UVLO vs. Temperature

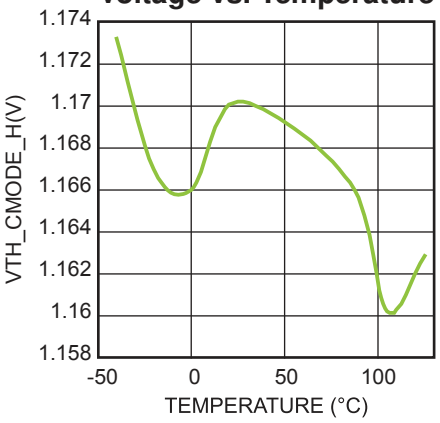


FSET Voltage at Standby Mode vs. Temperature

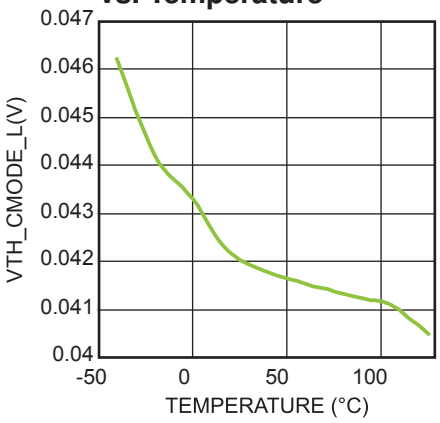


TYPICAL CHARACTERISTICS *(continued)*

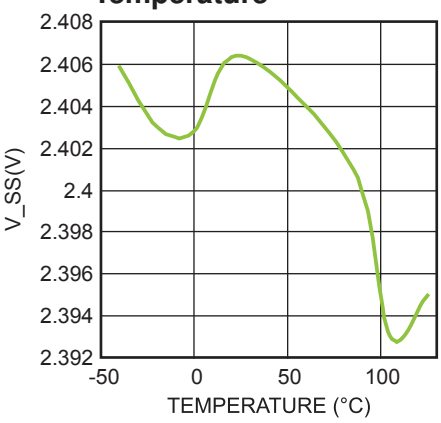
CMODE High-Level Threshold Voltage vs. Temperature



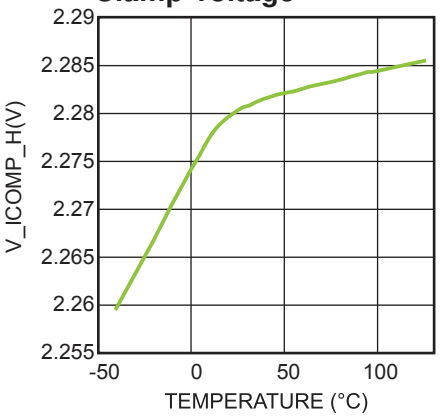
CMODE Low-Level Threshold vs. Temperature



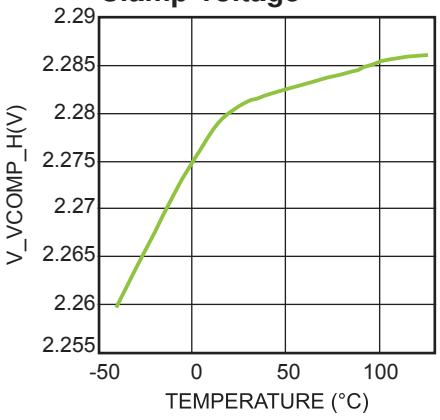
VSS Voltage vs. Temperature



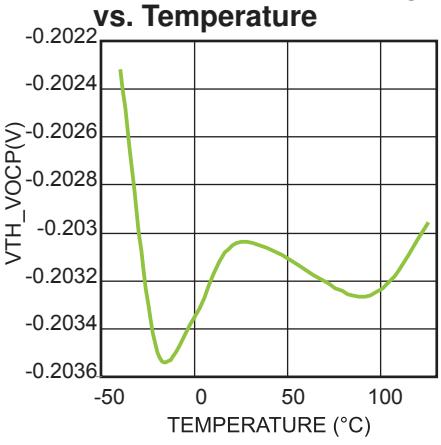
ICOMP High-Level Clamp Voltage



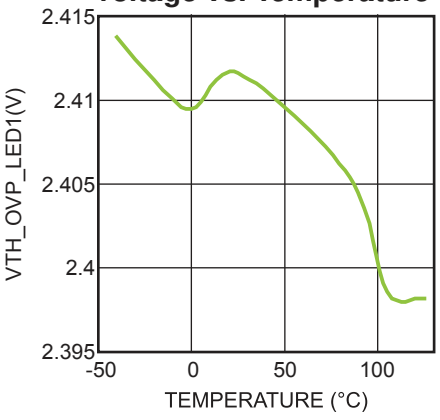
VCOMP High-Level Clamp Voltage



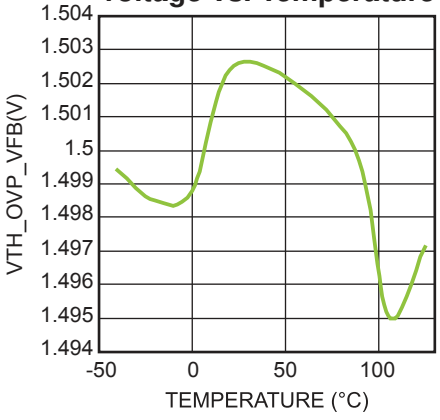
VOCP Threshold Voltage vs. Temperature



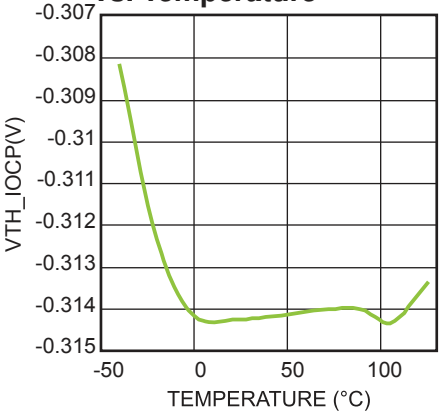
VLED OVP Threshold Voltage vs. Temperature



VFB OVP Threshold Voltage vs. Temperature

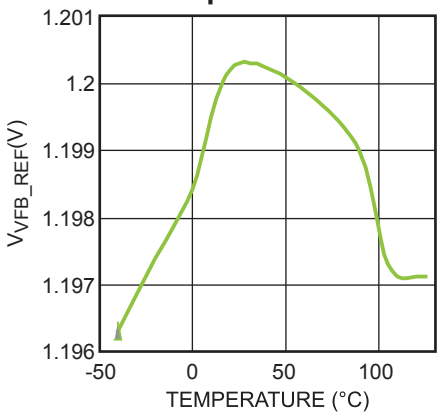


IOCP Threshold Voltage vs. Temperature

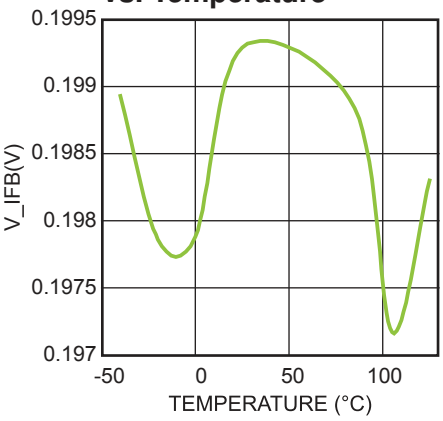


TYPICAL CHARACTERISTICS *(continued)*

VFB Reference Voltage vs. Temperature



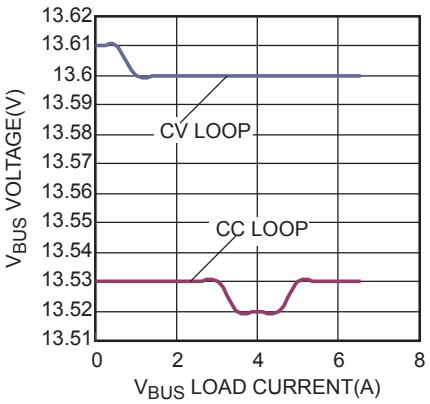
IFB Reference Voltage vs. Temperature



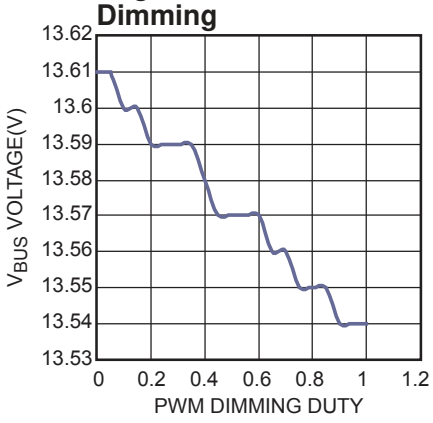
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. 400V_{bus} = 390V, V_{LED} = 130V, ILED = 375mA*2 strings, System output = 13.5V/6.5A, T_A = 25°C, unless otherwise noted.

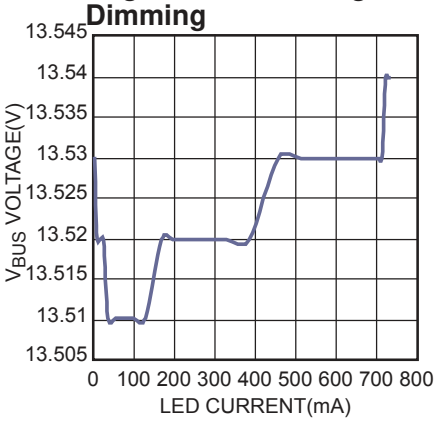
V_{BUS} Voltage Load Regulation



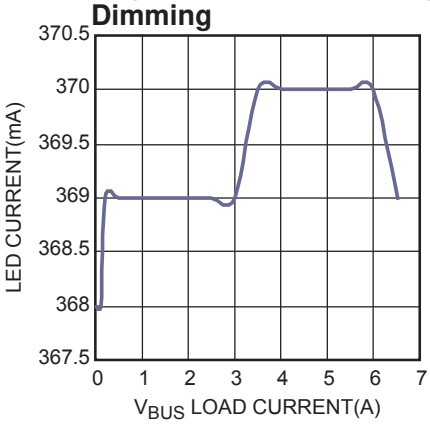
V_{BUS} Voltage Cross Regulation at PWM Dimming



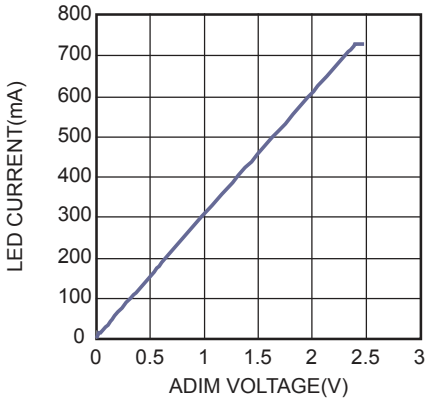
V_{BUS} Voltage Cross Regulation at Analog Dimming



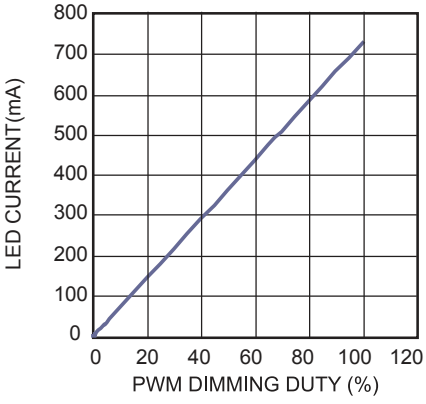
LED Current Cross Regulation at 50% Analog Dimming



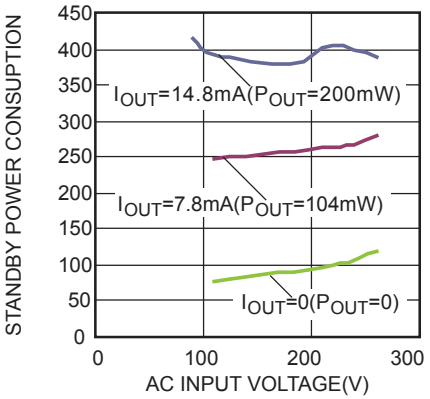
LED Current Analog Dimming Linearity



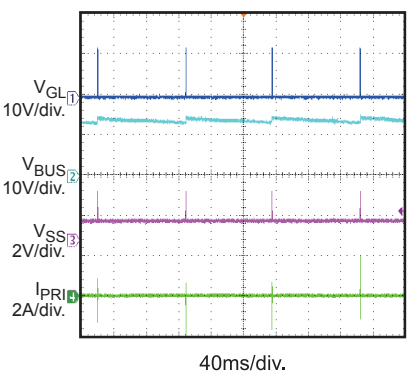
LED Current PWM Dimming Linearity



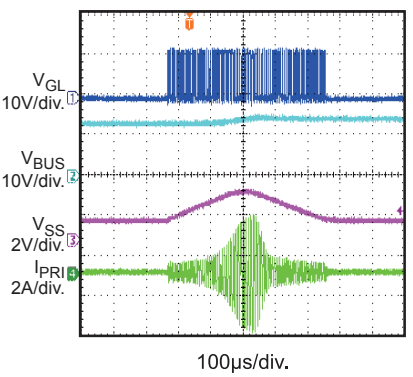
Standby Power Consumption



Standby Mode Opeartion



Standby Mode Opeartion

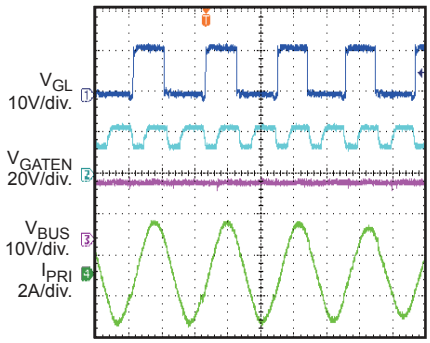


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

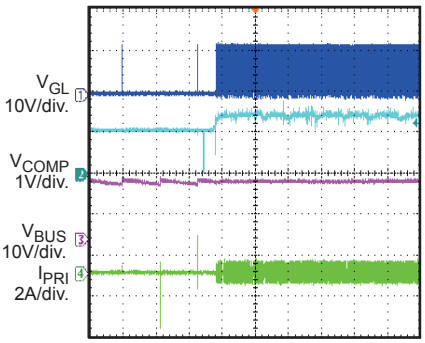
Performance waveforms are tested on the evaluation board of the Design Example section. 400V_{bus} = 390V, V_{LED} = 130V, ILED = 375mA*2 strings, System output = 13.5V/6.5A, T_A = 25°C, unless otherwise noted.

Normal Operation

PWM=High

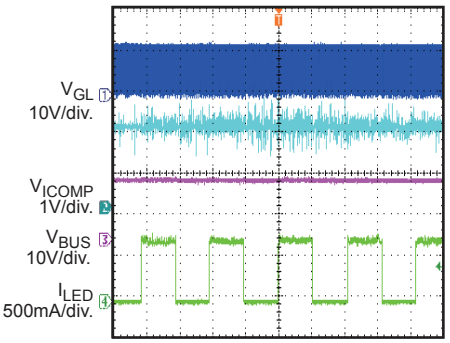


PSON Start-Up

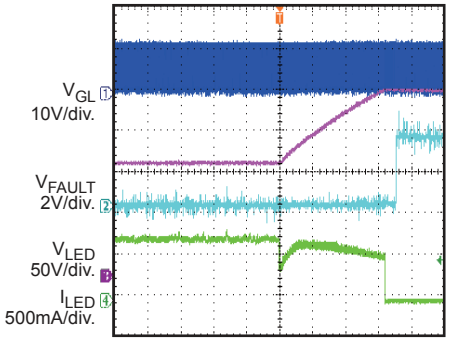


PWM Dimming

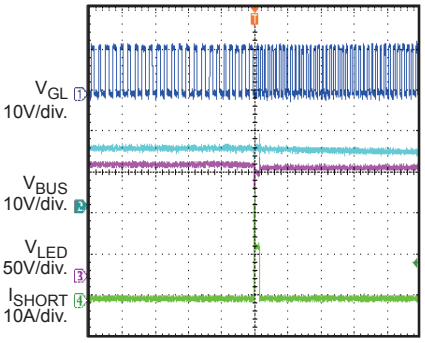
50%



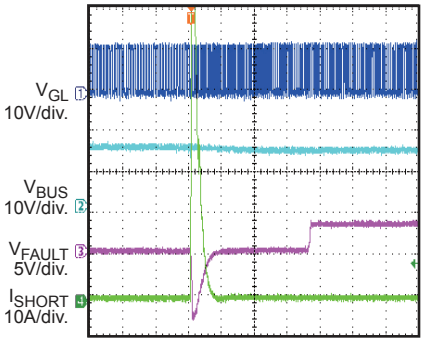
Open LED Protection



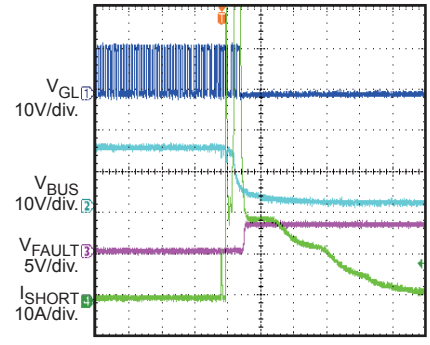
Short LED+ to LED-



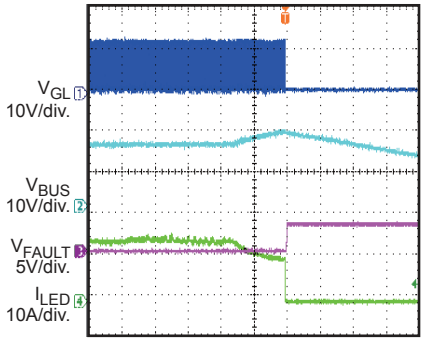
Short LED+ to GND



Short V_{BUS} to GND



V_{BUS} OVP Protection



PIN FUNCTIONS

Pin #	Name	Description
1	VDR_DN	**Drive voltage for the extra MOSFET.** VDR_DN is formed by the charge pump and is referred to SOURCE.
2	GATEN	**Gate of the extra N-channel MOSFET.**
3	SOURCE	**Source of the extra N-channel MOSFET.**
4	FTH_CMODE	**FTH_CMODE sets the threshold frequency to shut down the LLC when capacitive mode is detected.** Its typical voltage is 1.2V. The sourcing current through FTH_CMODE determines the threshold frequency. When capacitive mode is detected, the IC discharges SS and increases the operating frequency. If the operating frequency is higher than this threshold frequency when capacitive mode is detected, the IC latches up LLC and the IOCP/FAULT signal output is high.
5	CMODE	**Detection of capacitive mode.** The secondary side winding voltage is fed back on CMODE for capacitive mode detection.
6	SS	**Soft start.** SS functions as a soft start and also sets the operating frequency together with FSET. Connect a capacitor from SS to GND to set the soft-start time. An internal 10μA sourcing current charges this capacitor to 2.4V at soft start. Connect a resistor between SS and FSET to set the operating frequency together with the resistor from FSET to GND.
7	VOCP	**Over-current protection of the system bus voltage stage.** VOCP senses the secondary current of the system bus voltage stage. When VOCP is lower than -203mV, the IC triggers a bus stage protection. VOCP is also used for the inner current control loop for the bus voltage compensation to control the extra MOSFET duty cycle.
8	FSET	**Frequency set.** Connect a resistor from FSET to GND, and another resistor between FSET and SS. The operating frequency is determined by the sourcing current through FSET. The voltage of FSET and the operating frequency are programmed by the current control loop and the voltage control loop.
9	VCOMP	**Feedback compensation node of the voltage control loop.** Connect a compensation capacitor or an R-C network from VCOMP to GND. The VCOMP voltage is internally clamped between 1.02V and 2.28V, which limits the operating frequency range.
10	VFB	**Bus voltage feedback.** VFB feeds back the bus voltage for regulation. Its inner reference voltage is 1.2V. VFB is also used for over-voltage protection of the bus voltage stage. When VFB exceeds 1.5V, the over-voltage protection of the bus voltage stage is triggered. VFB also functions as the open feedback loop protection. If VFB is lower than 50% of its reference voltage and VCOMP or DCOMP is saturated for 512 cycles, the IC triggers the bus voltage stage protection.
11	DCOMP	**Feedback compensation node of the voltage control loop**. DCOMP is used to program the duty cycle of the extra N-channel MOSFET. Connect a compensation capacitor or an R-C network from DCOMP to GND.
12	IFB	**LED current feedback input.** IFB feeds back the LED current through a sensing resistor. The internal error amplifier sinks a current from ICOMP proportional to the absolute value of the voltage at IFB. The average voltage at IFB is regulated to the reference voltage (controlled by the ADIM voltage, 199mV when ADIM is high). The voltage on IFB is also used for LED over-current detection. When the voltage on IFB rises higher than 415mV for 340μs or when the voltage rises higher than 555mV, the IC triggers the LED stage protection. IFB also functions as the LED current open feedback loop protection. If the IFB voltage is lower than 50% of its reference voltage and the ICOMP is saturated for 1024 cycles, the IC triggers the LED stage protection.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
13	ICOMP	**Feedback compensation node of the current control loop.** Connect a compensation capacitor or an R-C network from ICOMP to GND. The ICOMP voltage is internally clamped between 1.02V and 2.28V, which limits the operating frequency range. ICOMP also functions as the short LED to GND protection. When ICOMP is saturated and the IFB voltage is lower than 50% of the reference current for 1024 cycles, IC uses it as the fault condition and triggers an LED fault protection.
14	IOCP/FAULT	**LED stage over-current protection and fault indicator.** IOCP/FAULT feeds back the secondary side current of the LED driver stage. When the voltage on IOCP/FAULT is less than -320mV for 7μs, the IC disables the output of the DIMO signal. After 270μs, the IC outputs the fault indicator. If the IOCP voltage is always lower than -320mV for 270μs, the IC latches up the LLC.
15	VLED1	**Voltage feedback of LED string 1.** VLED1 and VLED2 cooperate for the protection of the LED driver stage. The maximum voltage and the voltage difference among VLED1 and VLED2 are detected and used for LED stage protection. For 1-string applications, connect VLED1 and VLED2; for two-string applications, feed back the LED strings voltages to VLED1 and VLED2; for applications with more than two strings, feed back the maximum voltage of the LED strings and the minimum voltage of the LED strings to VLED1 and VLED2.
16	VLED2	**Voltage feedback of LED string 2.**
17	EN_LED	**The enable signal for the LED driver.** Logic high enables the LED stage; logic low disables the LED stage.
18	ADIMP	**The pulse input signal for analog dimming.** The duty cycle 0 to 100% of this pulse signal programs the amplitude of the LED current from 0 to 100%. Place a 100nF capacitor from ADIM to GND for this type of dimming. If this dimming is not being used, pull it high to VCC through a 100k resistor or leave it open.
19	ADIM	**Analog dimming input with DC voltage.** The LED current is set by 0~2.4V from 0 to 100%. ADIMP should be disabled if using this DC input analog dimming. If this dimming is not being used, pull it high to VCC through a 100kΩ resistor.
20	PWMIN	**PWM dimming control input.** Apply a 100Hz to 2kHz PWM signal to PWMIN for PWM dimming.
21	VIN	**Supply input.** Bypass VIN with a ceramic capacitor larger than 0.1μF.
22	PS_ON	**On/off signal for the system power supply**. PS_ON is the enable signal for the IC. This signal determines the operation mode of the IC. If PS_ON is less than 0.8V, the IC works in standby mode. IC operates in deep burst mode, and the system bus voltage is controlled with a larger ripple voltage to decrease the power consumption. If PS_ON is greater than 0.8V but less than 2V and this saturation lasts for 1ms, the IC shuts down. If PS_ON is greater than 2V, the IC works in normal operation mode.
23	VCC	**Power supply for the gate driver of the LLC MOSFETs and internal circuit.** Bypass VCC to GND with a ceramic capacitor larger than 1μF.
24	DIMO	**Output of the driving signal for the dimming MOSFET.**
25	GL	**LLC driving signal output.** 180 degree phase shift of GR.
26	GND	**Ground reference.**
27	GR	**LLC driving signal output.** 180 degree phase shift of GL.
28	CFLY	**Output of the pulse signal for the charge pump.** Connect a flying cap higher than 100nF of the charge pump to CFLY. Please refer to the typical application circuit for connection details.

BLOCK DIAGRAM

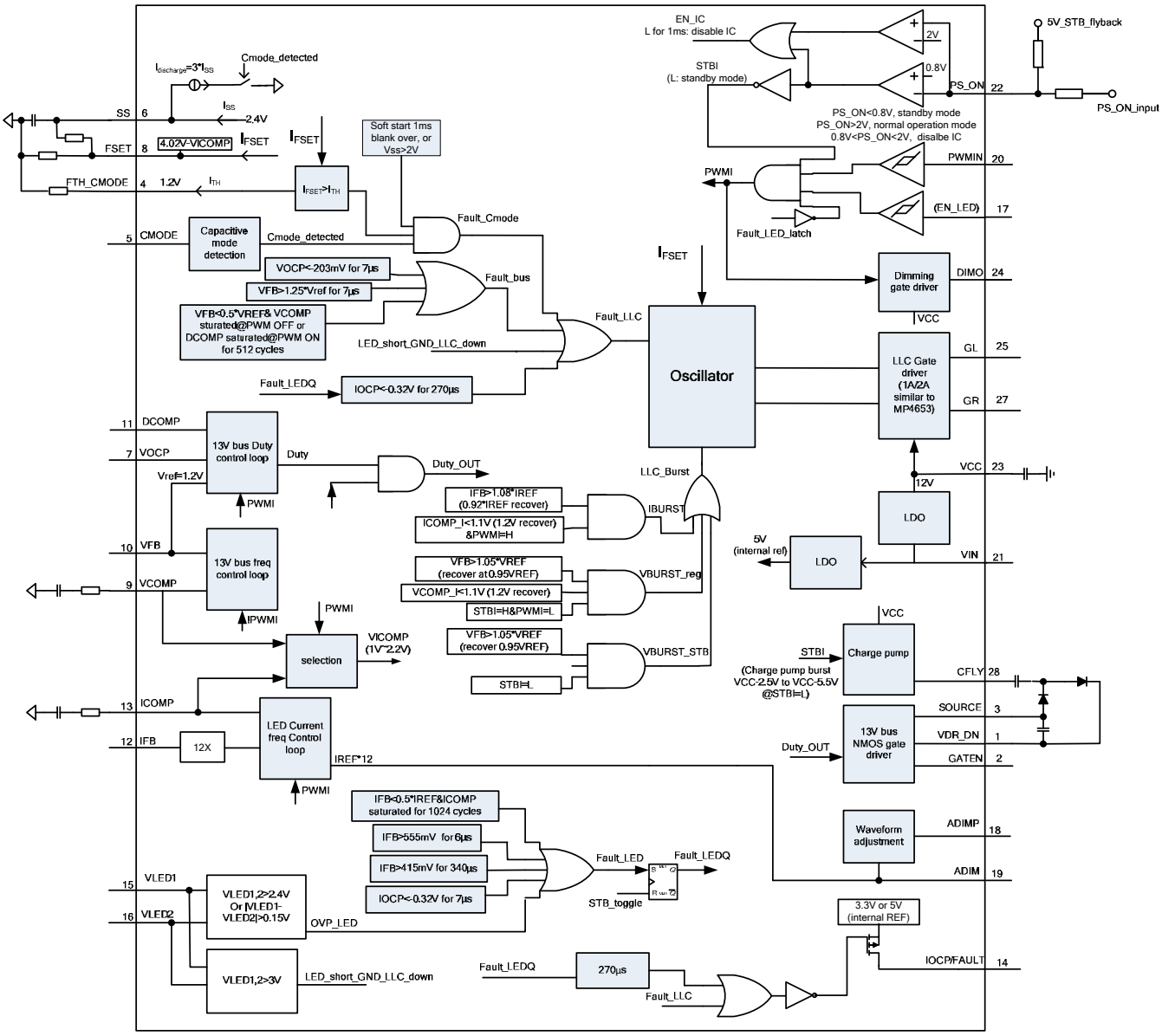


Figure 1: Functional Block Diagram

OPERATION

The MP4655 is a pure, single-stage, LLC, LED current and system voltage controller for LED backlighting located on the secondary side. The MP4655 uses the LLC power stage and an extra N-channel MOSFET to regulate both the LED current and the system supply voltage. The MP4655 is powered by 9V to 35V input supplies that output two 180 degree phase shifted driving signals for the external LLC power stages. Its enhanced 12V gate driver provides adequate driving capability and can directly drive the external LLC MOSFETs through an external gate driving transformer. The MP4655 also provides a direct driving signal to control the extra N-channel MOSFET and regulates the system supply voltage.

The MP4655 uses frequency control on the LLC power stage to regulate the LED current at the PWM dimming on interval and the system bus voltage at the PWM dimming off interval. The duty cycle of the extra N-channel MOSFET regulates the system bus voltage at the PWM on interval. Both the LED current and the system bus voltage are regulated accurately.

Internal Regulator

The MP4655 includes an internal linear regulator (VCC). VCC is the supply voltage for the LLC gate driver, the charge pump, and the internal circuit. The MP4655 features under-voltage lockout for both the VCC regulator and the inner circuit. Until VIN exceeds its UVLO threshold, the VCC regulator does not work. The chip is disabled until VCC exceeds its UVLO threshold.

The internal VCC regulator is also controlled by the IC enable signal (PS_ON).

Charge Pump and Extra N-Channel MOSFET Driver

The MP4655 integrates a charge pump that drives the extra N-channel MOSFET directly (see Figure 2). The charge pump is powered by VCC and outputs a high-frequency square wave signal. Together with an external C-diode network, the charge pump forms a floating driver supply voltage on VDR_DN referred to the SOURCE voltage with an amplitude close to VCC. This floating driver supply voltage can directly drive the extra N-channel MOSFET.

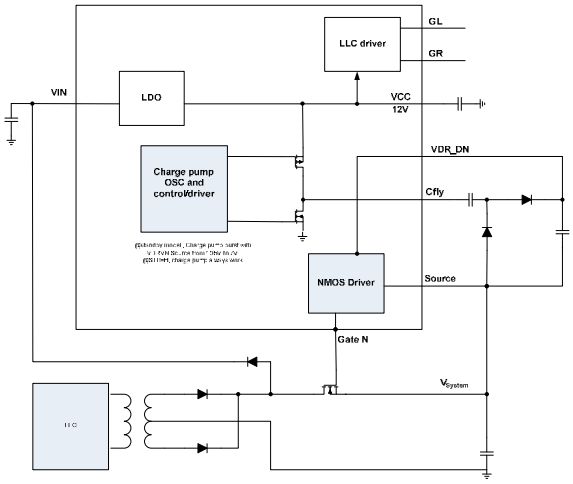


Figure 2: Charge Pump for Extra N-Channel MOSFET Driver

Operation Modes and System Start-Up

The MP4655 is controlled by its enable signal (PS_ON) and uses the following operating modes:

1. PS_ON > 2V: the IC is enabled in normal operation mode.
2. 0.8V < PS_ON ≤ 2V for 1ms: the IC is disabled and no circuits work.
3. PS_ON ≤ 0.8V: the IC is enabled in standby mode.

It is very easy to set up the system connection, whether the MP4655 is required to do so in standby or not.

When the MP4655 is enabled and the VIN supply is higher than its UVLO threshold, VCC is charged up. When VCC passes its UVLO threshold, the IC starts up. The voltage resets the control loop for LLC frequency control, voltage control loop for the extra N-channel MOSFET duty cycle control, and the soft-start capacitor.

EN_LED and PWMIN control the start-up of the LED driver stage. If either EN_LED or PWMIN are low, the LED driver stage is disabled and DIMO is pulled low. The system operates in constant voltage mode, and V_{System} is regulated through the LLC frequency control. The extra N-channel MOSFET is on in this condition. If either EN_LED or PWMIN are high, the LED driver

stage is enabled and DIMO rises high. The LED current is regulated through the LLC frequency control, and the V_{System} is regulated through the duty cycle control of the extra N-channel MOSFET.

Standby Mode with Low Consumption Power and No Audible Noise

The MP4655 features a standby mode with low consumption power on the LLC power stage. When PS_ON ≤ 0.8V, the MP4655 enters standby mode, regardless of the status of the LED driver stage control signals.

In standby mode, the LED stage is disabled, V_{System} is controlled through the LLC frequency control, and the extra N-channel MOSFET is on. The MP4655 takes the following actions to decrease the system power consumption:

1. V_{System} is controlled within ± 5% and the circuit works in soft-burst mode. The VFSET voltage is clamped at 2.1V, so the switching frequency at burst mode is not too high. Power consumption is decreased in this mode. A soft burst-on time and soft burst-off time are added to the burst mode to eliminate audible noise (see Figure 3).
2. The charge pump for VDR_DN works in burst mode, and VDR_DN is controlled with a larger ripple voltage. This decreases the IC consumption current.
3. The internal logic circuit consumption current is decreased.

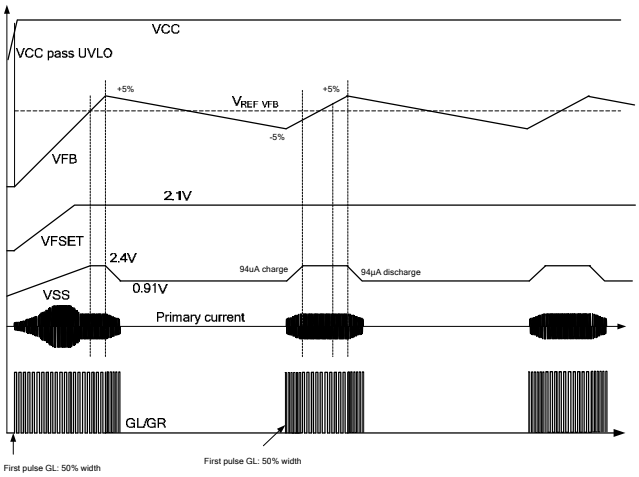


Figure 3: LLC Soft-Burst Operation at Standby Mode

LED Current and System Voltage Regulation

The MP4655 accurately regulates both the LED current and the output system voltage with only one LLC power stage.

In PWM dimming off condition, the LED stage is not enabled (PWMIN is low, EN_LED is not enabled, or LED stage fault detected). The MP4655 regulates the output system voltage through the LLC frequency control, and the extra N-channel MOSFET is on (see Figure 4A).

In PWM dimming on condition, the MP4655 regulates the LED current through the LLC frequency control, and regulates the output system voltage through the duty cycle control of the extra N-channel MOSFET. The integrated individual control for this extra N-channel MOSFET achieves soft switching, and there is no voltage spike (see Figure 4B).

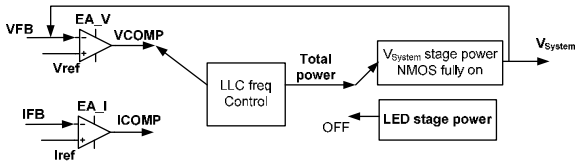


Figure 4A: MP4655 Control Scheme at PWM Dimming Off

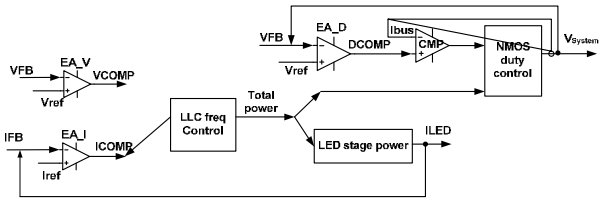


Figure 4B: MP4655 Control Scheme at PWM Dimming On

The regulation for the LED current and system voltage at different conditions is as follows:

1. LED current regulation at PWM dimming on (ICOMP loop)

For the LED current regulation loop with LLC frequency control, the LED current is fed back to IFB. The internal error amplifier regulates the average value of IFB signal to the internal 199mV reference voltage. Its output is connected to the external current-loop compensation network on ICOMP through an inner switch (S1).

During the PWM on interval, S1 is on, and the output of the error amplifier is connected to the external compensation network on ICOMP. The

LED current is regulated by this control loop and the LLC operating frequency is programmed by the ICOMP voltage.

During the PWM off interval, S1 is turned off, and the compensation network on ICOMP is disconnected from the error amplifier and holds its value until the next PWM on interval.

The MP4655 integrates burst mode for the LED current regulation. When the IFB voltage is higher than 1.08 times its reference voltage and the ICOMP voltage is low enough (which means it is at its highest operating frequency), the IC skips some switching cycles until the IFB voltage decreases sufficiently.

2. Output system voltage regulation at PWM dimming off (VCOMP loop)

For the system voltage regulation loop, the output system voltage is fed back to VFB. During the PWM off interval, the MP4655 regulates the system voltage through the LLC frequency control, and the extra N-channel MOSFET is on. The internal voltage-loop error amplifier regulates the average value of the VFB voltage to the reference voltage (VREF). Its output is connected to the external voltage-loop compensation network on VCOMP through an inner switch S2. During the PWM off interval, S2 is on, and the output of the voltage-loop error amplifier is connected to the external compensation network on VCOMP. The output system voltage is regulated by this control loop and the LLC operating frequency is programmed by VCOMP.

During the PWM on interval, S2 is turned off, and the compensation network on VCOMP is disconnected from the error amplifier and holds its value until the next PWM off interval.

The MP4655 also integrates burst mode for voltage regulation with the LLC frequency control through the VCOMP loop. When VFB is higher than 1.05 times the reference voltage and VCOMP is sufficiently low (which means a high LLC operating frequency), the IC skips some switching cycles until VFB voltage decreases sufficiently.

The LLC operating frequency is controlled by the output of the current loop error amplifier on ICOMP at PWM dimming on and is controlled by the voltage loop error amplifier on VCOMP at PWM dimming off. A higher compensation output voltage results in a lower operating frequency.

3. Output system voltage regulation at PWM dimming on (DCOMP loop)

During the PWM on interval, the LLC frequency control regulates the LED current, and the output system voltage is regulated through the duty cycle of the extra N-channel MOSFET. The output system voltage is fed back on VFB, and the internal error amplifier regulates its average value to its reference voltage (VREF). The output of this error amplifier is connected to DCOMP through an inner switch (S3). S3 is on during the PWM on interval, and the output of this error amplifier is connected to the DCOMP compensation network. Together with slope compensation, the DCOMP voltage is compared with the current through the output system voltage stage, which is fed back to VOCP and determines the duty cycle of the extra N-channel MOSFET. The duty cycle of this extra N-channel MOSFET can achieve a 0 to 100% range. The MP4655 integrates individual controls on the extra N-channel MOSFET and achieves soft switching with no voltage spike.

During the PWM off interval, S3 is disconnected and DCOMP holds its voltage until the next PWM on interval. The extra N-channel MOSFET is forced on during the PWM off interval.

Both the LED current and output system voltage are accurately regulated at PWM dimming on and PWM dimming off. ICOMP, VCOMP, or DCOMP holds its voltage when its loop is not effective. This achieves a fast transition between different compensation loops at PWM dimming. Together with the external dimming MOSFET, which holds the LED output voltage during the PWM off interval, both the LED current and output system voltage are regulated accurately and smoothly at PWM dimming. No voltage ripple or LED current overshoot or undershoot is caused by PWM dimming.

Dimming Control

The MP4655 provides two dimming methods: PWM dimming mode and analog dimming mode. Applying a digital PWM signal on PWMIN allows for PWM dimming. The brightness of the LED string is proportional to the duty cycle of the external PWM signal. A driving signal on DIMO is

output to drive the dimming MOSFET directly, which helps achieve fast and high-contrast ratio PWM dimming.

The MP4655 achieves a 1000:1 PWM dimming ratio at 200Hz PWM dimming frequency (0.1% minimum PWM dimming duty). The PWM dimming ratio may decrease with a higher PWM dimming frequency.

For analog dimming mode, a DC voltage on ADIM or a pulse signal on ADIMP can be used. For DC input analog dimming, apply a DC analog signal from 0V to 2.4V on ADIM to dim the LED current amplitude from 0 to 100%. ADIMP can be left open or pulled high to VCC through a 100kΩ resistor in this mode.

For analog dimming with a pulse input signal, apply the pulse signal on ADIMP and a 100nF capacitor on ADIM, depending on the frequency of this pulse signal. The duty cycle of this pulse signal from 0 to 100% dims the LED current from 0 to 100%.

The PWM dimming and analog dimming could be applied to the IC simultaneously for an extra dimming ratio.

Protection Features

The MP4655 integrates sufficient protection for the LLC power stage, the output system voltage stage, and the LED driver stage.

Capacitive Mode Protection for the LLC Power Stage

The MP4655 integrates individual capacitive mode protection for the LLC power stage by detecting the secondary side signal. Feed back the secondary side winding voltage to CMODE for capacitive mode protection. When capacitive mode is detected, the MP4655 discharges the SS voltage and increases the LLC operating frequency. If the capacitive mode is still detected when the operating frequency is higher than the threshold frequency setting by FTH_CMODE, the IC latches up and outputs a high fault indicator.

System Voltage Stage Protection

The protections for the system voltage stage include over-system voltage protection, short protection, and open-feedback loop protection.

1. Over-system voltage protection

VFB senses the output system voltage for regulation and over-voltage protection. If the VFB voltage is higher than $1.25V_{REF}$, the MP4655 triggers the over-system voltage protection and latches up. The fault indicator output is high.

2. System voltage stage short protection

VOCP senses the current through the output system voltage stage for short protection of the system voltage stage. If the voltage on VOCP is lower than -203mV for 7μs, the MP4655 latches up and outputs a high fault indicator.

3. System voltage stage open-feedback protection

During the PWM dimming off interval, if the VFB voltage is lower than 50% of its reference and VCOMP is saturated for 512 switching cycles, the IC latches up and outputs a high fault indicator.

During the PWM dimming on interval, if the VFB voltage is lower than 50% of its reference voltage and DCOMP is high for 512 cycles, the IC latches up and outputs a high fault indicator.

LED Driver Stage Protection

The fault protection for the LED driver stage includes the open LED protection, short LED protection, over-LED current protection, open feedback loop protection, and protection for any point of the LED string shorting to ground.

The voltage of the LED strings is sensed on VLED1 and VLED2. Both the maximum value and the difference in voltages of VLED1 and VLED2 are used for protection. When the maximum value of VLED1 and VLED2 rises higher than 2.41V or the difference in the voltages rises higher than 150mV for 8μs, the IC triggers over-LED voltage protection (the voltage difference can be adjusted by the external input resistance on VLED1 or VLED2).

DIMO is pulled low, and the output system voltage is regulated by the LLC frequency control, the same as in PWM off condition, and the fault indicator output is high. If the maximum value of VLED1 and VLED2 rises higher than 3V for 7.6μs, the MP4655 latches up and disables the LLC power stage to avoid any damage to the LED driver stage. The fault indicator output is high.

The secondary side current of the LED driver stage is sensed on IOCP/FAULT. When the

IOCP voltage is lower than -320mV for 7μs, the MP4655 triggers the LED driver stage protection. At the LED driver stage protection, the DIMO is pulled low, and the output system voltage is regulated by the LLC frequency control, the same as in PWM off condition. The fault indicator output is high after 270μs. After the LED driver stage protection is triggered, IOCP/FAULT continues detecting the LED driver stage current. If the voltage on IOCP/FAULT remains lower than -320mV for 270μs, the MP4655 latches up and disables the LLC power stage.

The LED current feedback (IFB) is used for over-LED current protection. When IFB voltage rises higher than 415mV for 340μs or the IFB voltage rises higher than 555mV for 6μs, the IC triggers the LED driver stage protection.

If the voltage on IFB is lower than 50% of its reference voltage, and the ICOMP is saturated for 1024 cycles, the IC considers this to be a short LED to GND protection or open feedback protection and triggers the LED driver stage protection. The reference voltage varies according to the analog dimming signal.

In a fault condition of the LED driver stage, the gate driving signals for the LLC power MOSFETs are still active and the output system voltage is regulated, only if the LED driver stage can be disconnected from the power stage. Therefore, the system power supply is not influenced by the fault protection of the LED driver stage. A MOSFET can be used to disconnect the LED driver stage at the LED fault condition (see Figure 11).

Thermal protection is also integrated in the MP4655.

APPLICATION INFORMATION

Frequency Set and Soft Start (SS, FSET)

The resistor on FSET and the resistor between FSET and SS determine the operating frequency, which can be calculated with Equation (1):

$$f = (\frac{V_{FSET}}{R_{FSET}} - \frac{Vss - V_{FSET}}{R_{SS\_FSET}}) * 11.4 * 10^9 (Hz) \quad (1)$$

Where V_{FSET} = 4.01V - V_C. V_C is the VCOMP voltage at PWM dimming off and ICOMP voltage at PWM dimming on. The V_C range is clamped from 1.02V to 2.28V. V_{SS} is the voltage on SS, typically 2.4V.

The minimum operating frequency can be calculated with Equation (2):

$$f_{min} = (\frac{1.73V}{R_{FSET}} - \frac{0.675V}{R_{SS\_FSET}}) * 11.4 * 10^9 (Hz) \quad (2)$$

The maximum operating frequency at steady state can be calculated with Equation (3):

$$f_{max} = (\frac{2.99V}{R_{FSET}} + \frac{0.585V}{R_{SS\_FSET}}) * 11.4 * 10^9 (Hz) \quad (3)$$

When V_{SS} is 0V, the soft start-up frequency is calculated with Equation (4):

$$f_{start} = (\frac{2.99V}{R_{FSET}} + \frac{2.99V}{R_{SS\_FSET}}) * 11.4 * 10^9 (Hz) \quad (4)$$

The operating frequency at standby mode is calculated with V_{FSET} = 2.1V. See Equation (5):

$$f_{STB} = (\frac{2.1V}{R_{FSET}} - \frac{0.305V}{R_{SS\_FSET}}) * 11.4 * 10^9 (Hz) \quad (5)$$

It is recommended to set the operating frequency in standby mode close to the LLC resonant frequency (f_0) for optimum efficiency.

The soft start-up time is determined by the capacitor on SS and can be calculated with Equation (6):

$$T_{SS} = \frac{2.405V * C_{SS}}{13uA} \quad (6)$$

A 10nF capacitor on SS results in a 1.85ms soft-start time.

LED Current Set (IFB)

The LED current is set by the current sense resistor on the cathode of LED and can be calculated with Equation (7):

$$I_{LED} = \frac{V_{IREF}}{Rsense} = \frac{199mV}{Rsense} \quad (7)$$

A 2kΩ resistor is recommended between the LED current sense resistor and IFB, considering the possible spike voltage on the current sense resistor when shorting the LED string.

System Output Voltage Set (VFB)

VFB feeds back the system output voltage. Adjust the voltage divider to set the output system voltage. See Equation (8):

$$V_{system} = \frac{V_{REF\_VFB} * (R_{VFBH} + R_{VFBL})}{R_{VFBL}} = \frac{1.2V * (R_{VFBH} + R_{VFBL})}{R_{VFBL}} \quad (8)$$

A capacitor (C_{VFBH}) between the system output and VFB provides a better phase margin for the system output voltage control loop (see Figure 5).

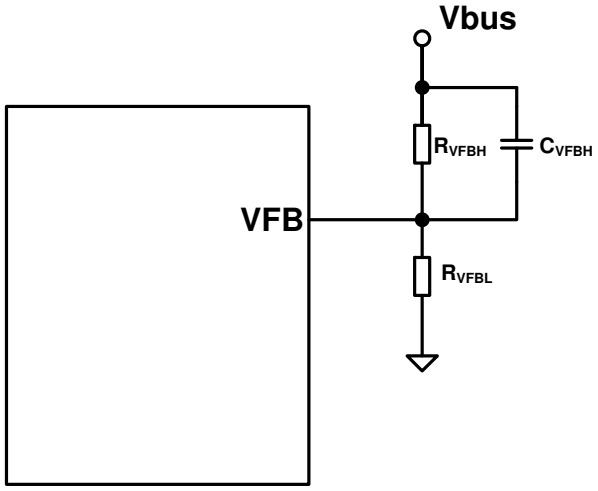


Figure 5: Voltage Feedback Network

The zero composed by R_{VFBH} and C_{VFBH} is recommended to be in range of one-fifth to one-third of the operating frequency. See Equation (9):

$$\frac{1}{2\pi * R_{VFBH} * C_{VFBH}} = (\frac{1}{5} \text{ to } \frac{1}{3}) f_{op} \quad (9)$$

The VFB also functions as the protection for the over system output voltage. When VFB is 25% higher than its reference voltage, the IC triggers system output voltage stage protection.

LED Current Compensation Loop (ICOMP)

ICOMP is the compensation node for the LED current control loop. Connect a capacitor in series with a resistor on ICOMP or an R-C-C network (see Figure 6). The zero composed of R_{ICOMP} and C_{ICOMP} is recommended to cancel the pole formed by the LED output. See Equation (10):

$$\frac{1}{R_{ICOMP} * C_{ICOMP}} = \frac{1}{R_{eq\_LED} * C_{OUT\_LED}} = \frac{1}{\frac{(10\% \text{ to } 20\%) * V_{LED}}{I_{LED}} * C_{OUT\_LED}} \quad (10)$$

C_{ICOMP} is in range of 10nF to 470nF, typically. Select C_{ICOMP_P} to be less than one-twentieth of C_{ICOMP}.

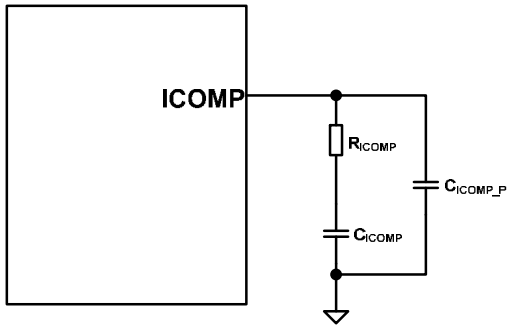


Figure 6: Compensation Network on ICOMP

System Output Voltage Compensation Loop through LLC Control (VCOMP)

VCOMP is the compensation node for the system output voltage control loop through the LLC frequency. Connect a capacitor in series with a resistor on VCOMP or an R-C-C network (see Figure 7). The zero composed of the R_{ICOMP} and C_{ICOMP} is recommended to cancel the pole formed by the system output. See Equation (11):

$$\frac{1}{R_{VCOMP} * C_{VCOMP}} = \frac{1}{R_{Vbus} * C_{OUT\_Vbus}} = \frac{1}{\frac{V_{bus}}{I_{out\_full}} * C_{OUT\_Vbus}} \quad (11)$$

Where C_{VCOMP} is in the range of 10nF to 470nF, typically.

The pole formed by R_{VCOMP} and C_{VCOMP_P} can be designed to be around half of the operating frequency. See Equation (12):

$$\frac{1}{2\pi * R_{VCOMP} * C_{VCOMP\_P}} = \frac{f_{op}}{2} \quad (12)$$

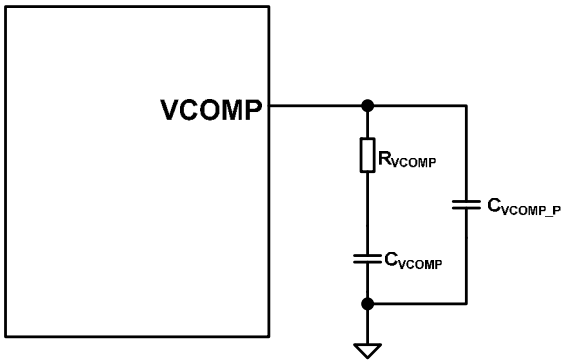


Figure 7: Compensation Network on VCOMP

System Output Voltage Compensation Loop through Duty-Controlled NMOS (DCOMP)

DCOMP is the compensation node for the system output voltage control loop through the duty-controlled NMOS. Connect a capacitor in series with a resistor on DCOMP or an R-C-C network (see Figure 8).

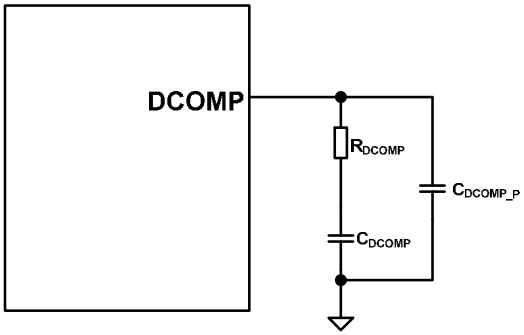


Figure 8: Compensation Network on DCOMP

The zero composed of R_{DCOMP} and C_{DCOMP} is recommended to cancel the pole formed by the system output. See Equation (13):

$$\frac{1}{R_{DCOMP} * C_{DCOMP}} = \frac{1}{R_{Vbus} * C_{OUT\_Vbus}} = \frac{1}{\frac{V_{bus}}{I_{out\_full}} * C_{OUT\_Vbus}} \quad (13)$$

Where C_{VCOMP} is in the range of 4.7nF to 100nF, typically.

The pole formed by R_{DCOMP} and C_{DCOMP_P} can be designed to be around half of the operating frequency. See Equation (14):

$$\frac{1}{2\pi * R_{DCOMP} * C_{DCOMP\_P}} = \frac{f_{op}}{2} \quad (14)$$

Over-Current Protection for the System Output Stage (VOCP)

VOCP implements an over-current protection for the system output voltage stage. The current of the system output voltage stage is sensed on VOCP with a negative polarity. When the voltage on VOCP is lower than -203mV, the IC triggers the system output voltage stage protection. Calculate the over-bus current protection threshold with Equation (15):

$$I_{OCP\_Bus} = \frac{203mV}{R_{VOCP}} \quad (15)$$

Typically, the protection point is around 1.5 to 3 times the normal current of the system output voltage stage.

Over-Current Protection for the LED Driver Stage (IOCP/FAULT)

IOCP detects the current through the LED stage with a negative polarity. When the voltage on IOCP falls below -320mV, the IC triggers LED driver stage protection. Calculate the over-LED current protection threshold with Equation (16):

$$I_{OCP\_LED} = \frac{320mV}{R_{IOCP}} \quad (16)$$

The over-current protection point for the LED stage can be set at around 1.5 to 2 times the total current through the LED strings.

ICOP also functions as the fault indicator for the system. When either LED driver stage protection, system bus voltage protection, or capacitive mode protection are triggered, the fault signal output is high. Place a 10kΩ resistor between IOCP and the LED stage current sense point.

Over-LED Voltage Protection and LED Voltage Difference Protection (VLED1, VLED2)

VLED1 and VLED2 sense the LED voltages and function as the over-LED voltage protection. The voltage divider sets the over-voltage protection point with Equation (17):

$$V_{OVP} = \frac{R_{OVPH} + R_{OVPL}}{R_{OVPL}} \times 2.41V \quad (17)$$

Normally, the OVP point is set about 10% - 30% higher than the maximum LED voltage.

The MP4655 also implements protection when the LED string voltages are different from each other to protect the condition in which several LEDs in a string are shorted. This protection is used only for multiple-string applications. The protection point of the voltage difference between the LED strings is set with Equation (18):

$$\Delta V_{pro} = \frac{R_{OVPH} + R_{OVPL}}{R_{OVPL}} \times 2.41V \times \frac{20k + R_{input}}{16 \times 20k} \quad (18)$$

Where R_{input} is the input resistance of VLED1 or VLED2). Adjust the input resistance to program the protection point.

A resistor (R_X) can be added between the voltage divider and VLED1 or VLED2 to adjust the input resistance. See Equation (19):

$$R_{input} = \frac{R_{OVPH} \times R_{OVPL}}{R_{OVPL} + R_{OVPH}} + R_X \quad (19)$$

Capacitive Mode Protection (CMODE, FTH_CMODE)

The MP4655 implements individual capacitive mode protection for the LLC power stage from the secondary side. CMODE monitors the secondary side winding voltage and functions as the capacitive mode protection. The winding voltage polarity is positive (high) when GL is on.

When capacitive mode is detected, the IC decreases the SS voltage and increases the operating frequency to attempt to move the power stage to inductive mode. FTH_CMODE sets the threshold frequency to trigger capacitive mode protection. If the operating frequency is higher than that set by FTH_CMODE and capacitive mode is still detected, the IC triggers capacitive mode protection. Connect a resistor on FTH_CMODE to set the threshold frequency. See Equation (20):

$$f_{th\_Cmode} = (\frac{1.2V}{R_{Fth\_Cmode}}) * 11.4 * 10^9 (Hz) \quad (20)$$

PWM Dimming Input (PWM)

PWM is for the PWM dimming input. Apply a PWM dimming signal with a frequency between 100Hz to 2kHz on PWM. The PWM dimming has positive polarity.

PWM Dimming Signal Output (DIMO)

DIMO outputs a PWM dimming signal to drive the external dimming N-channel MOSFET in series with the LED string and achieves fast PWM dimming. Connect a resistor in series with DIMO to adjust the driving speed.

Analog Dimming (ADIM, ADIMP)

The MP4655 implements either DC analog dimming or pulse analog dimming for the LED current (see Table 1).

For DC input analog dimming, apply a 0V to 2.4V DC voltage on ADIM to program the LED current from 0 to 100%. ADIMP is left open or pulled high above 5V.

For pulse input analog dimming, apply the pulse analog dimming signal on ADIMP and a capacitor on ADIM. A duty cycle on the pulse analog dimming signal from 0 to 100% dims the LED current from 0 to 100%. A lower frequency of the pulse analog dimming signal requires a larger capacitor on ADIM. For a 10kHz pulse signal, a capacitor 100nF or above on ADIM is recommended.

If analog dimming is not required, pull ADIM high and leave ADIMP open. Analog dimming and PWM dimming can be applied together.

Table 1: MP4655 Dimming Connections

Items	ADIM	ADIMP	PWM
Only DC input analog dimming	DC analog dimming signal 0 to 2.4V	Float or pulled high above 5V	Pull high
Only pulse input analog dimming	Capacitor	Pulse analog dimming signal	Pull high
Only PWM dimming	Pull high	Float	PWM
PWM + DC input analog dimming	DC analog dimming signal 0-2.4V	Float or pull high above 5V	PWM
PWM + pulse analog dimming	Capacitor	Pulse analog dimming signal	PWM

Supply Input (VIN)

VIN is the supply input voltage of the IC. Bypass VIN with a ceramic capacitor 0.47μF or larger.

LLC Gate Driver (VCC, GL, GR)

VCC supplies the gate drive signals GL, GR, DIMO, and the charge pump from CFLY. Bypass VCC with a ceramic capacitor 1μF or larger. VCC can also be used to supply an external circuit. To avoid noise during layout, place the VCC capacitor directly between VCC and GND with a short and separate wire.

GL and GR provide the driving signal for the LLC power stage. GL and GR are 180 degree phase shifted gate drive signals. With their enhanced drive capability, GL and GR can directly drive the external LLC MOSFETs in the power stage through a gate driving transformer.

The gate driving transformer also isolates the primary power stage and the secondary control circuit. Place a 2.2nF Y-cap between the power stage ground and the reference ground for the control circuit to improve EMI performance. The primary inductance of the gate driving transformer influences its magnetic current, which is also supplied by the IC. The primary inductance should be larger than 1mH, and is recommended to be over 2mH.

Extra NMOS Gate Driver (CFLY, VDR_DN, GATEN, SOURCE)

GATEN and SOURCE are connected to the extra duty-controlled NMOS' gate and source. They provide a floating driving signal for the duty-controlled NMOS. A resistor on GATEN can adjust the driving speed.

CFLY and VDR_DN provide a charge pump supply for GATEN referred to SOURCE. Connect a flying capacitor 100nF or above on CFLY, and diodes on SOURCE and VDR_DN, as shown in the typical application circuit.

LED Driver Stage Enable Signal (EN_LED)

EN_LED is connected to the enable signal for the LED driver stage. Logic high enables the LED driver stage and logic low disables the LED driver stage. When the LED driver stage fault is triggered but the IC is not latched up, toggle the enable signal to restart the LED driver stage.

System Enable Signal (PS_ON)

PS_ON is connected to the enable signal or standby signal. The voltage level on PS_ON determines the operation of the IC as follows:

1. PS_ON > 2V: the IC is enabled in normal operation mode.
2. 0.8V < PS_ON ≤ 2V for 1ms: the IC is disabled and no circuits work.
3. PS_ON ≤ 0.8V: the IC is enabled in standby mode.

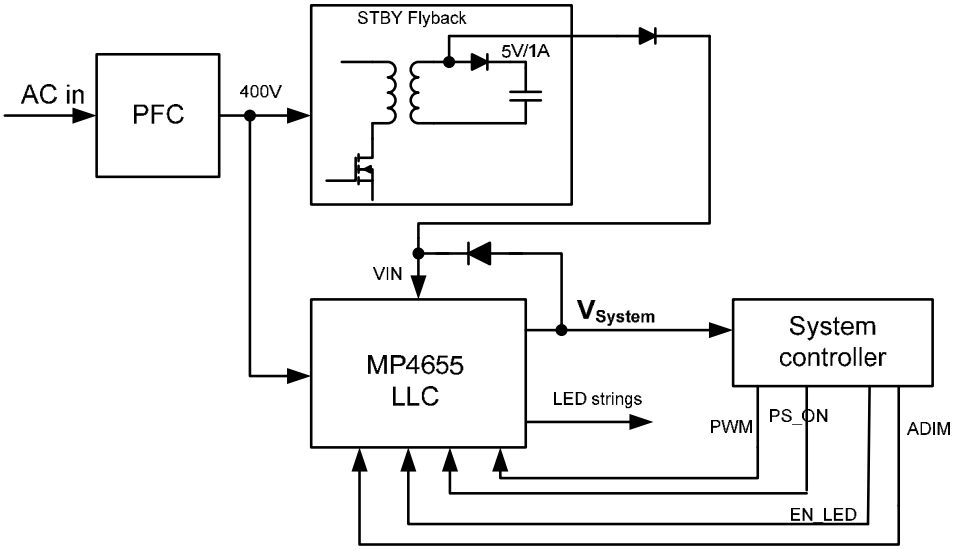


Figure 9: LLC Power System with External Standby Flyback

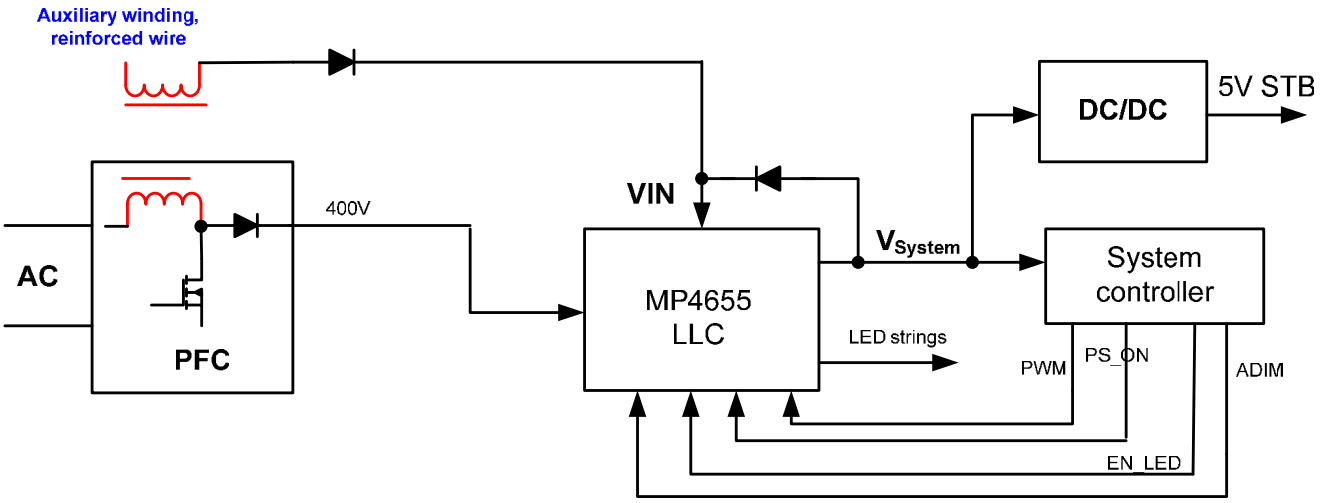


Figure 10: LLC Power System without External Standby Flyback

APPLICATION INFORMATION

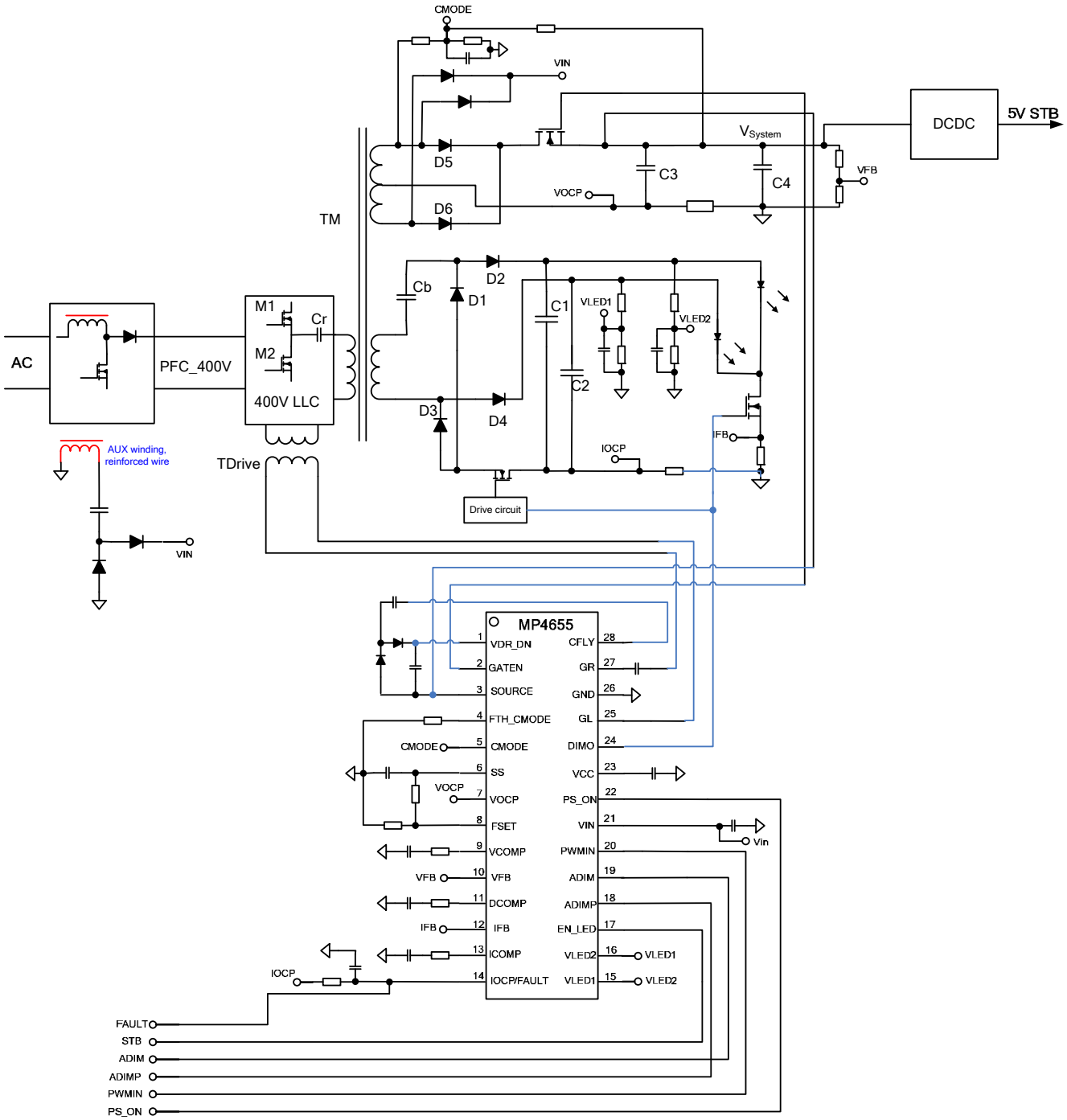


Figure 11: Application Circuit without Standby Flyback

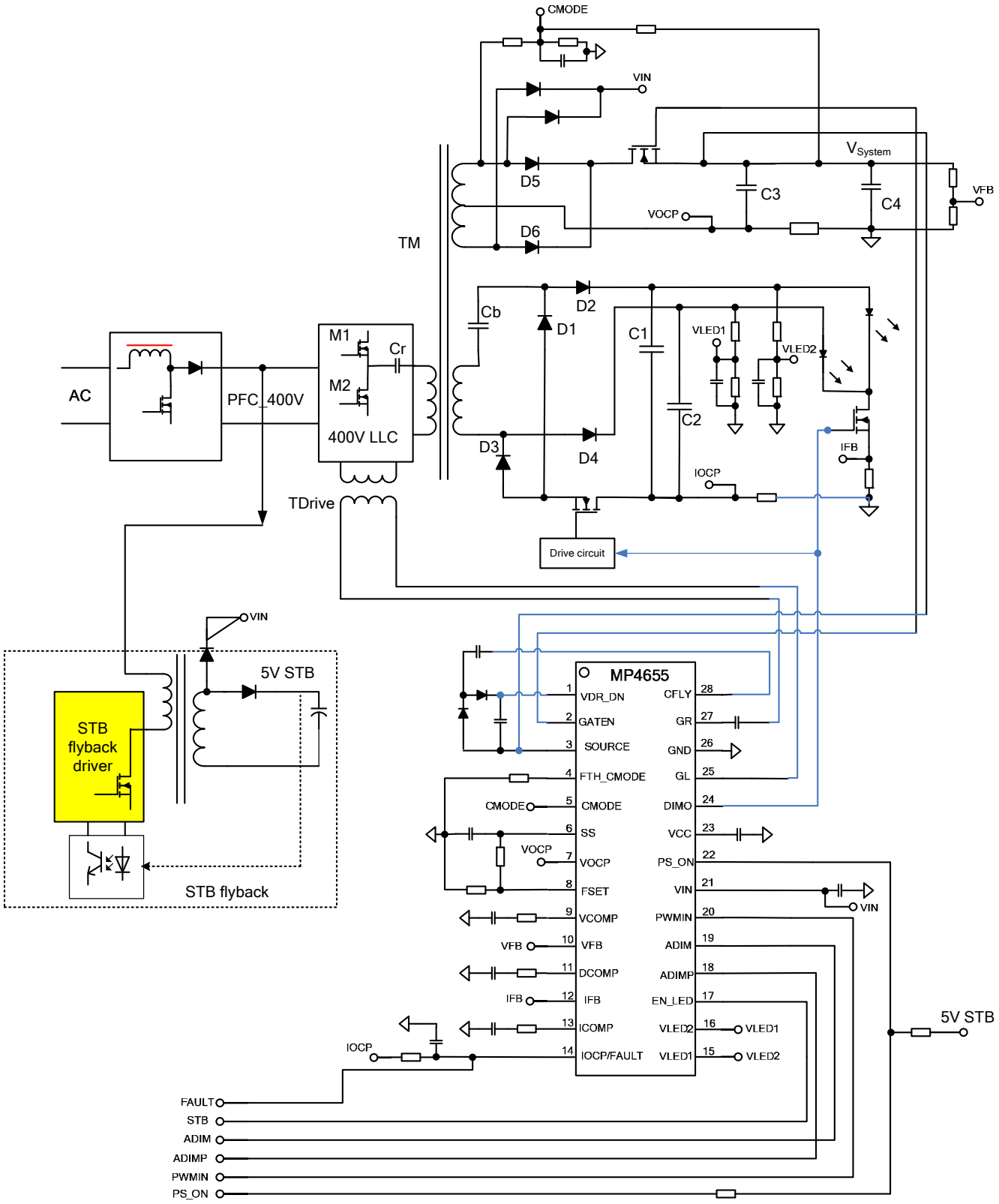


Figure 12: Application Circuit with Standby Flyback

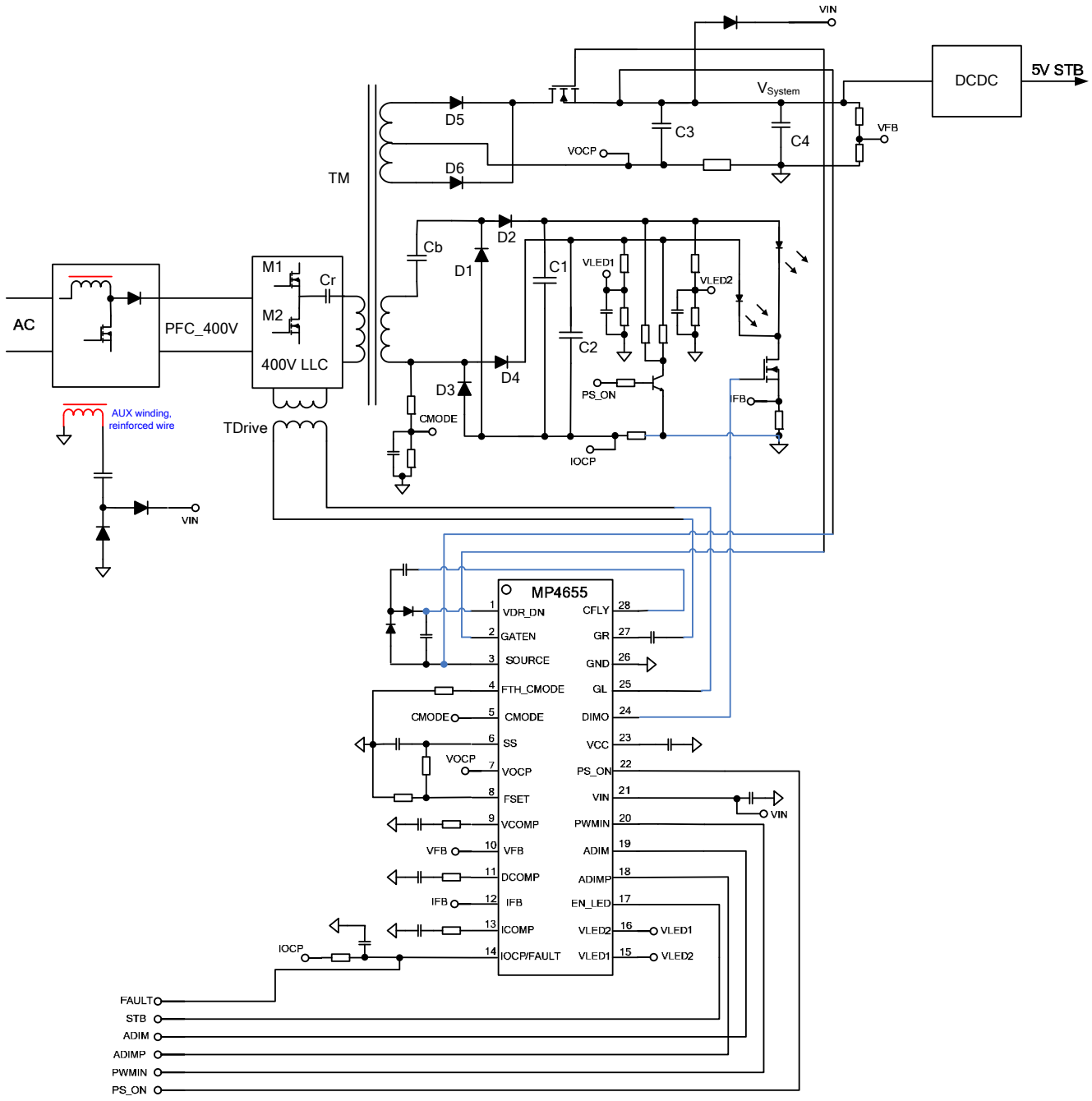
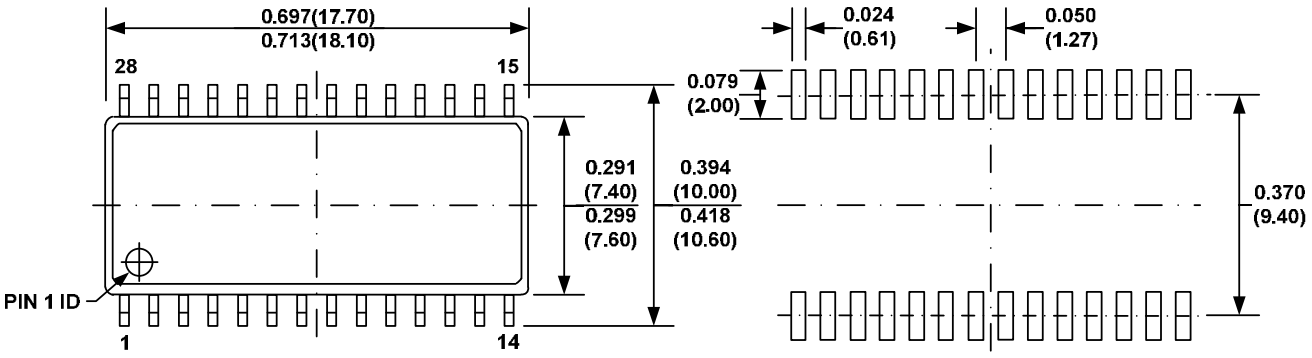


Figure 13: Application Circuit without Protection MOSFET on LED Stage

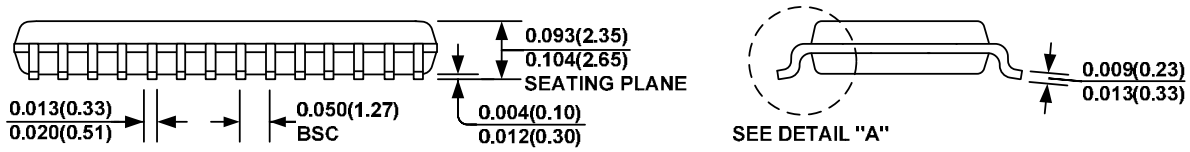
PACKAGE INFORMATION

SOIC-28



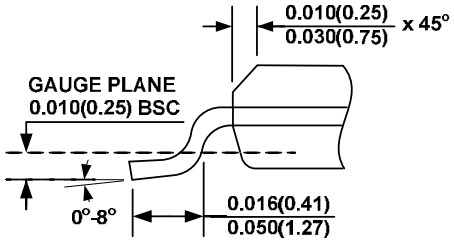
TOP VIEW

RECOMMENDED LAND PATTERN



FRONT VIEW

SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AE.
6) DRAWING IS NOT TO SCALE.