C2M0045170P

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology
N-Channel Enhancement Mode

Features

- 2nd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low On-Resistance
- High speed switching with low capacitances
- Resistant to latch-up
- Halogen Free, RoHS Compliant

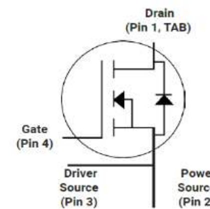
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Solar inverters
- Switch Mode Power Supplies
- High voltage DC/DC converters
- Motor drive
- Pulsed power applications

Package



Part Number	Package	Marking
C2M0045170P	TO-247-4L	C2M0045170P

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1700	V	V_{GS} = 0 V, I_D = 100 μA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values, AC (f >1 Hz)	Note: 1
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	Note: 2
I_D	Continuous Drain Current	75	A	V_{GS} =20 V, T_C = 25˚C	Fig. 19
		48		V_{GS} =20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	160	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	338	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-40 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063") from case for 10s	

Note (1): When using MOSFET Body Diode V_{GSmax} = -5V/+25V
Note (2): MOSFET can also safely operate at 0/+20V

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Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1700			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	3.0	4	V	V_{DS} = V_{GS}, I_D = 18mA	Fig. 11
			2.5		V	V_{DS} = V_{GS}, I_D = 18mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		2	100	μA	V_{DS} = 1700 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			600	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		40	70	mΩ	V_{GS} = 20 V, I_D = 50 A	Fig. 4,5,6
			80			V_{GS} = 20 V, I_D = 50 A, T_J = 150 °C	
g_{fs}	Transconductance		24.7		S	V_{DS}= 20 V, I_{DS}= 50 A	Fig. 7
			23.4			V_{DS}= 20 V, I_{DS}= 50 A, T_J = 150 °C	
C_{iss}	Input Capacitance		3455		pF	V_{GS} = 0 V V_{DS} = 1200 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		171				
C_{rss}	Reverse Transfer Capacitance		6.7				
E_{oss}	C_{oss} Stored Energy		139		μJ		Fig 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		188		pF	V_{GS} = 0 V, V_{DS} = 0... 1200V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		255		pF		
E_{ON}	Turn-On Switching Energy (SiC Diode FWD)		0.52		mJ	V_{DS} = 1200 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω, L= 99 μH, T_J = 150 °C, using SiC Diode as FWD	Fig. 26, 29b Note 2
E_{OFF}	Turn Off Switching Energy (SiC Diode FWD)		0.43				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		2.0		mJ	V_{DS} = 1200 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω, L= 99 μH, T_J = 150 °C, using MOSFET as FWD	Fig. 26, 29a Note 2
E_{OFF}	Turn Off Switching Energy (Body Diode FWD)		0.31				
$t_{d(on)}$	Turn-On Delay Time		15		ns	V_{DD} = 1200 V, V_{GS} = -5/20 V I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 27, 29 Note 2
t_r	Rise Time		18				
$t_{d(off)}$	Turn-Off Delay Time		34				
t_f	Fall Time		12				
$R_{G(int)}$	Internal Gate Resistance		1.3		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		46		nC	V_{DS} = 1200 V, V_{GS} = -5/20 V I_D = 50 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		71				
Q_g	Total Gate Charge		204				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 1200V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 1200V

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Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.8		V	V_{GS} = - 5 V, I_{SD} = 25 A	Fig. 8, 9, 10 Note 1
		3.4		V	V_{GS} = - 5 V, I_{SD} = 25 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		76	A	V_{GS} = - 5 V, T_C= 25 °C	Note 1
$I_{S, pulse}$	Diode pulse Current		160	A	V_{GS} = - 5 V, pulse width t_P limited by T_{jmax}	Note 1
t_{rr}	Reverse Recovery Time	44		ns	V_{GS} = - 5 V, I_{SD} = 50 A , V_R = 1200 V dif/dt = 3000 A/μs, T_J = 150 °C	
Q_{rr}	Reverse Recovery Charge	1.9		uC		
I_{rrm}	Peak Reverse Recovery Current	64		A		
t_{rr}	Reverse Recovery Time	25		ns	V_{GS} = - 5 V, I_{SD} = 50 A , V_R = 1200 V dif/dt = 13450 A/μs, T_J = 150 °C	
Q_{rr}	Reverse Recovery Charge	2.4		uC		
I_{rrm}	Peak Reverse Recovery Current	166		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.22	0.37	°C/W		Fig. 21
$R_{\theta JC}$	Thermal Resistance from Junction to Ambient		40			

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Typical Performance

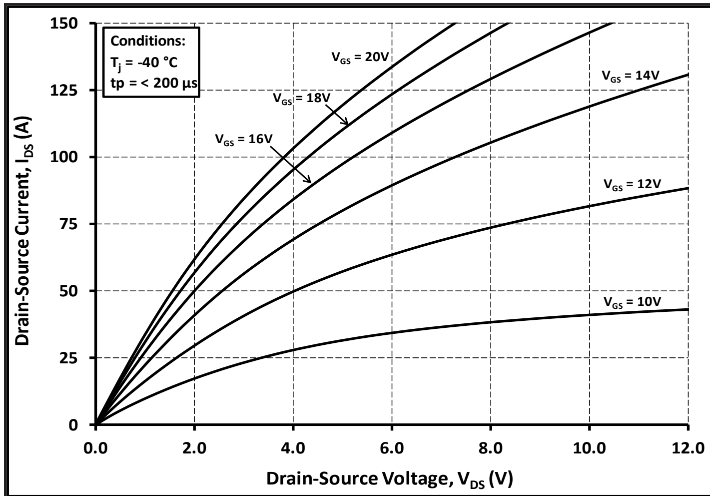

Figure 1. Output Characteristics T_J = -40 °C

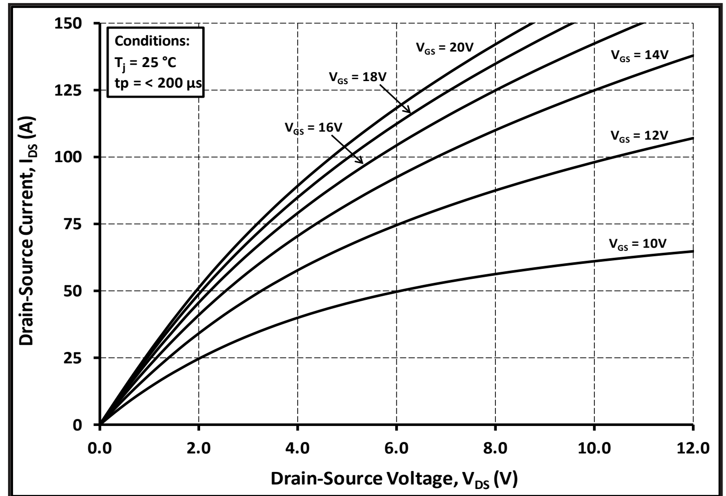

Figure 2. Output Characteristics T_J = 25 °C

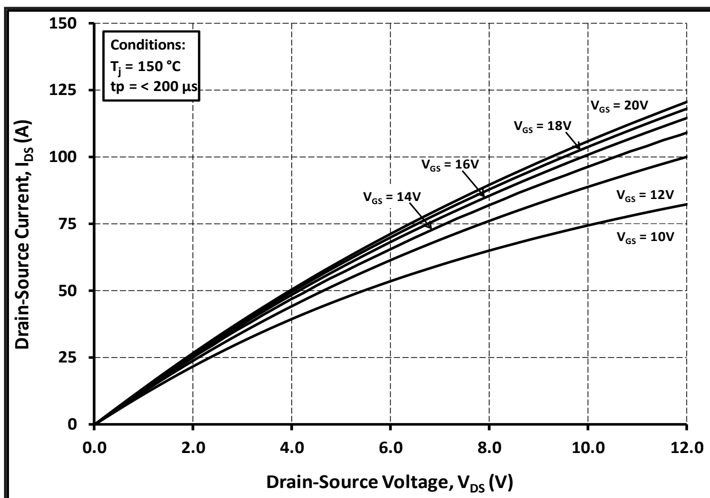

Figure 3. Output Characteristics T_J = 150 °C

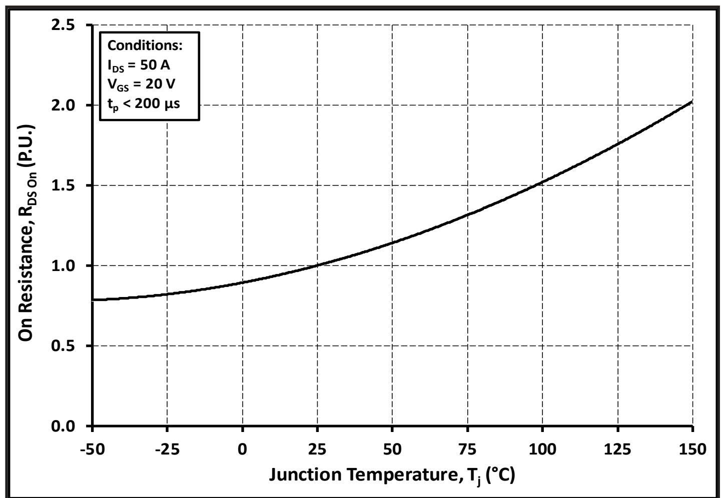

Figure 4. Normalized On-Resistance vs. Temperature

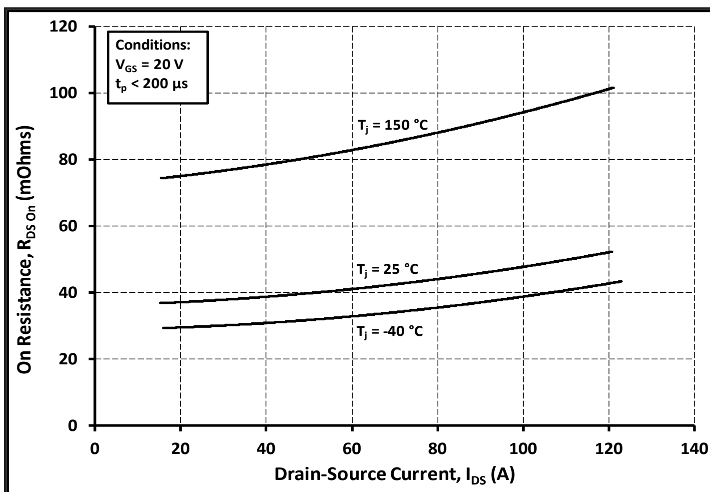

Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

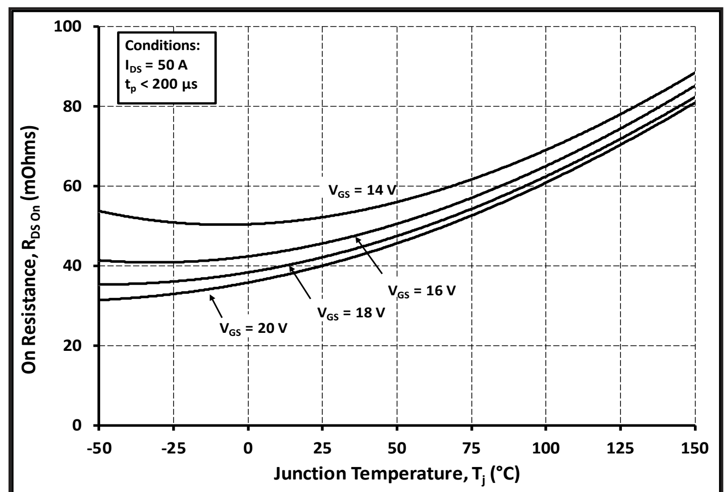

Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

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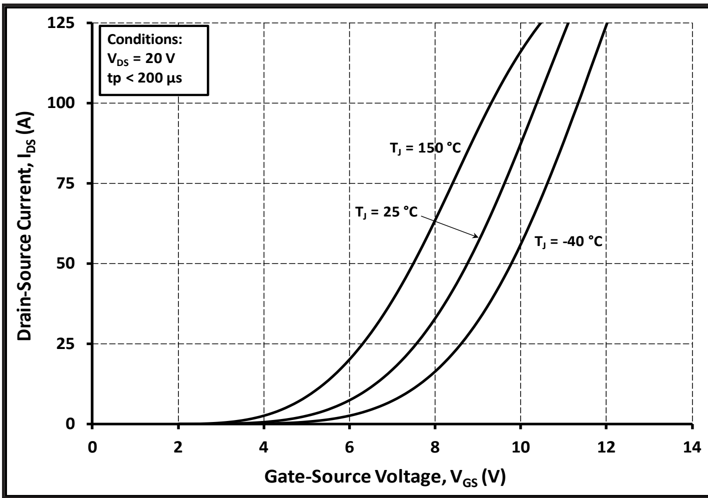

Figure 7. Transfer Characteristic For Various Junction Temperatures

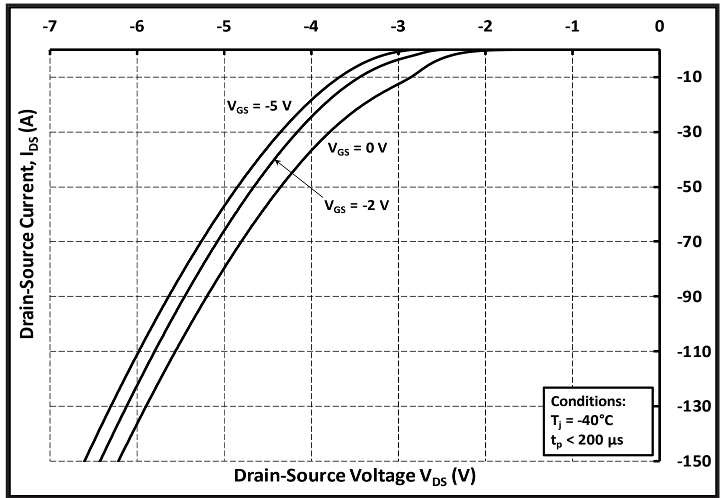

Figure 8. Body Diode Characteristic at -40 °C

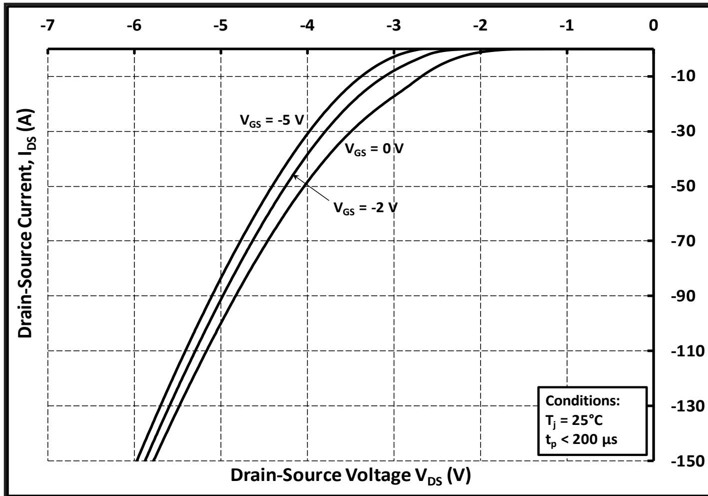

Figure 9. Body Diode Characteristic at 25 °C

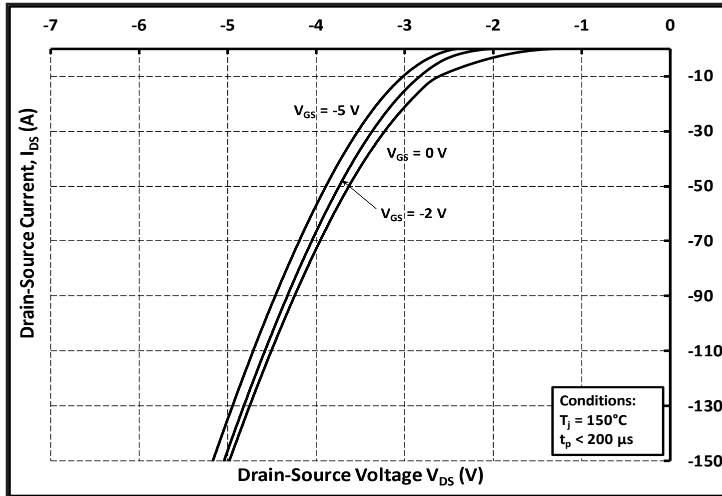

Figure 10. Body Diode Characteristic at 150 °C

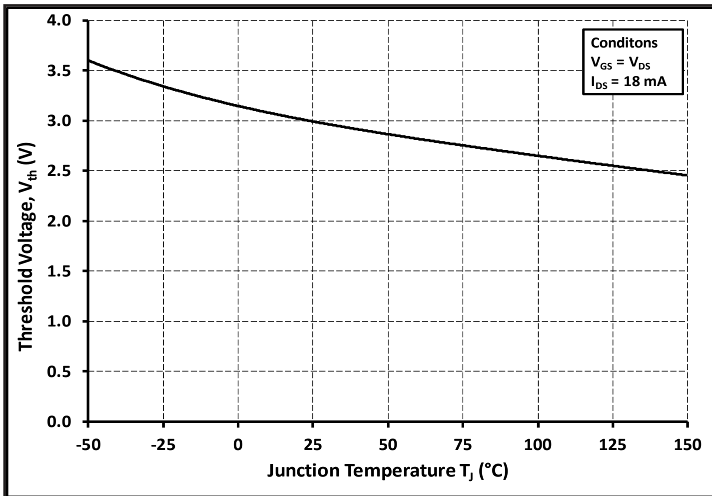

Figure 11. Threshold Voltage vs. Temperature

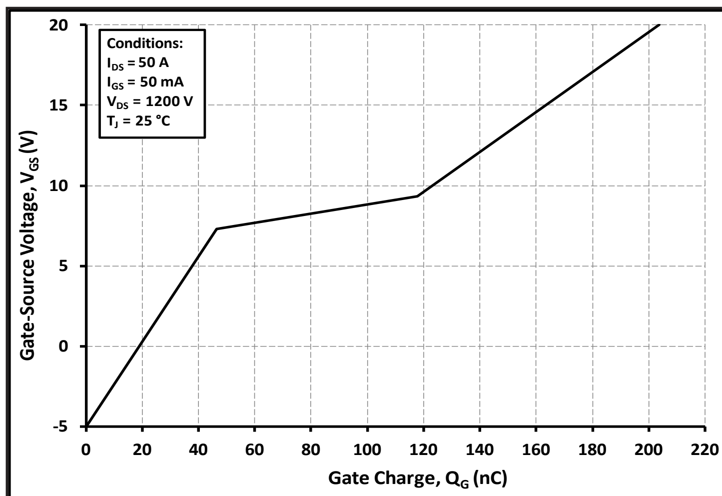

Figure 12. Gate Charge Characteristic

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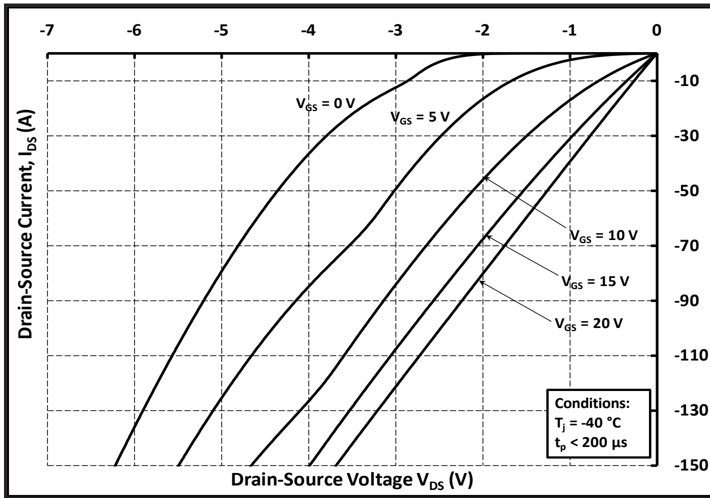

Figure 13. 3rd Quadrant Characteristic at -40 °C

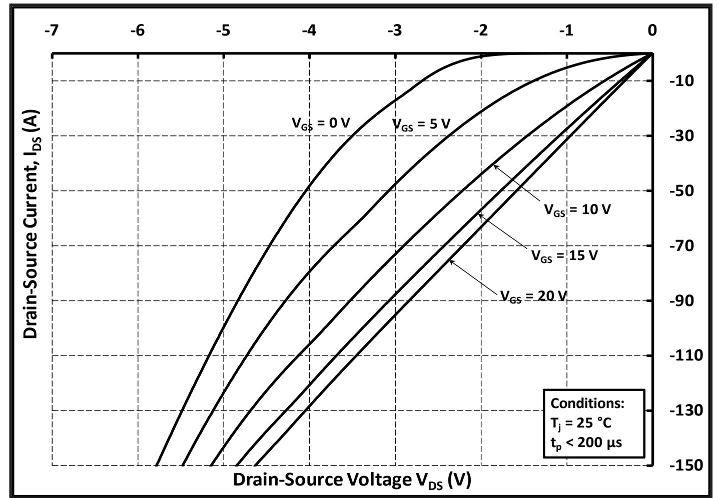

Figure 14. 3rd Quadrant Characteristic at 25 °C

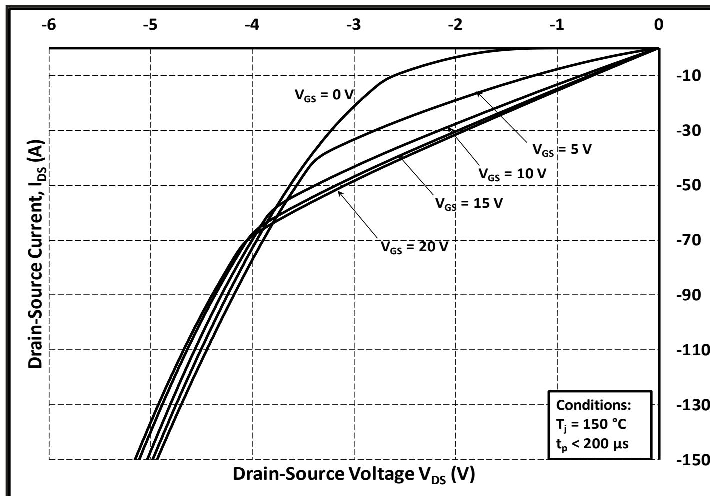

Figure 15. 3rd Quadrant Characteristic at 150 °C

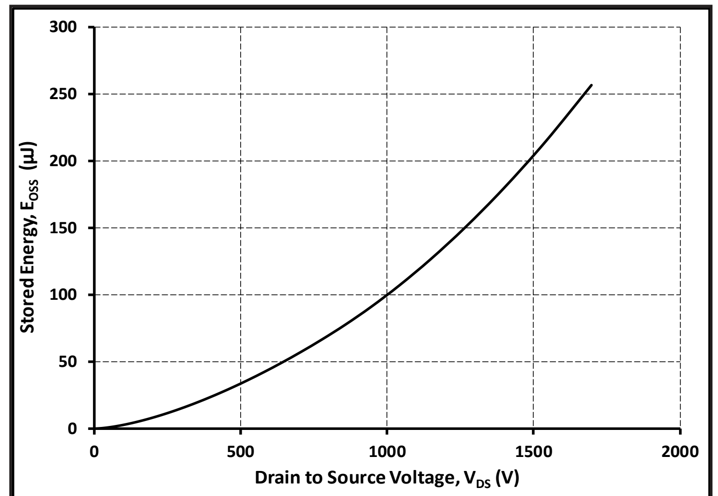

Figure 16. Output Capacitor Stored Energy

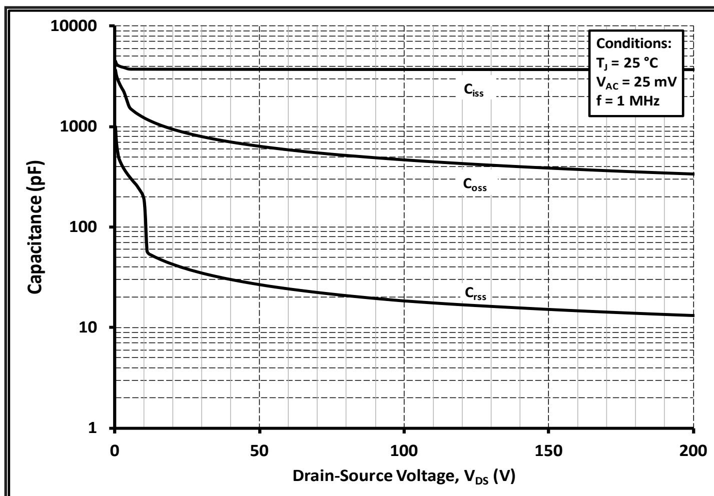

Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

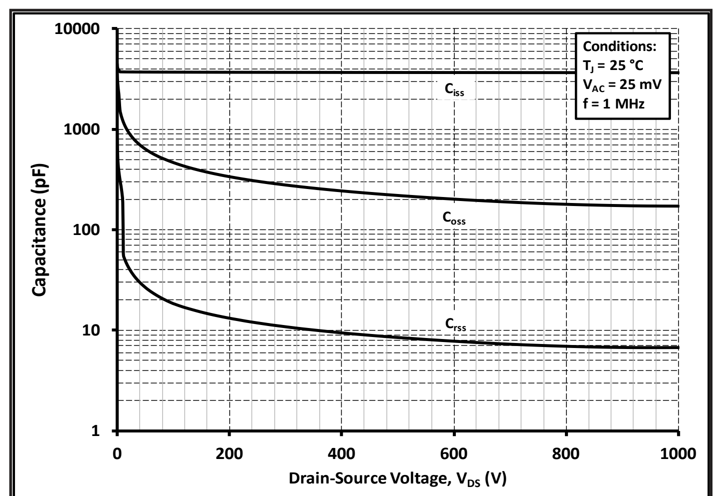

Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

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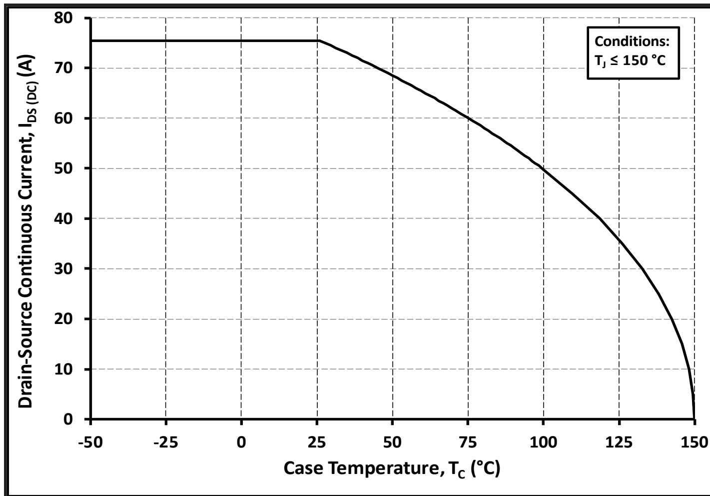

Figure 19. Continuous Drain Current Derating vs. Case Temperature

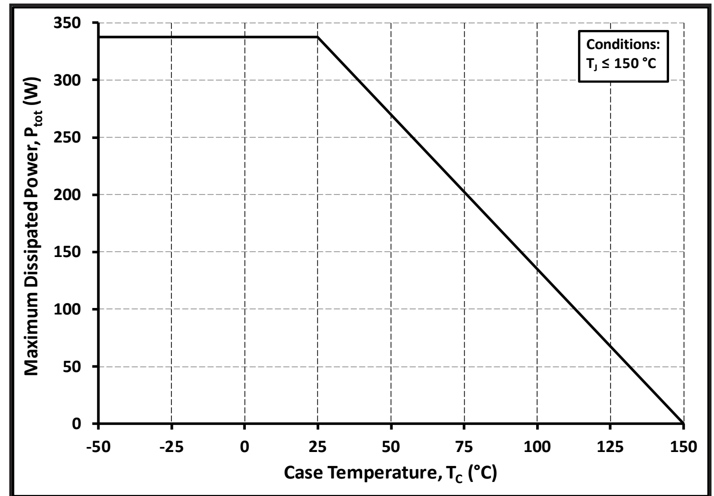

Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

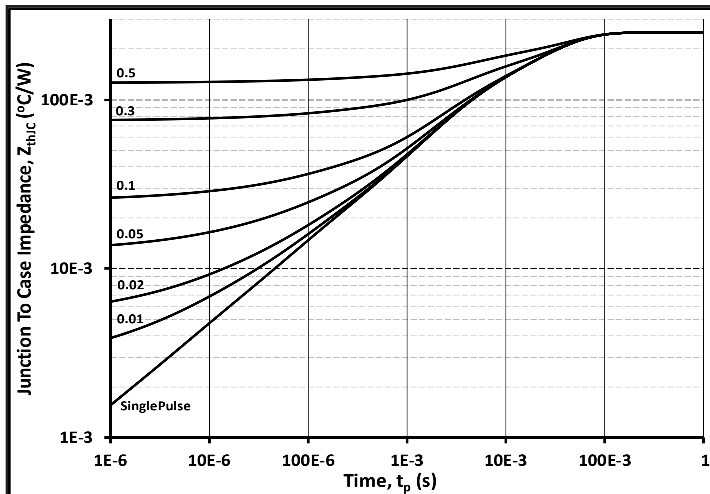

Figure 21. Transient Thermal Impedance (Junction - Case)

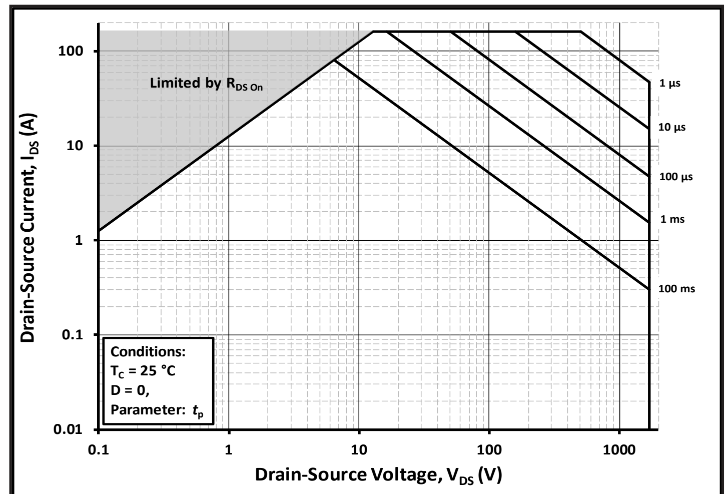

Figure 22. Safe Operating Area

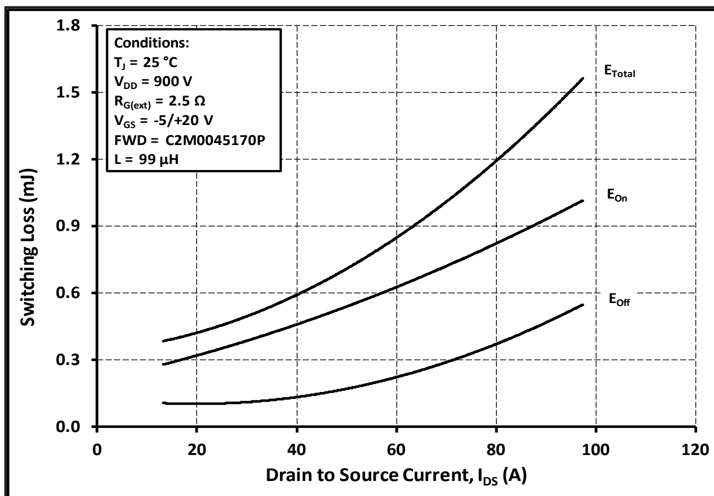

Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 900V)

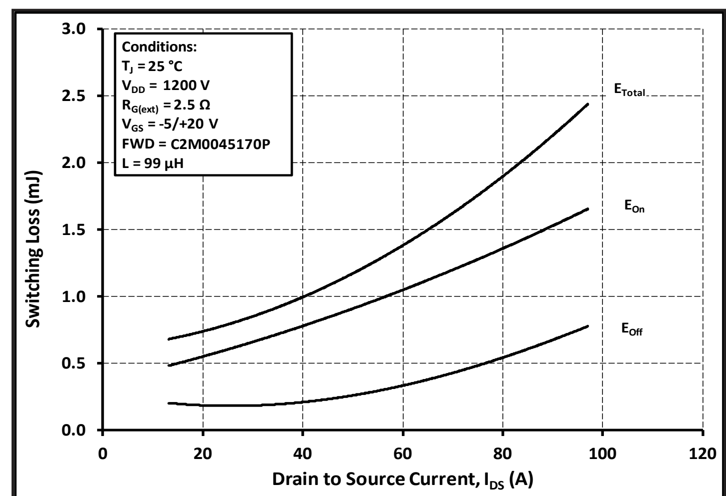

Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 1200V)

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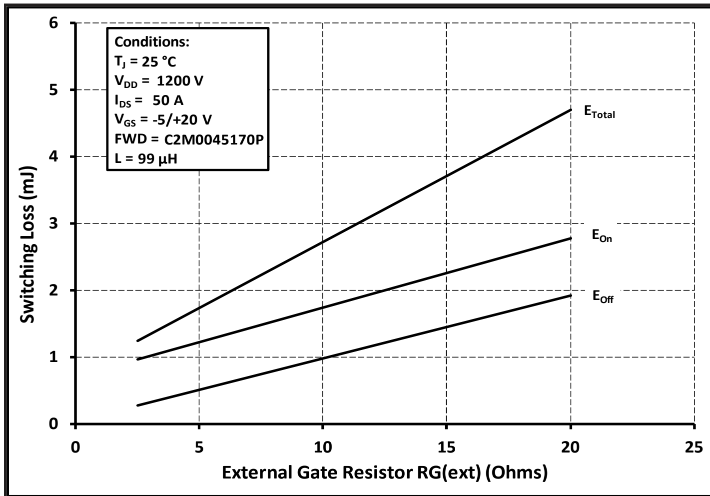

Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

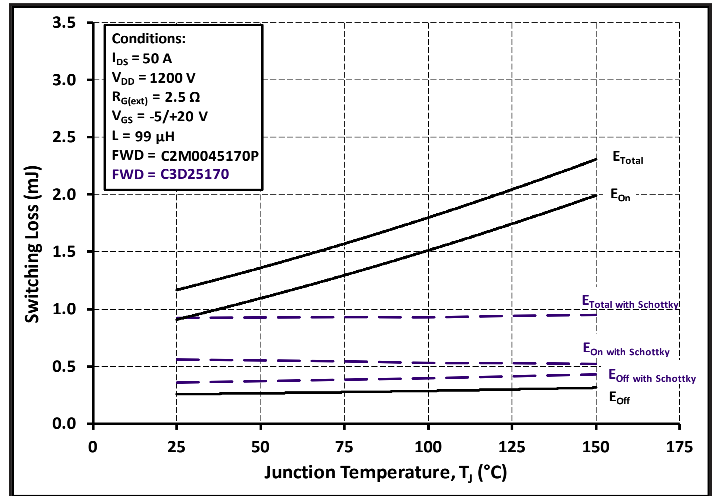

Figure 26. Clamped Inductive Switching Energy vs. Temperature

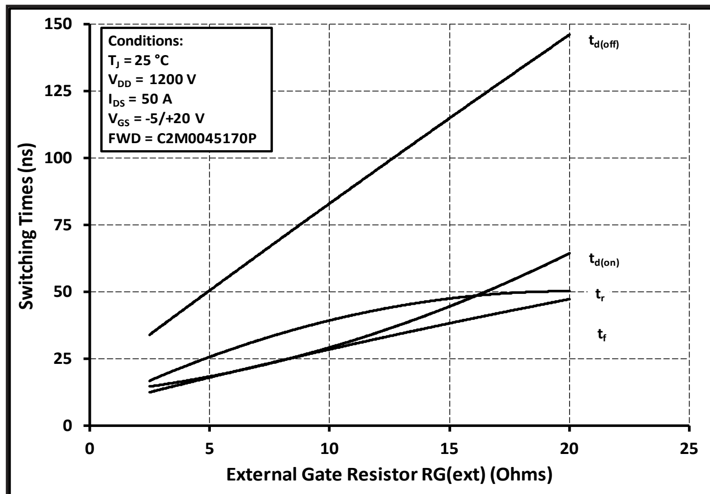

Figure 27. Switching Times vs. $R_{G(ext)}$

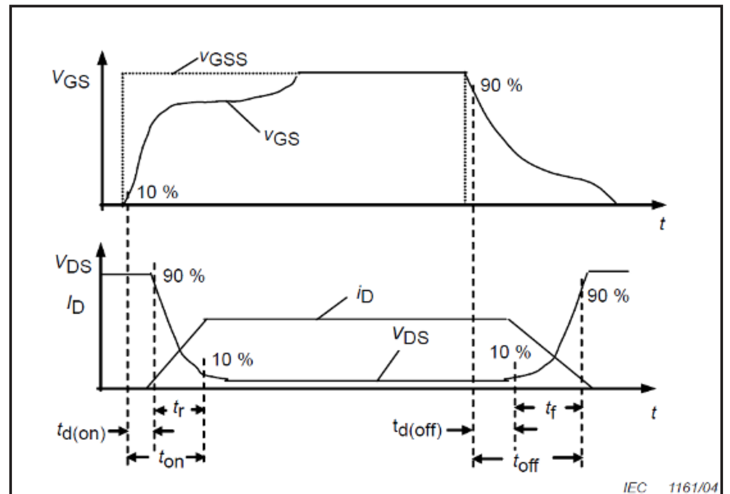

Figure 28. Switching Times Definition

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Test Circuit Schematic

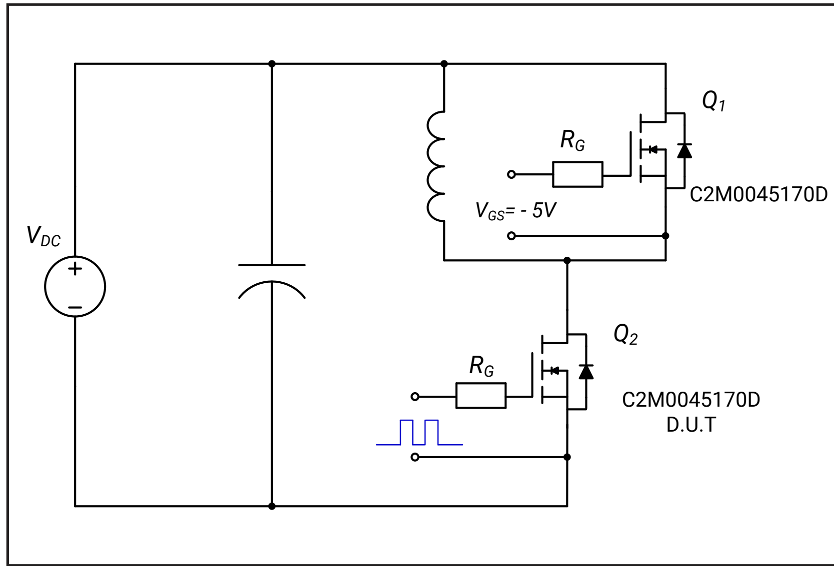

Figure 29a. Clamped Inductive Switching Test Circuit using MOSFET intristic body diode

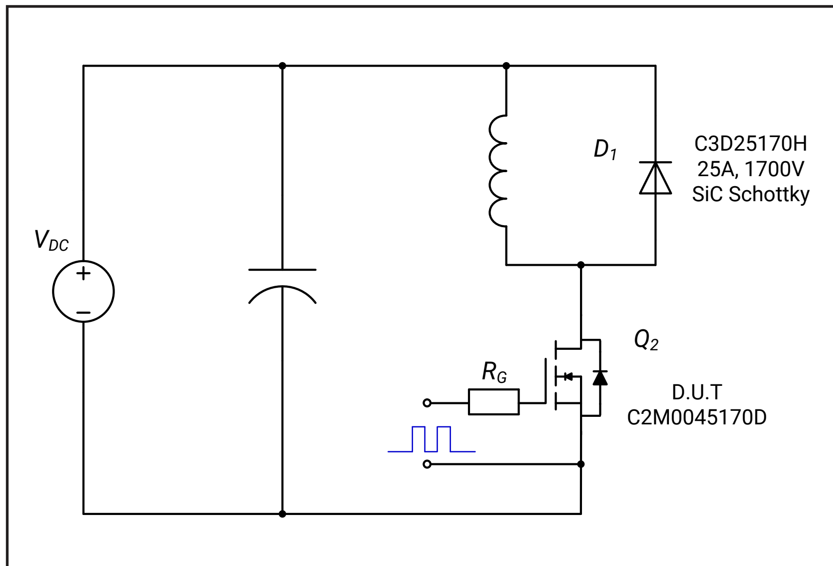

Figure 29b. Clamped Inductive Switching Test Circuit using SiC Schottky diode

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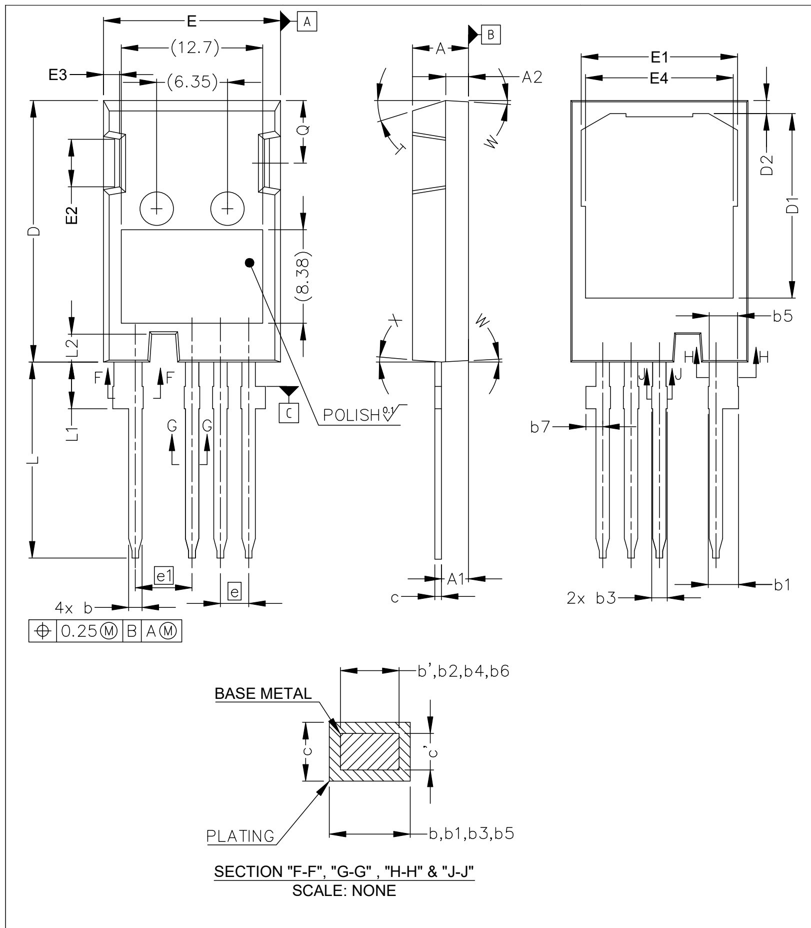
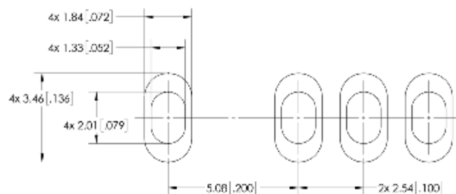
Package Dimensions



SYM	MILLIMETERS	
	MIN	MAX
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	2.39	2.94
b2	2.39	2.84
b3	1.07	1.60
b4	1.07	1.50
b5	2.39	2.69
b6	2.39	2.64
b7	1.30	1.70
c'	0.55	0.65
c	0.55	0.68
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
N*	4	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
Q	5.49	6.00
T	17.5° REF.	
W	3.5 ° REF.	
X	4° REF.	

Recommended Solder Pad Layout



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Revision history

Document Version	Date of release	Descriptiion of changes
Rev -	April - 2018	Initial datasheet
Rev 1	NA	Revision 1 not released.
Rev 2	May - 2022	Added effective output capacitance, Typical values updated to support PCN-1278.

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REACh Compliance
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