

#### SNAS538C – JUNE 1999 – REVISED FEBRUARY 2013

# DAC0800/DAC0802 8-Bit Digital-to-Analog Converters

Check for Samples: DAC0800, DAC0802

## **FEATURES**

- Fast Settling Output Current: 100 ns
- Full Scale Error: ±1 LSB
- Nonlinearity Over Temperature: ±0.1%
- Full Scale Current Drift: ±10 ppm/°C
- High Output Compliance: -10V to +18V
- Complementary Current Outputs
- Interface Directly with TTL, CMOS, PMOS and Others
- 2 Quadrant Wide Range Multiplying Capability
- Wide Power Supply Range: ±4.5V to ±18V
- Low Power Consumption: 33 mW at ±5V
- Low Cost

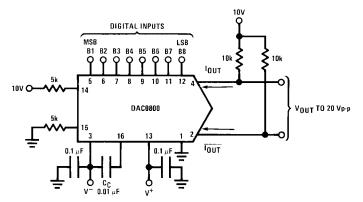
## DESCRIPTION

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads. The reference-to-full-scale current matching of better than  $\pm$ 1 LSB eliminates the need for full-scale trims in most applications, while the nonlinearities of better than  $\pm$ 0.1% over temperature minimizes system error accumulations.

The noise immune inputs will accept a variety of logic levels. The performance and characteristics of the device are essentially unchanged over the  $\pm 4.5V$  to  $\pm 18V$  power supply range and power consumption at only 33 mW with  $\pm 5V$  supplies is independent of logic input levels.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively. For single supply operation, refer to AN-1525.

## **Typical Application**



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

### Figure 1. ±20 V<sub>P-P</sub> Output Digital-to-Analog Converter

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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### Absolute Maximum Ratings <sup>(1)</sup>

Supply Voltage (V <sup>+</sup> – V <sup>-</sup> )	±18V or 36V
Power Dissipation <sup>(2)</sup>	500 mW
Reference Input Differential Voltage	
(V14 to V15)	V <sup>-</sup> to V <sup>+</sup>
Reference Input Common-Mode	
Range (V14, V15)	V <sup>-</sup> to V <sup>+</sup>
Reference Input Current	5 mA
Logic Inputs	V <sup>−</sup> to V <sup>−</sup> plus 36V
Analog Current Outputs	
(V <sub>S</sub> -=-15V)	4.25 mA
ESD Susceptibility <sup>(3)</sup>	TBD V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
PDIP Package (plastic)	260°C
CDIP Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions. The maximum junction temperature of the DAC0800 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the

(2)CDIP package must be derated based on a thermal resistance of 100°C/W, junction-to-ambient, 175°C/W for the molded PDIP package and 100°C/W for the SOIC package. Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

(3)

## **Operating Conditions**<sup>(1)</sup>

	Min	Max	Units
Temperature (T <sub>A</sub> )			
DAC0800L	-55	+125	°C
DAC0800LC	0	+70	°C
DAC0802LC	0	+70	°C
V <sup>+</sup>	(V <sup>−</sup> ) + 10	(V <sup>-</sup> ) + 30	V
V-	-15	-5	V
$I_{REF} (V^{-} = -5V)$	1	2	mA
$I_{REF} (V^{-} = -15V)$	1	4	mA

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not (1) apply when operating the device beyond its specified operating conditions.



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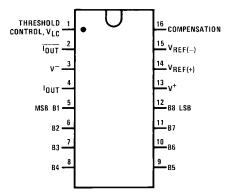
### **Electrical Characteristics**

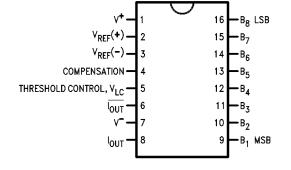
The following specifications apply for  $V_S = \pm 15V$ ,  $I_{REF} = 2$  mA and  $T_{MIN} \le T_A \le T_{MAX}$  unless otherwise specified. Output characteristics refer to both  $I_{OUT}$  and  $\overline{I_{OUT}}$ .

	Parameter	Test Conditions	D	AC0802L	.C		AC0800		Units
			Min	Тур	Max	Min	Тур	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19	%FS
		To $\pm \frac{1}{2}$ LSB, All Bits Switched "ON" or "OFF", T <sub>A</sub> =25°C		100	135				ns
t <sub>s</sub>	Settling Time	DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
t <sub>PLH</sub> ,	Propagation Delay	T <sub>A</sub> =25°C							
t <sub>PHL</sub>	Each Bit			35	60		35	60	ns
	All Bits Switched			35	60		35	60	ns
TCI <sub>FS</sub>	Full Scale Tempco			±10	±50		±10	±50	ppm/°C
V <sub>OC</sub>	Output Voltage Compliance	Full Scale Current Change <½ LSB, R <sub>OUT</sub> >20 MΩ, Typical	-10		18	-10		18	V
I <sub>FS4</sub>	Full Scale Current	$V_{REF} = 10.000V,$ R14 = R15 = 5.000 kΩ, T <sub>A</sub> =25°C	1.984	1.992	2.00	1.94	1.99	2.04	mA
I <sub>FSS</sub>	Full Scale Symmetry	I <sub>FS4</sub> -I <sub>FS2</sub>		±0.5	±4.0		±1	±8.0	μA
I <sub>ZS</sub>	Zero Scale Current			0.1	1.0		0.2	2.0	μA
I <sub>FSR</sub>	Output Current Range	$V^{-} = -5V$ V <sup>-</sup> = -8V to -18V	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
	Logic Input Levels	$V_{LC} = 0V$							
V <sub>IL</sub>	Logic "0"				0.8			0.8	V
VIH	Logic "1"		2.0			2.0			V
	Logic Input Current	$V_{LC} = 0V$							
I <sub>IL</sub>	Logic "0"	$-10V \le V_{IN} \le +0.8V$		-2.0	-10		-2.0	-10	μA
IIH	Logic "1"	$2V \le V_{IN} \le +18V$		0.002	10		0.002	10	μA
V <sub>IS</sub>	Logic Input Swing	V <sup>-</sup> = -15V	-10		18	-10		18	V
V <sub>THR</sub>	Logic Threshold Range	V <sub>S</sub> = ±15V	-10		13.5	-10		13.5	V
I <sub>15</sub>	Reference Bias Current			-1.0	-3.0		-1.0	-3.0	μA
dl/dt	Reference Input Slew Rate	(Figure 26)	4.0	8.0		4.0	8.0		mA/µs
PSSI <sub>FS+</sub>	Positive Power Supply Sensitivity	4.5V ≤ V <sup>+</sup> ≤ 18V		0.0001	0.01		0.0001	0.01	%/%
PSSI <sub>FS-</sub>	Negative Power Supply Sensitivity	$-4.5V \le V^- \le 18V$ , $I_{REF} = 1mA$		0.0001	0.01		0.0001	0.01	%/%
l+	Dowor Supply Current	(1 - 15)(1 - 1 - 2)		2.3	3.8		2.3	3.8	mA
I-	Power Supply Current	$V_{S} = \pm 5V$ , $I_{REF} = 1 \text{ mA}$		-4.3	-5.8		-4.3	-5.8	mA
l+	David Overali Overali			2.4	3.8		2.4	3.8	mA
I-	Power Supply Current	$V_{S} = +5V, -15V, I_{REF} = 2 \text{ mA}$		-6.4	-7.8		-6.4	-7.8	mA
l+	David Overali Overali			2.5	3.8		2.5	3.8	mA
I-	Power Supply Current	$V_{S} = \pm 15V$ , $I_{REF} = 2 \text{ mA}$		-6.5	-7.8		-6.5	-7.8	mA
		±5V, I <sub>REF</sub> = 1 mA		33	48		33	48	mW
P <sub>D</sub>	Power Consumption	+5V, -15V, I <sub>REF</sub> = 2 mA		108	136		108	136	mW
-		$\pm 15V$ , I <sub>REF</sub> = 2 mA		135	174		135	174	mW



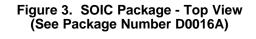
### **Connection Diagrams**

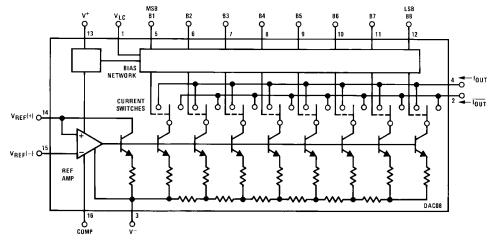






### **Block Diagram**





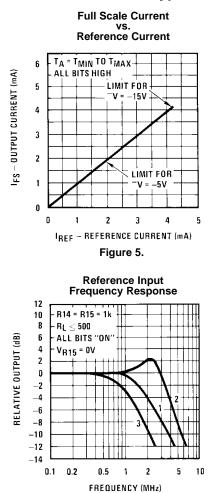
Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 4.

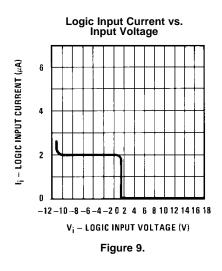


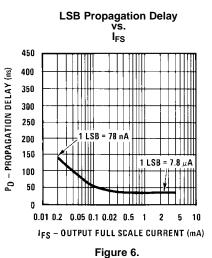
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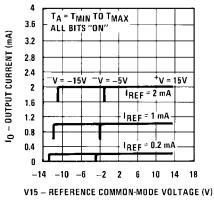


 $\begin{array}{l} \textbf{Curve 1: } C_{C}{=}15 \ \text{pF}, \ V_{IN}{=}2 \ \text{Vp-p} \ \text{centered at } 1V. \\ \textbf{Curve 2: } C_{C}{=}15 \ \text{pF}, \ V_{IN}{=}50 \ \text{mVp-p} \ \text{centered at } 200 \ \text{mV}. \\ \textbf{Curve 3: } C_{C}{=}0 \ \text{pF}, \ V_{IN}{=}100 \ \text{mVp-p} \ \text{centered at } 0V \ \text{and applied} \\ \text{through } 50\Omega \ \text{connected to pin } 14.2V \ \text{applied to } R14. \\ \textbf{Figure 7.} \end{array}$ 



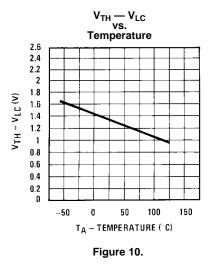






Note. Positive common-mode range is always (V+) - 1.5V.

Figure 8.



2.8

2.4

2

1.6

1.2

0.8

0.4

0

1.4

1.2

1

0.8

0.6

0.4

0.2

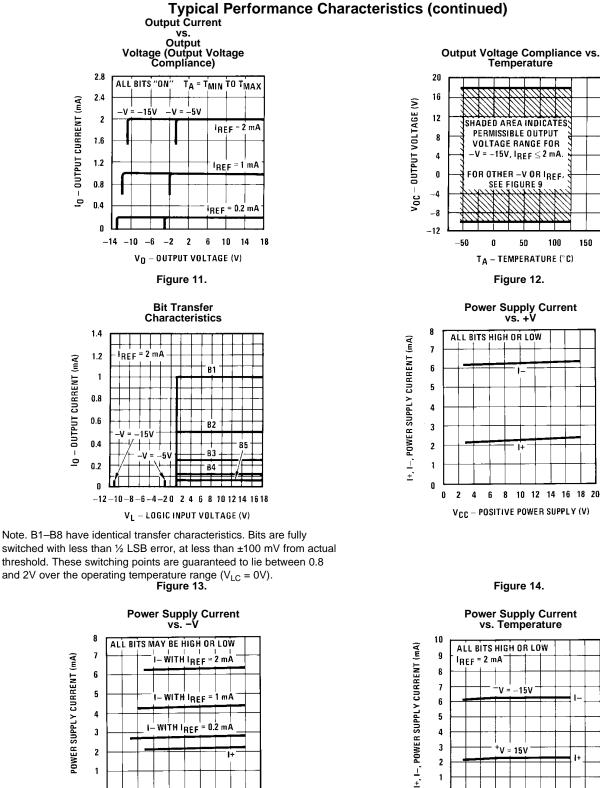
0

IQ – OUTPUT CURRENT (mA)

IREF

-15V

t<sub>0</sub> – OUTPUT CURRENT (mA)

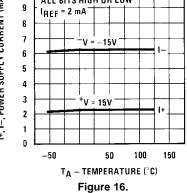




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**Power Supply Current** 



and 2V over the operating temperature range ( $V_{LC} = 0V$ ). Figure 13. Power Supply Current vs. -V 8 ALL BITS MAY BE HIGH OR LOW 7 POWER SUPPLY CURRENT (mA) I-WITH IREF - 2 mA 6 5 4 I-WITH IREF = 0.2 mA 3 2 1 Π -2 -4 -6 -8 -10 -12 -14 -16 -18 -20 0 V - NEGATIVE POWER SUPPLY (V)

Figure 15.

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#### **EQUIVALENT CIRCUIT**

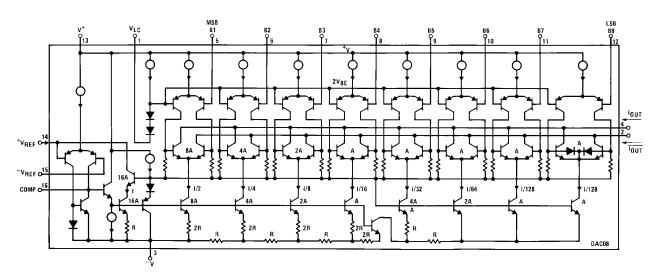


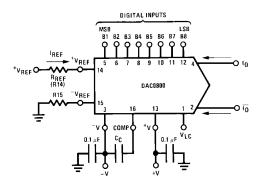
Figure 17. Equivalent Circuit



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### **TYPICAL APPLICATIONS**



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

$$I_{\text{FS}} \approx \frac{+ \, V_{\text{REF}}}{R_{\text{REF}}} \times \frac{255}{256}$$

$$\begin{split} &\mathsf{I}_{O}+\bar{\mathsf{I}}_{O}=\mathsf{I}_{FS} \text{ for all logic states} \\ &\mathsf{For fixed reference, TTL operation, typical values are:} \\ &\mathsf{V}_{REF}=10.000\mathsf{V} \\ &\mathsf{R}_{REF}=5.000\mathsf{k} \\ &\mathsf{R15}\approx\mathsf{R}_{REF} \\ &\mathsf{C}_{C}=0.01\ \mu\mathsf{F} \\ &\mathsf{V}_{LC}=0\mathsf{V} \mbox{ (Ground)} \end{split}$$



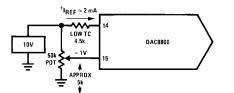




Figure 19. Recommended Full Scale Adjustment Circuit



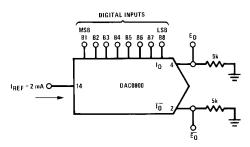
Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

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Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

#### Figure 21. Basic Unipolar Negative Operation

B1	B2	B3	B4	B5	B6	B7	B8	l <sub>o</sub> mA	Ī <sub>o</sub> mA	Eo	Eo		
1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000		
1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040		
1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920		
1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960		
0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000		
0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920		
0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960		
	1 1 1 1 1 0 0	1         1           1         1           1         0           1         0           0         1           0         0	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	B1         B2         B3         B4         B5         B6         B7           1         1         1         1         1         1         1           1         1         1         1         1         1         1           1         1         1         1         1         1         1           1         0         0         0         0         0         0           1         0         0         0         0         0         0           1         1         1         1         1         1         1           0         0         0         0         0         0         0           0         1         1         1         1         1         1           0         0         0         0         0         0         0	1         1	B1         B2         B3         B4         B5         B6         B7         B8         Io mA           1         1         1         1         1         1         1         1.992           1         1         1         1         1         1         1         1.992           1         1         1         1         1         1         1         1.992           1         1         1         1         1         1         1         1.992           1         0         0         0         0         0         1.984           1         0         0         0         0         0         1         1.008           1         0         0         0         0         0         0         1.000           0         1         1         1         1         1         1         0.992           0         0         0         0         0         0         1         0.008	B1         B2         B3         B4         B5         B6         B7         B8         I <sub>0</sub> mA         Ī <sub>0</sub> mA           1         1         1         1         1         1         1         1.992         0.000           1         1         1         1         1         1         1         1.992         0.000           1         1         1         1         1         1         1.992         0.008           1         1         1         1         1         1         0         0.984         0.008           1         0         0         0         0         0         1         1.008         0.984           1         0         0         0         0         0         0         0.992           0         1         1         1         1         1         1         0.992         1.000           0         0         0         0         0         0         1         0.008         1.984	B1         B2         B3         B4         B5         B6         B7         B8         Io mA         ĪomA         Eo           1         1         1         1         1         1         1         1.992         0.000         -9.960           1         1         1         1         1         1         1.992         0.000         -9.960           1         1         1         1         1         1         9.992         -0.008         -9.920           1         0         0         0         0         1         1.008         0.984         -5.040           1         0         0         0         0         0         0         0.992         -5.000           1         1         1         1         1         1         1.000         0.992         -5.000           0         1         1         1         1         1         0.992         1.000         -4.960           0         0         0         0         0         1         0.008         1.984         -0.040		

#### Table 1. Basic Unipolar Negative Operation



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 22. Basic Bipolar Output Operation

	B1	B2	B3	B4	B5	B6	B7	B8	Eo	Ēo
Pos. Full Scale	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos. Full Scale-LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale-LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920

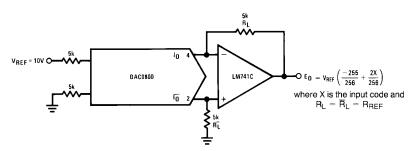
#### Table 2. Basic Bipolar Output Operation

# DAC0800, DAC0802



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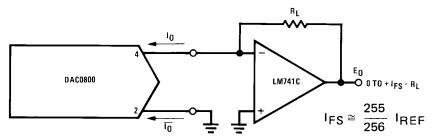


- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) If  $R_L = \overline{R}_L$  within ±0.05%, output is symmetrical about ground.

#### Figure 23. Symmetrical Offset Binary Operation

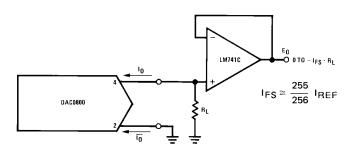
	B1	B2	B3	B4	B5	B6	B7	B8	Eo
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale-LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(-)Zero Scale	0	1	1	1	1	1	1	1	-0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	-9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	-9.960

#### Table 3. Symmetrical Offset Binary Operation



- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) For complementary output (operation as negative logic DAC), connect inverting input of op amp to  $\overline{I}_{O}$  (pin 2), connect  $I_{O}$  (pin 4) to ground.

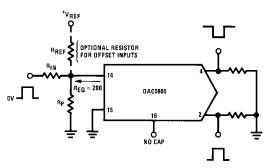
Figure 24. Positive Low Impedance Output Operation



- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to I
  <sub>0</sub> (pin 2); connect I
  <sub>0</sub> (pin 4) to ground.

#### Figure 25. Negative Low Impedance Output Operation

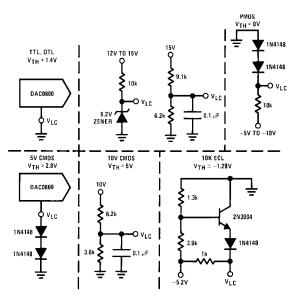




Typical values: R<sub>IN</sub>=5k,+V<sub>IN</sub>=10V

Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

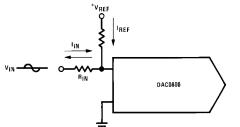
#### Figure 26. Pulsed Reference Operation



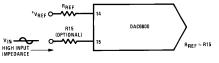
$$\begin{split} V_{TH} &= V_{LC} + 1.4V \\ 15V CMOS, HTL, HNIL \\ V_{TH} &= 7.6V \\ Note. \ Do \ not \ exceed \ negative \ logic \ input \ range \ of \ DAC. \end{split}$$

#### Figure 27. Interfacing with Various Logic Families





(b) +V<sub>REF</sub> must be above peak positive swing of  $V_{\text{IN}}$ 



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

Figure 28. Accommodating Bipolar References

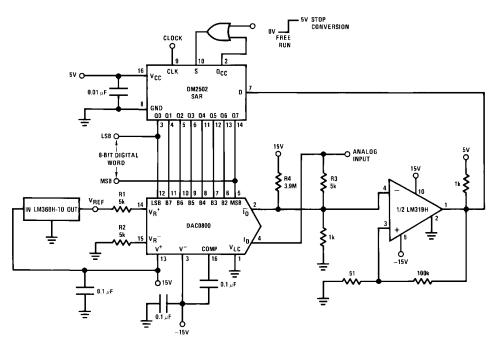


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FOR TURN "ON" FOR TURN "OFF V<sub>L</sub> = 2.7V V<sub>L</sub> = 0.7V MINIMUM HP5082-2800 SCHOTTKY DIODES VCL 0.7V VOUT 1 x probe RREF 10 11 12 <sup>+</sup>VREF**O** юлт DAC0800 (D.U.T.) TO D.U.T 0.01 µF 0.1 al

Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

#### Figure 29. Settling Time Measurement



- (1) For 1  $\mu$ s conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 k $\Omega$  and R4 to 2 M $\Omega$ .
- (2) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

#### Figure 30. A Complete 2 µs Conversion Time, 8-Bit A/D Converter

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## **REVISION HISTORY**

Ch	Changes from Revision B (February 2013) to Revision C Provide								
•	Changed layout of National Data Sheet to TI format	1:	2						

EXAS
STRUMENTS

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CI	Changes from Revision B (February 2013) to Revision C								
	Changed layout of National Data Sheet to TI format								



30-Sep-2016

## PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
DAC-08EP	LIFEBUY	PDIP	NFG	16		TBD	Call TI	Call TI	0 to 70	DAC0800LCN DAC-08EP	
DAC0800LCM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 70	DAC0800LCM	
DAC0800LCM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM	Samples
DAC0800LCMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70	DAC0800LCM	
DAC0800LCMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM	Samples
DAC0800LCN	OBSOLETE	PDIP	NFG	16		TBD	Call TI	Call TI	0 to 70	DAC0800LCN DAC-08EP	
DAC0800LCN/NOPB	ACTIVE	PDIP	NFG	16	25	Pb-Free (RoHS)	SN	Level-1-NA-UNLIM	0 to 70	DAC0800LCN DAC-08EP	Samples
DAC0802LCMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70	DAC0802LCM	
DAC0802LCMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DAC0802LCM	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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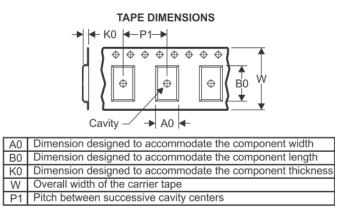
# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC0800LCMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DAC0800LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DAC0802LCMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DAC0802LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

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# PACKAGE MATERIALS INFORMATION

18-Aug-2014

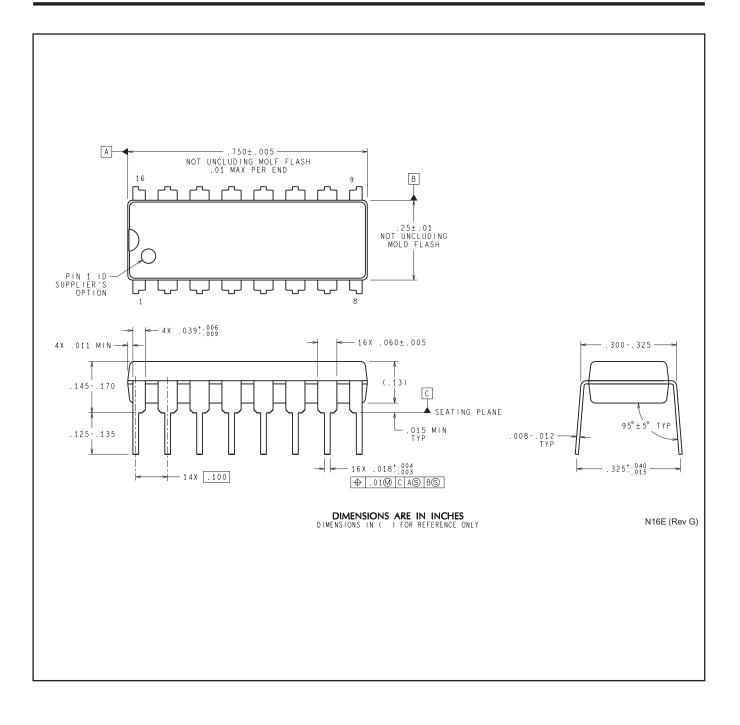


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC0800LCMX	SOIC	D	16	2500	367.0	367.0	35.0
DAC0800LCMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
DAC0802LCMX	SOIC	D	16	2500	367.0	367.0	35.0
DAC0802LCMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

# **MECHANICAL DATA**

# NFG0016E





D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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