8-Bit, 60 MSPS A/D Converter

AD9057

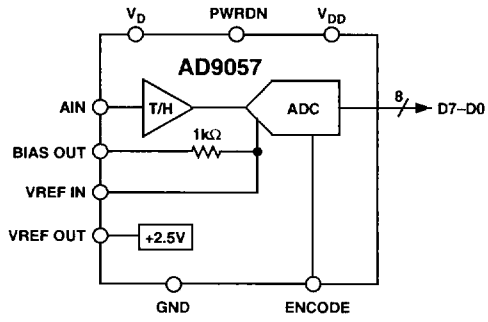
FEATURES

8-Bit, Low Power ADC: 200 mW Typical
120 MHz Analog Bandwidth
On-Chip +2.5 V Reference and T/H
1 V p-p Analog Input Range
Single +5 V Supply Operation
+5 V or +3 V Logic Interface
Power-Down Mode: < 10 mW

APPLICATIONS

Digital Communications (QAM Demodulators)
RGB & YC/Composite Video Processing
Digital Data Storage Read Channels
Medical Imaging
Digital Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9057 is an 8-bit monolithic analog-to-digital converter optimized for low cost, low power, small size, and ease of use. With a 60 MSPS encode rate capability and full-power analog bandwidth of 120 MHz, the component is ideal for applications requiring excellent dynamic performance.

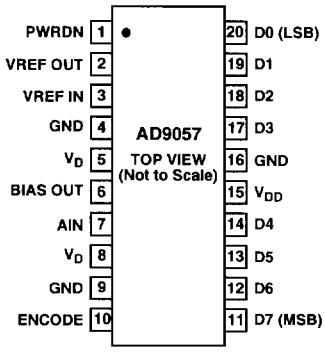
To minimize system cost and power dissipation, the AD9057 includes an internal +2.5 V reference and a track-and-hold circuit. The user must provide only a +5 V power supply and an encode clock. No external reference or driver components are required for many applications.

The AD9057's encode input is TTL/CMOS compatible and the 8-bit digital outputs can be operated from +5 V or +3 V supplies. A power-down function may be exercised to bring total consumption to < 10 mW. In power-down mode the digital outputs are driven to a high impedance state.

Fabricated on an advanced BiCMOS process, the AD9057 is available in a space saving 20-lead surface mount plastic package (20 SSOP) and is specified over the industrial (–40°C to +85°C) temperature range.

Customers desiring multichannel digitization may consider the AD9059, a dual 8-bit, 60 MSPS monolithic based on the AD9057 ADC core. The AD9059 is available in a 28-lead surface mount plastic package (28 SSOP) and is specified over the industrial temperature range.

PIN CONFIGURATION



REV. 0

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AD9057–SPECIFICATIONS (V_D = +5 V, V_{DD} = +3 V; external reference; ENCODE = 60 MSPS unless otherwise noted)

Parameter	Temp	Test Level	AD9057BRS Min	AD9057BRS Typ	AD9057BRS Max	Units
RESOLUTION				8		Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.75	1.5	LSB
	Full	VI			2.0	LSB
Integral Nonlinearity	+25°C	I		0.75	1.5	LSB
	Full	VI			2.0	LSB
No Missing Codes	Full	VI		GUARANTEED		
Gain Error[1]	+25°C	I	–6	–2.5	+6	% FS
	Full	VI	–8		+8	% FS
Gain Tempco[1]	Full	V		±70		ppm/°C
ANALOG INPUT						
Input Voltage Range (Centered at +2.5 V)	+25°C	V		1.0		V p-p
Input Offset Voltage	+25°C	I	–15	±0	+15	mV
	Full	VI	–25		+25	mV
Input Resistance	+25°C	V		150		kΩ
Input Capacitance	+25°C	V		2		pF
Input Bias Current	+25°C	I		6	16	µA
	Full	VI			25	µA
Analog Bandwidth	+25°C	V		120		MHz
BANDGAP REFERENCE						
Output Voltage	Full	VI	2.4	2.5	2.6	V
Temperature Coefficient	Full	V		±10		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	60			MSPS
Minimum Conversion Rate	Full	IV			5	MSPS
Aperture Delay (t_A)	+25°C	V		2.7		ns
Aperture Uncertainty (Jitter)	+25°C	V		5		ps, rms
Output Valid Time (t_V)[2]	Full	IV	4.0	6.6		ns
Output Propagation Delay (t_{PD})[2]	Full	IV		9.5	14.2	ns
DYNAMIC PERFORMANCE[3]						
Transient Response	+25°C	V		9		ns
Overvoltage Recovery Time	+25°C	V		9		ns
Signal-to-Noise Ratio (SINAD)						
(With Harmonics)						
f_{IN} = 10.3 MHz	+25°C	I	42	45		dB
f_{IN} = 76 MHz	+25°C	V		43.5		dB
Effective Number of Bits						
f_{IN} = 10.3 MHz	+25°C	I	6.7	7.2		Bits
f_{IN} = 76 MHz	+25°C	V		6.9		Bits
Signal-to-Noise Ratio (SNR)						
(Without Harmonics)						
f_{IN} = 10.3 MHz	+25°C	I	43	46		dB
f_{IN} = 76 MHz	+25°C	V		45		dB
2nd Harmonic Distortion						
f_{IN} = 10.3 MHz	+25°C	I	–50	–62		dBc
f_{IN} = 76 MHz	+25°C	V		–54		dBc
3rd Harmonic Distortion						
f_{IN} = 10.3 MHz	+25°C	I	–46	–60		dBc
f_{IN} = 76 MHz	+25°C	V		–54		dBc
Two Tone Intermodulation Distortion (IMD)	+25°C	V		–52		dBc
Differential Phase	+25°C	V		0.8		Degrees
Differential Gain	+25°C	V		1.0		%
DIGITAL INPUTS						
Logic "1" Voltage	Full	VI	2.0			V
Logic "0" Voltage	Full	VI			0.8	V
Logic "1" Current	Full	VI			±1	µA
Logic "0" Current	Full	VI			±1	µA
Input Capacitance	+25°C	V		4.5		pF
Encode Pulse Width High (t_{EH})	+25°C	IV	6.7		166	ns
Encode Pulse Width Low (t_{EL})	+25°C	IV	6.7		166	ns

Parameter	Temp	Test Level	Min	Typ	Max	Units
DIGITAL OUTPUTS						
Logic "1" Voltage (V_{DD} = +3 V)	Full	VI	2.95			V
Logic "1" Voltage (V_{DD} = +5 V)	Full	IV	4.95			V
Logic "0" Voltage	Full	VI			0.05	V
Output Coding				Offset Binary Code		
POWER SUPPLY						
V_D Supply Current (V_D = +5 V)	Full	VI		38	48	mA
V_{DD} Supply Current (V_{DD} = +3 V)[4]	Full	VI		5.5	6.5	mA
Power Dissipation[5, 6]	Full	VI		205	260	mW
Power-Down Dissipation	Full	VI		6	10	mW
Power Supply Rejection Ratio (PSRR)	+25°C	I			15	mV/V

NOTES

[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed +2.5 V external reference).

[2]t_V and t_{PD} are measured from the 1.5 V level of the ENCODE to the 10%/90% levels of the digital output swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 μA.

[3]SNR/harmonics based on an analog input voltage of -0.5 dBFS referenced to a 1.0 V full-scale input range.

[4]Digital supply current based on V_{DD} = +3 V output drive with <10 pF loading under dynamic test conditions.

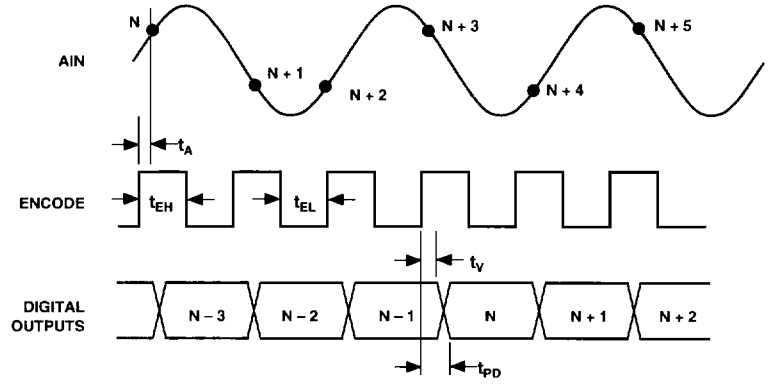
[5]Power dissipation is based on 60 MSPS encode and 10.3 MHz analog input dynamic test conditions (V_D = +5 V ± 5%, V_{DD} = +3 V ± 5%).

[6]Typical thermal impedance for the RS style (SSOP) 20-pin package: θ_{JC} = 46°C/W, θ_{CA} = 80°C/W, θ_{JA} = 126°C/W.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level	Description
I	100% Production Tested
II	100% Production Tested at +25°C and Sample Tested at Specified Temperatures
III	Sample Tested Only
IV	Parameter is Guaranteed by Design and Characterization Testing
V	Parameter is a Typical Value Only
VI	100% Production Tested at +25°C; Guaranteed by Design and Characterization Testing for Industrial Temperature Range



		MIN	TYP	MAX
t_A	APERTURE DELAY		2.7 ns	
t_{EH}	PULSE WIDTH HIGH	6.7 ns		166 ns
t_{EL}	PULSE WIDTH LOW	6.7 ns		166 ns
t_V	OUTPUT VALID TIME	4.0 ns	6.6 ns	
t_{PD}	OUTPUT PROP DELAY		9.5 ns	14.2 ns

Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

V_D, V_{DD} ..... +7 V
Analog Inputs ..... -0.5 V to V_D + 0.5 V
Digital Inputs ..... -0.5 V to V_{DD} + 0.5 V
V_{REF} Input ..... -0.5 V to V_D + 0.5 V
Digital Output Current ..... 20 mA
Operating Temperature ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature ..... +175°C
Maximum Case Temperature ..... +150°C

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9057BRS	-40°C to +85°C	RS-20
AD9057/PCB	+25°C	Evaluation Board

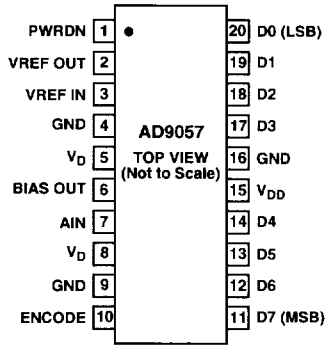
Table I. Digital Coding (VREF = +2.5 V)

Analog Input	Voltage Level	Digital Output
3.0 V	Positive Full Scale	1111 1111
2.502 V	Midscale +1/2 LSB	1000 0000
2.498 V	Midscale -1/2 LSB	0111 1111
2.0	Negative Full Scale	0000 0000

PIN DESCRIPTIONS

Pin No.	Name	Function
1	PWRDN	Power-Down Function Select; Logic HIGH for Power-Down Mode (Digital Outputs Go to High Impedance State).
2	VREF OUT	Internal Reference Output (+2.5 V typ); Bypass with 0.1 µF to Ground.
3	VREF IN	Reference Input for ADC (+2.5 V typ, ±10%).
4, 9, 16	GND	Ground (Analog/Digital).
5, 8	V_D	Analog +5 V Power Supply.
6	BIAS OUT	Bias Pin for AC Coupling (1 kΩ to REF IN).
7	AIN	Analog Input for ADC.
10	ENCODE	Encode Clock for ADC (ADC Samples on Rising Edge of ENCODE).
11-14, 17-20	D7-D4, D3-D0	Digital Outputs of ADC.
15	V_{DD}	Digital Output Power Supply. Nominally +3 V to +5 V.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9057 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

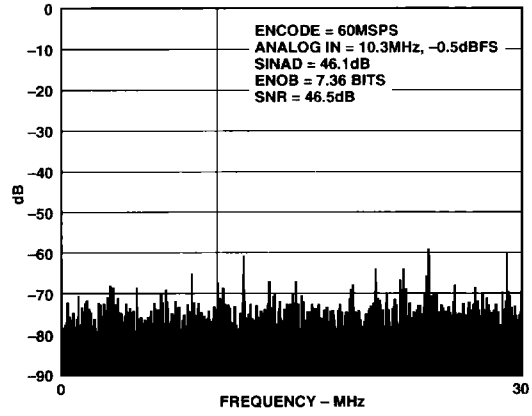


Figure 2. Spectral Plot 60 MSPS, 10.3 MHz

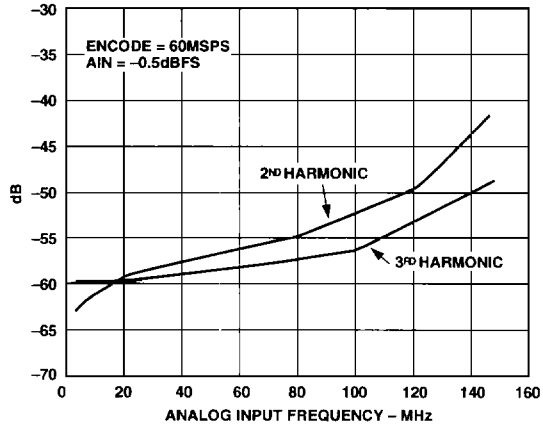


Figure 5. Harmonic Distortion vs. AIN Frequency

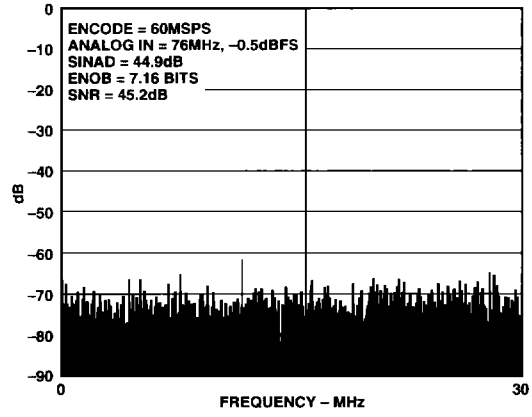


Figure 3. Spectral Plot 60 MSPS, 76 MHz

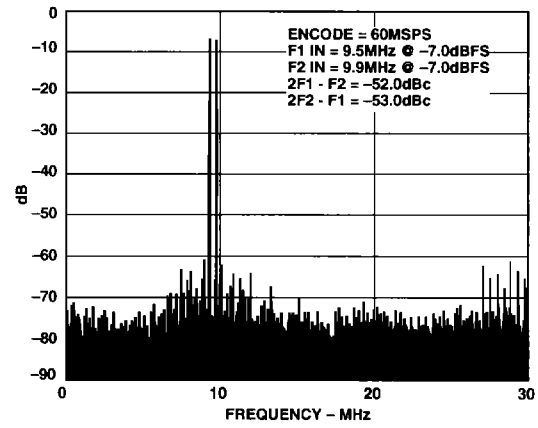


Figure 6. Two-Tone Intermodulation Distortion

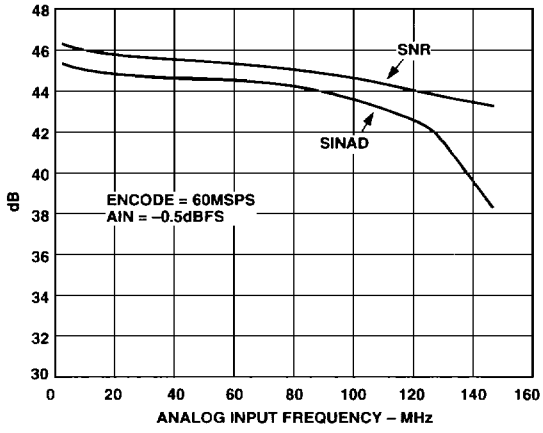


Figure 4. SINAD/SNR vs. AIN Frequency

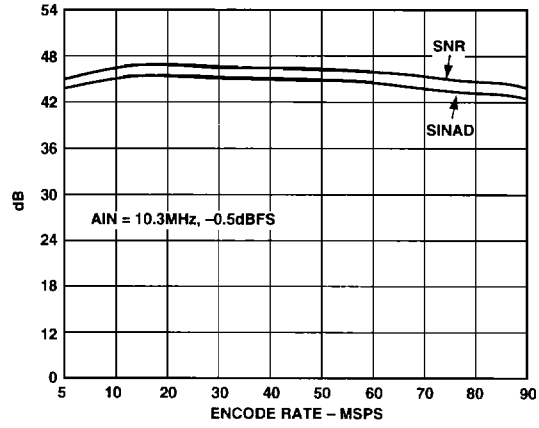


Figure 7. SINAD/SNR vs. Encode Rate

AD9057–Typical Performance Characteristics

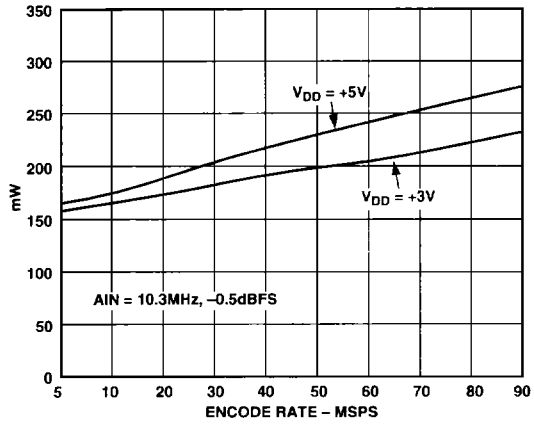


Figure 8. Power Dissipation vs. Encode Rate

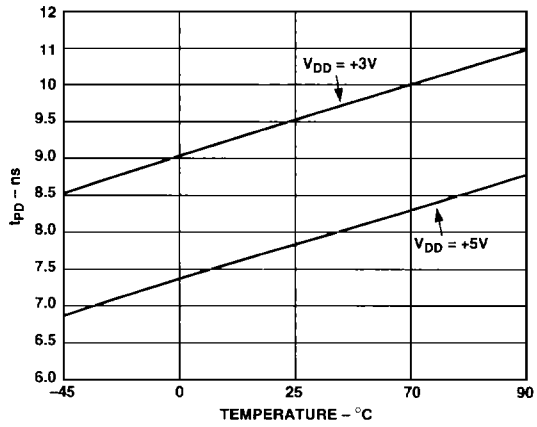


Figure 11. t_{PD} vs. Temperature/Supply (V_{DD} = +3 V/+5 V)

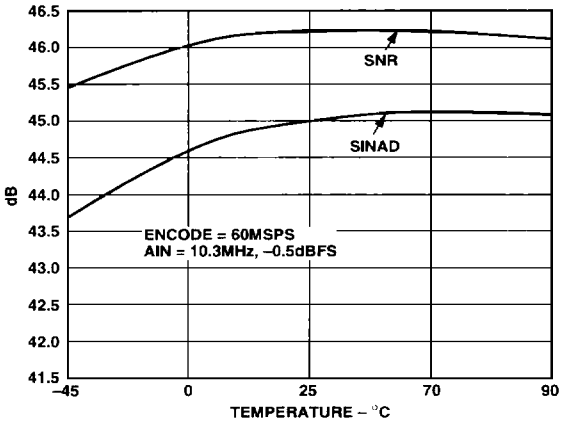


Figure 9. SINAD/SNR vs. Temperature

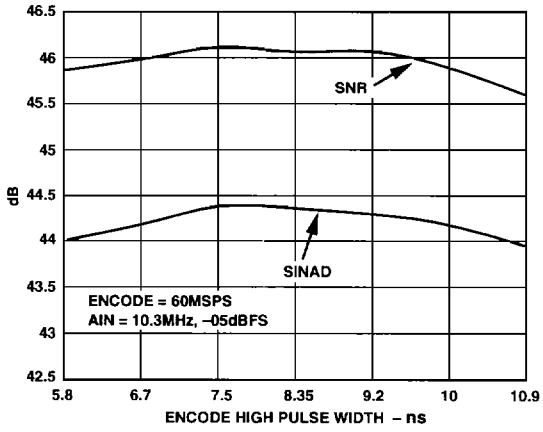


Figure 12. SINAD/SNR vs. Encode Pulse Width

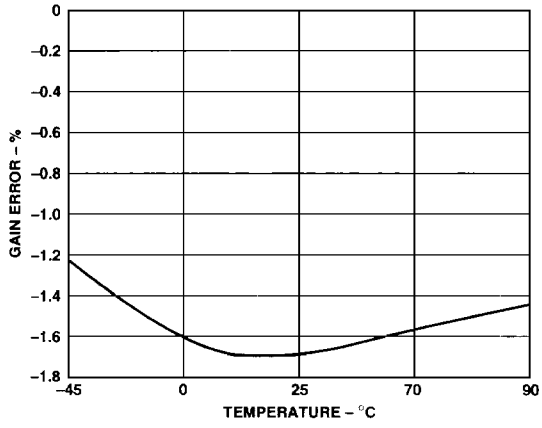


Figure 10. ADC Gain vs. Temperature (with External +2.5 V Reference)

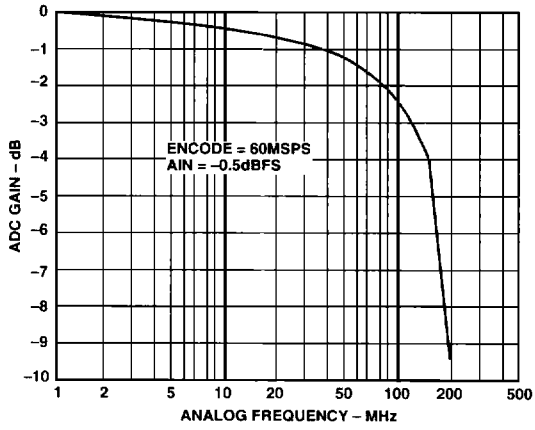


Figure 13. ADC Frequency Response

THEORY OF OPERATION

The AD9057 combines Analog Devices' proprietary MagAmp gray code conversion circuitry with flash converter technology to provide a high performance, low cost ADC. The design architecture ensures low power, high speed, and 8-bit accuracy. A single-ended TTL/CMOS compatible ENCODE input controls ADC timing for sampling the analog input pin and strobing the digital outputs (D7–D0). An internal voltage reference (VREF OUT) may be used to control ADC gain and offset or an external reference may be applied.

The analog input signal is buffered at the input of the ADC and applied to a high speed track-and-hold. The T/H circuit holds the analog input value during the conversion process (beginning with the rising edge of the ENCODE command). The T/H's output signal passes through the gray code and flash conversion stages to generate coarse and fine digital representations of the held analog input level. Decode logic combines the multistage data and aligns the 8-bit word for strobed outputs on the rising edge of the ENCODE command. The MagAmp/Flash architecture of the AD9057 results in three pipeline delays for the output data.

USING THE AD9057

Analog Inputs

The AD9057 provides a single-ended analog input impedance of 150 kΩ. The input requires a dc bias current of 6 µA (typical) centered near +2.5 V (±10%). The dc bias may be provided by the user or may be derived from the ADC's internal voltage reference. Figure 14 shows a low cost dc bias implementation allowing the user to capacitively couple ac signals directly into the ADC without additional active circuitry. For best dynamic performance, the VREF OUT pin should be decoupled to ground with a 0.1 µF capacitor (to minimize modulation of the reference voltage) and the bias resistor should be approximately 1 kΩ. A 1 kΩ bias resistor (±20%) is included within the AD9057 and may be used to reduce application board size and complexity.

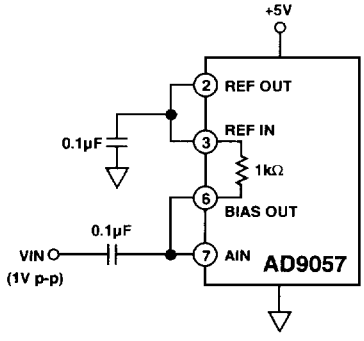


Figure 14. Capacitively Coupled AD9057

Figure 15 shows typical connections for high performance dc biasing using the ADC's internal voltage reference. All components may be powered from a single +5 V supply (in the example analog input signals are referenced to ground).

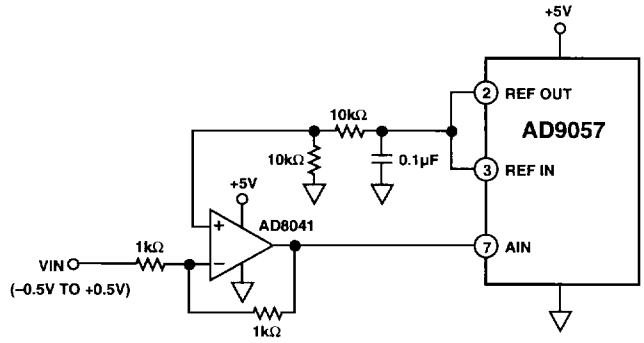


Figure 15. DC Coupled AD9057 (Inverted VIN)

Voltage Reference

A stable and accurate +2.5 V voltage reference is built into the AD9057 (VREF OUT). The reference output may be used to set the ADC gain / offset by connecting VREFOUT to VREF IN. The internal reference is capable of providing 300 µA of drive current (for dc biasing the analog input or other user circuitry).

Some applications may require greater accuracy, improved temperature performance, or gain adjustments which cannot be obtained using the internal reference. An external voltage may be applied to the VREF IN with VREF OUT disconnected for gain adjustment of up to ±10% (the VREF IN pin is internally tied directly to the ADC circuitry). ADC gain and offset will vary simultaneously with external reference adjustment with a 1:1 ratio (a 2% or 50 mV adjustment to the +2.5 V reference varies ADC gain by 2% and ADC input range center offset by 50 mV). Theoretical input voltage range versus reference input voltage may be calculated from the following equations:

$$V_{RANGE}\ (p\text{-}p) = VREF\ IN/2.5$$

$$V_{MIDSCALE} = VREF\ IN$$

$$V_{TOP\text{-}OF\text{-}RANGE} = VREF\ IN + V_{RANGE}/2$$

$$V_{BOTTOM\text{-}OF\text{-}RANGE} = VREF\ IN - V_{RANGE}/2$$

Digital Logic (+5 V/+3 V Systems)

The digital inputs and outputs of the AD9057 can easily be configured to interface directly with +3 V or +5 V logic systems. The ENCODE and power-down (PWRDN) inputs are CMOS stages with TTL thresholds of 1.5 V, making the inputs compatible with TTL, +5 V CMOS, and +3 V CMOS logic families. As with all high speed data converters, the encode signal should be clean and jitter free to prevent degradation of ADC dynamic performance.

The AD9057's digital outputs will also interface directly with +5 V or +3 V CMOS logic systems. The voltage supply pin (V_{DD}) for these CMOS stages is isolated from the analog V_D voltage supply. By varying the voltage on this supply pin the digital output HIGH level will change for +5 V or +3 V systems. Care should be taken to isolate the V_{DD} supply voltage from the +5 V analog supply to minimize digital noise coupling into the ADC.

The AD9057 provides high impedance digital output operation when the ADC is driven into power-down mode (PWRDN, logic HIGH). A 200 ns (minimum) power-down time should be provided before a high impedance characteristic is required at the outputs. A 200 ns power-up period should be provided to ensure accurate ADC output data after reactivation (valid output data is available three clock cycles after the 200 ns delay).

Timing

The AD9057 is guaranteed to operate with conversion rates from 5 MSPS to 60 MSPS. At 60 MSPS the ADC is designed to operate with an encode duty cycle of 50%, but performance is insensitive to moderate variations. Pulse width variations of up to ±10% (allowing the encode signal to meet the minimum/maximum HIGH/LOW specifications) will cause no degradation in ADC performance (see Figure 1 timing diagram).

Power Dissipation

The power dissipation of the AD9057 is specified to reflect a typical application setup under the following conditions: encode is 60 MSPS, analog input is -0.5 dBFS at 10.3 MHz, V_D is +5 V, V_{DD} is +3 V, and digital outputs are loaded with 7 pF typical (10 pF maximum). The actual dissipation will vary as these conditions are modified in user applications. Figure 8 shows typical power consumption for the AD9057 versus ADC encode frequency and V_{DD} supply voltage.

A power-down function allows users to reduce power dissipation when ADC data is not required. A TTL/CMOS HIGH signal (PWRDN) shuts down portions of the ADC and brings total power dissipation to less than 10 mW. The internal bandgap voltage reference remains active during power-down mode to minimize ADC reactivation time. If the power-down function is not desired, Pin 1 should be tied to ground.

APPLICATIONS

The wide analog bandwidth of the AD9057 makes it attractive for a variety of high performance receiver and encoder applications. Figure 16 shows two ADCs in a typical low cost I & Q demodulator implementation for cable, satellite, or wireless LAN modem receivers. The excellent dynamic performance of the ADC at higher analog input frequencies and encode rates empowers users to employ direct IF sampling techniques (refer to Figure 3 spectral plot). IF sampling eliminates or simplifies analog mixer and filter stages to reduce total system cost and power.

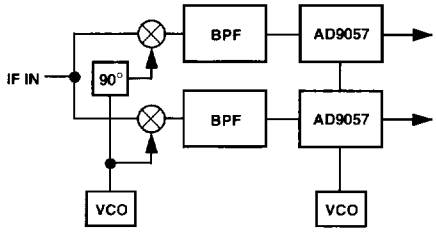


Figure 16. I & Q Digital Receiver

The high sampling rate and analog bandwidth of the AD9057 are ideal for computer RGB video digitizer applications. With a full-power analog bandwidth of 2× the maximum sampling rate, the ADC provides sufficient pixel to pixel transient settling time to ensure accurate 60 MSPS video digitization. Figure 17 shows a typical RGB video digitizer implementation for the AD9057.

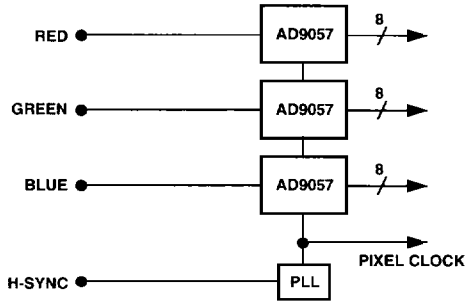


Figure 17. RGB Video Encoder

Evaluation Board

The AD9057/PCB evaluation board provides an easy to use analog/digital interface for the 8-bit, 60 MSPS ADC. The board includes typical hardware configurations for a variety of high speed digitization evaluations. On board components include the AD9057 (in the 20-pin SSOP package), an optional analog input buffer amplifier, a digital output latch, board timing drivers, an analog reconstruction digital-to-analog converter, and configurable jumpers for ac coupling, dc coupling, and power-down function testing. The board is configured at shipment for dc coupling using the AD9057's internal voltage reference.

For dc coupled analog input applications, amplifier U2 is configured to operate as a unity gain inverter with adjustable offset for the analog input signal. For full-scale ADC drive the analog input signal should be 1 V p-p into 50 Ω (R1) referenced to ground (0 V). The amplifier offsets the analog signal by +VREF (+2.5 V typical) to center the voltage for proper ADC input drive. For dc coupled operation, connect E1 to E2 (analog input to R2) and E11 to E12 (amplifier output to analog input of AD9057) using the board jumper connectors. DC offset of the analog input signal can be modified by adjusting potentiometer R10.

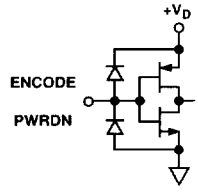
For ac coupled analog input applications, amplifier U2 is removed from the analog signal path. The analog signal is coupled into the input of the AD9057 through capacitor C2. The ADC pulls analog input bias current from the VREF IN voltage through the 1 kΩ resistor internal to the AD9057 (BIAS OUT). The analog input signal to the board should be 1 V p-p into 50 Ω (R1) for full-scale ADC drive. For ac coupled operation, connect E1 to E3 (analog input A to C2 feedthrough capacitor) and E10 to E12 (C2 to the analog input and internal bias resistor) using the board jumper connectors.

The onboard reference voltage may be used to drive the ADC or an external reference may be applied. To use the internal voltage reference, connect E6 to E5 (VREF OUT to VREF IN). To apply an external voltage reference, connect E4 to E5 (external reference from the REF banana jack to VREF IN). The external voltage reference should be +2.5 V ± 10%.

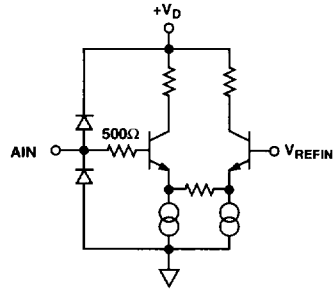
The power-down function of the AD9057 can be exercised through a board jumper connection. Connect E7 to E9 (+5 V to PWRDN) for power-down operation. For normal operation, connect E8 to E9 (ground to PWRDN).

The encode signal source should be TTL/CMOS compatible and capable of driving a 50 Ω termination (R7). The digital outputs of the AD9057 are buffered through latches on the evaluation board (U3) and are available for the user at connector Pins 30–37. Latch timing is derived from the ADC ENCODE clock and a digital clocking signal is provided for the board user at connector Pins 2 and 21.

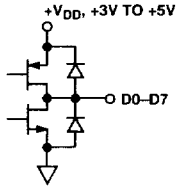
An onboard reconstruction digital-to-analog converter is available for quick evaluations of ADC performance using an oscilloscope or spectrum analyzer. The DAC converts the ADC's digital outputs to an analog signal for examination at the DAC OUT connector. The DAC is clocked at the ADC ENCODE frequency. The AD9760 is a 10-bit/100 MSPS single +5 V supply DAC. The reconstruction signal facilitates quick system troubleshooting or confirmation of ADC functionality without requiring external digital memory, timing, or display interfaces. The DAC can be used for limited dynamic testing, but customers should note that test results will be based on the combined performance of the ADC and DAC (the best ADC performance will be recognized by evaluating the digital outputs of the ADC directly).



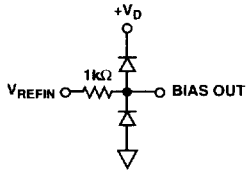
Digital Inputs



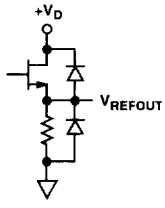
Analog Input



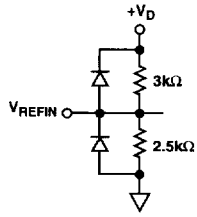
Digital Outputs



Bias Output



V_{REF} Output



V_{REF} Input

Figure 18. Equivalent Circuits

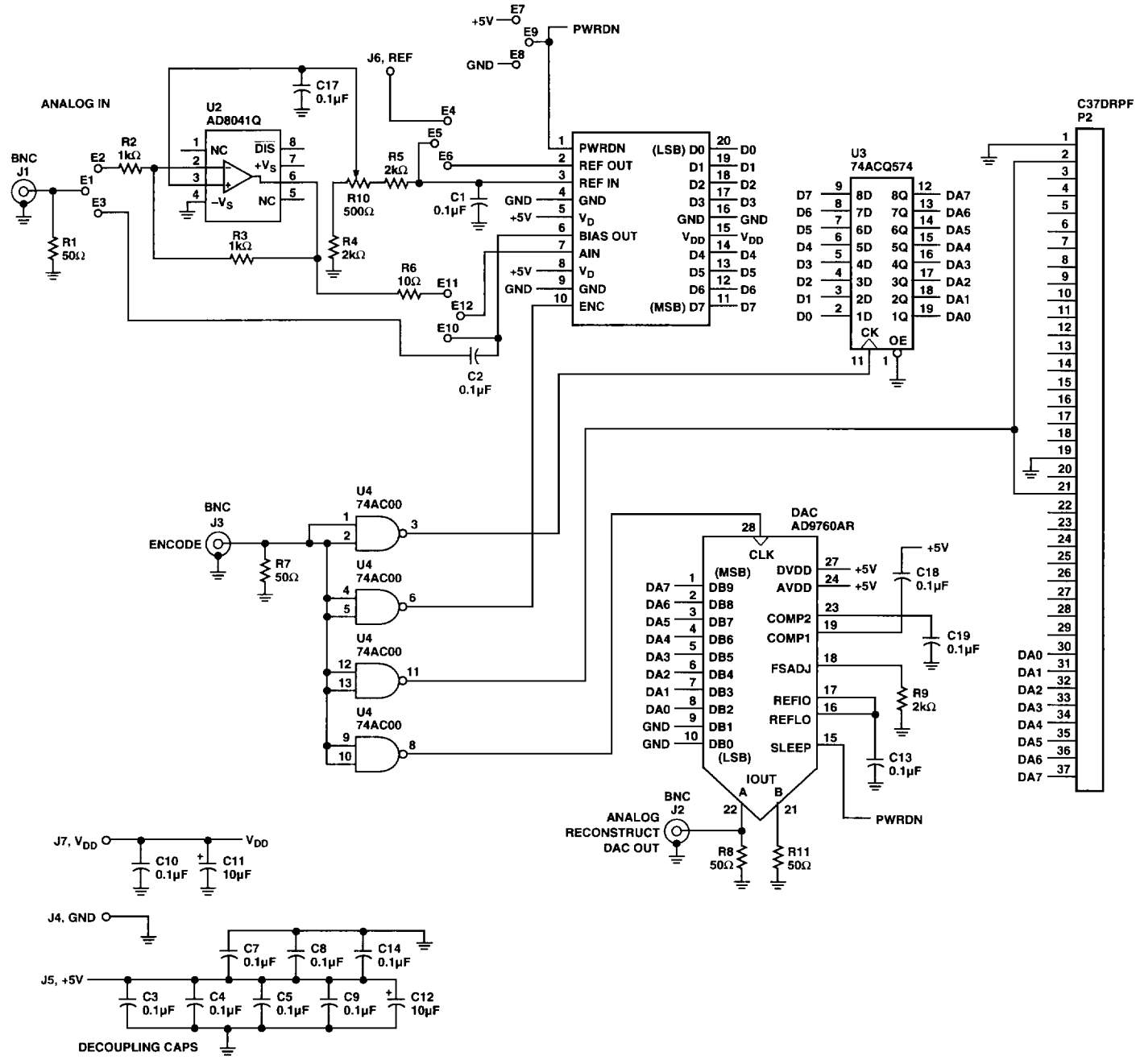


Figure 19. Evaluation Board Schematic

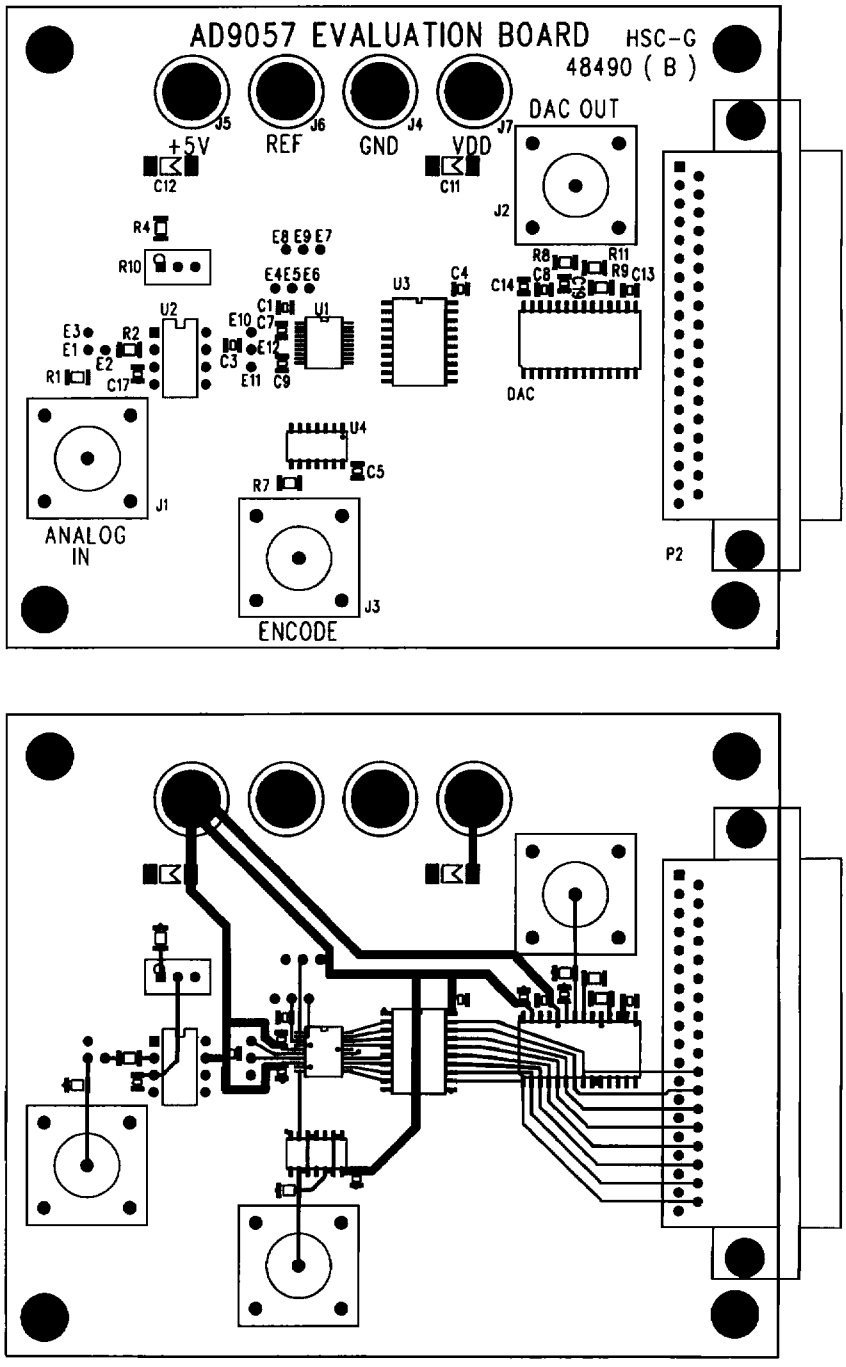
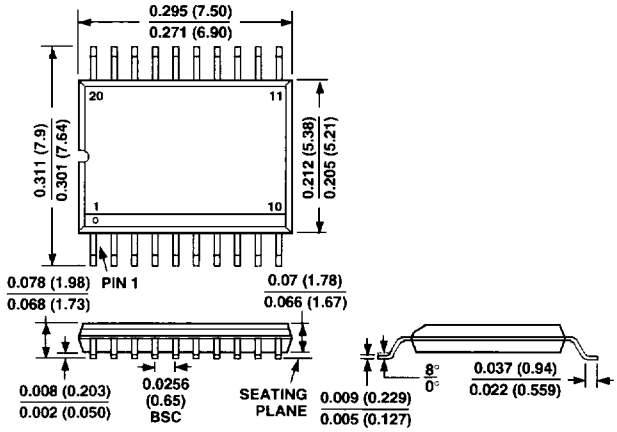


Figure 20. Evaluation Board Layout

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead SSOP
(RS-20)



C2156-10-7/96

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