

Transistors

2.5V Drive Nch+Pch MOSFET

EM6M1

●Structure

Silicon N-channel MOSFET /
Silicon P-channel MOSFET

●Features

- 1) Nch MOSFET and Pch MOSFET are put in EMT6 package.
- 2) High-speed switching.
- 3) Low voltage drive (2.5V drive).
- 4) Built-in G-S Protection Diode.

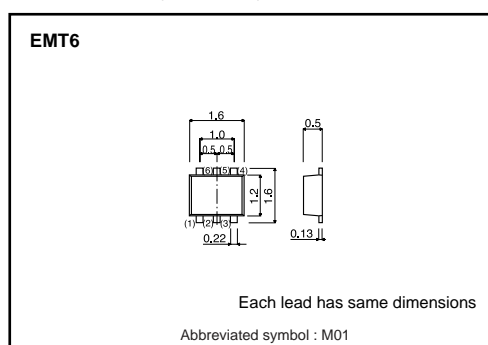
●Applications

Switching

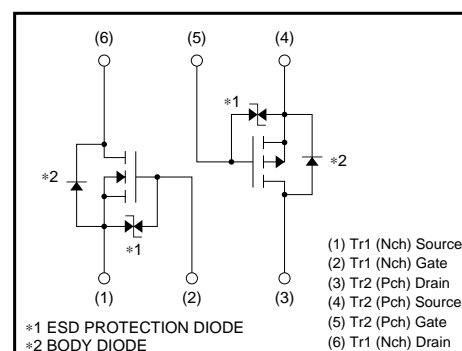
●Packaging specifications

| Type | Package | Taping |
|-------|------------------------------|--------|
| | Code | T2R |
| | Basic ordering unit (pieces) | 8000 |
| EM6M1 | | ○ |

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

| Parameter | Symbol | Limits | | Unit |
|------------------------------|------------|---------------|------------|--------------|
| | | Tr1 : N-ch | Tr2 : P-ch | |
| Drain-source voltage | V_{DSS} | 30 | -20 | V |
| Gate-source voltage | V_{GSS} | ± 20 | ± 12 | V |
| Drain current | Continuous | I_D | ± 0.1 | A |
| | Pulsed | I_{DP}^{*1} | ± 0.4 | A |
| Power dissipation | P_D^{*2} | 150 | | mW / TOTAL |
| | | 120 | | mW / ELEMENT |
| Channel temperature | T_{ch} | 150 | | °C |
| Range of storage temperature | T_{stg} | -55 to +150 | | °C |

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

Transistors

N-ch

●Electrical characteristics (Ta=25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|-----------------------|------|------|------|------|---|
| Gate-source leakage | I _{GSS} | – | – | ±1 | μA | V _{GS} = ±20V, V _{DS} =0V |
| Drain-source breakdown voltage | V _{(BR) DSS} | 30 | – | – | V | I _D =10μA, V _{GS} =0V |
| Zero gate voltage drain current | I _{DSS} | – | – | 1 | μA | V _{DS} =30V, V _{GS} =0V |
| Gate threshold voltage | V _{GS(th)} | 0.8 | – | 1.5 | V | V _{DS} =3V, I _D =100μA |
| Static drain-source on-state resistance | R _{DS(on)} * | – | 5 | 8 | Ω | I _D =10mA, V _{GS} =4V |
| | | – | 7 | 13 | Ω | I _D =1mA, V _{GS} =2.5V |
| Forward transfer admittance | Y _{fs} * | 20 | – | – | mS | V _{DS} =3V, I _D =10mA |
| Input capacitance | C _{iss} | – | 13 | – | pF | V _{DS} =5V |
| Output capacitance | C _{oss} | – | 9 | – | pF | V _{GS} =0V |
| Reverse transfer capacitance | C _{rss} | – | 4 | – | pF | f=1MHz |
| Turn-on delay time | t _{d(on)} * | – | 15 | – | ns | V _{DD} ≐5V |
| Rise time | t _r * | – | 35 | – | ns | I _D =10mA |
| Turn-off delay time | t _{d(off)} * | – | 80 | – | ns | V _{GS} =5V |
| Fall time | t _f * | – | 80 | – | ns | R _L =500Ω |
| Total gate charge | Q _g * | – | 0.9 | – | nC | R _G =10Ω |
| Gate-source charge | Q _{gs} * | – | 0.2 | – | nC | V _{DD} ≐15V, I _D =0.1A |
| Gate-drain charge | Q _{gd} * | – | 0.2 | – | nC | V _{GS} =4.5V |
| | | | | | | R _L =150Ω, R _G =10Ω |

*Pulsed

P-ch

●Electrical characteristics (Ta=25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|-----------------------|------|------|------|------|---|
| Gate-source leakage | I _{GSS} | – | – | ±10 | μA | V _{GS} = ±12V, V _{DS} =0V |
| Drain-source breakdown voltage | V _{(BR) DSS} | –20 | – | – | V | I _D = –1mA, V _{GS} =0V |
| Zero gate voltage drain current | I _{DSS} | – | – | –1 | μA | V _{DS} = –20V, V _{GS} =0V |
| Gate threshold voltage | V _{GS(th)} | –0.7 | – | –2.0 | V | V _{DS} = –10V, I _D = –1mA |
| Static drain-source on-state resistance | R _{DS(on)} * | – | 1.0 | 1.5 | Ω | I _D = –0.2A, V _{GS} = –4.5V |
| | | – | 1.1 | 1.6 | Ω | I _D = –0.2A, V _{GS} = –4V |
| | | – | 2.0 | 3.0 | Ω | I _D = –0.2A, V _{GS} = –2.5V |
| Forward transfer admittance | Y _{fs} * | 0.2 | – | – | S | V _{DS} = –10V, I _D = –0.15A |
| Input capacitance | C _{iss} | – | 50 | – | pF | V _{DS} = –10V |
| Output capacitance | C _{oss} | – | 5 | – | pF | V _{GS} = 0V |
| Reverse transfer capacitance | C _{rss} | – | 5 | – | pF | f=1MHz |
| Turn-on delay time | t _{d(on)} * | – | 9 | – | ns | V _{DD} ≐ –15V |
| Rise time | t _r * | – | 6 | – | ns | I _D = –0.15A |
| Turn-off delay time | t _{d(off)} * | – | 35 | – | ns | V _{GS} = –4.5V |
| Fall time | t _f * | – | 45 | – | ns | R _L = 100Ω |
| Total gate charge | Q _g * | – | 1.2 | – | nC | R _G = 10Ω |
| Gate-source charge | Q _{gs} * | – | 0.2 | – | nC | V _{DD} ≐ –15V, I _D = –0.2A |
| Gate-drain charge | Q _{gd} * | – | 0.2 | – | nC | V _{GS} = –4.5V |
| | | | | | | R _L = 75Ω, R _G = 10Ω |

*Pulsed

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●Electrical characteristic curve

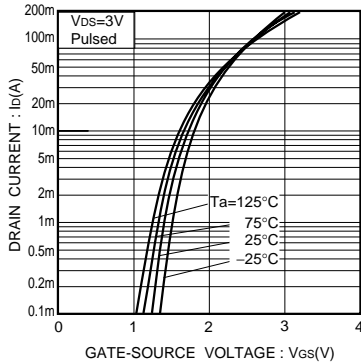


Fig.1 Typical Transfer Characteristics

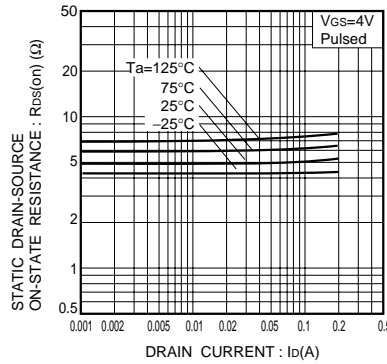


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (I)

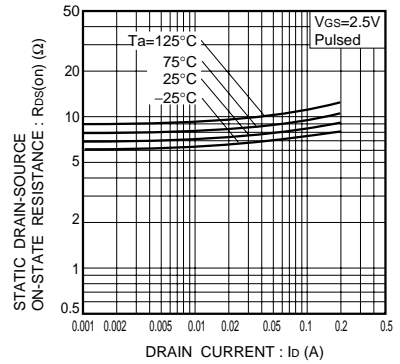


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (II)

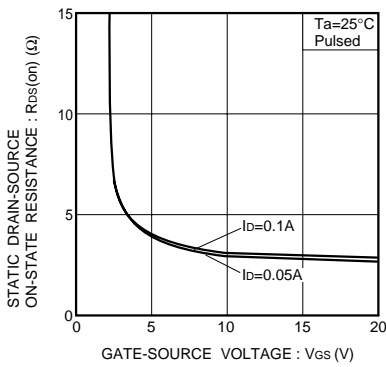


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

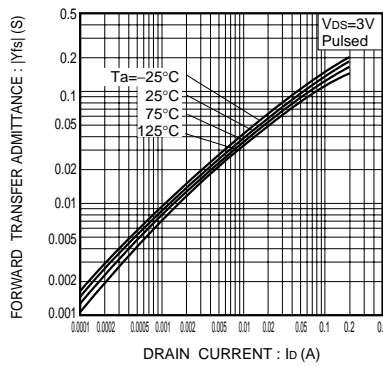


Fig.5 Forward Transfer Admittance vs. Drain Current

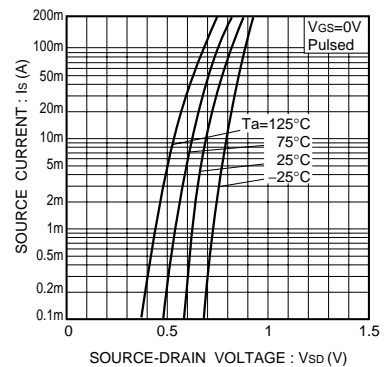


Fig.6 Reverse Drain Current vs. Source-Drain Voltage (I)

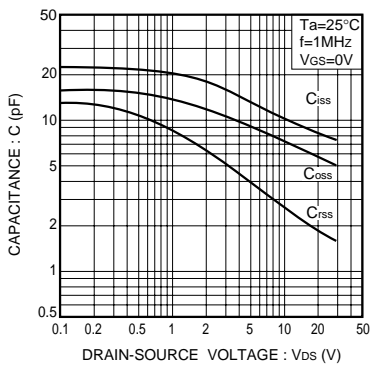


Fig.7 Typical Capacitance vs. Drain-Source Voltage

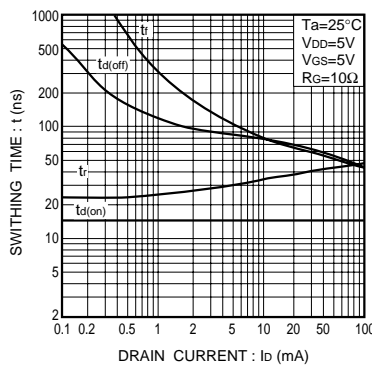


Fig.8 Switching Characteristics

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●Electrical characteristic curve

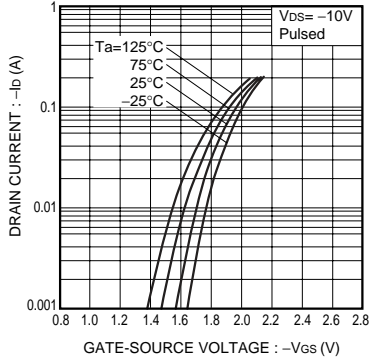


Fig.1 Typical Transfer Characteristics

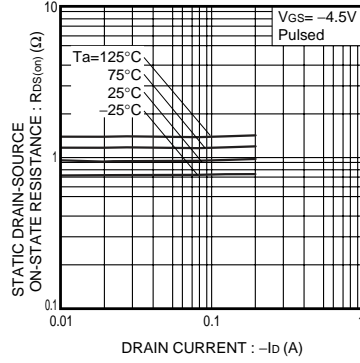


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (I)

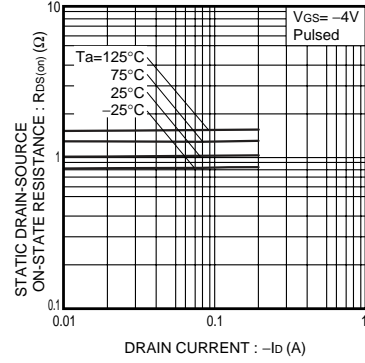


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (II)

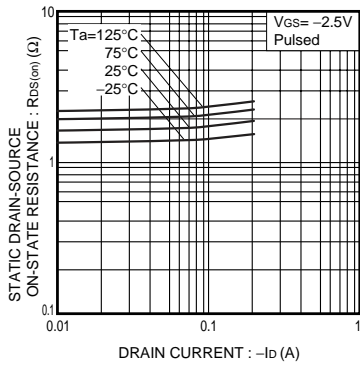


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (III)

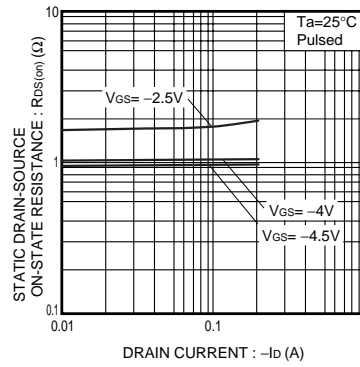


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (IV)

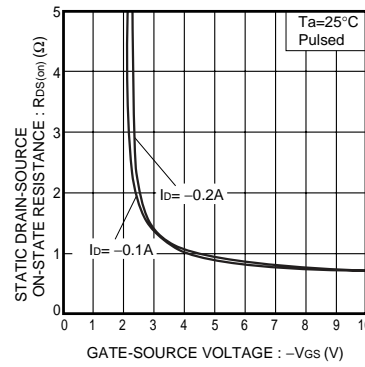


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

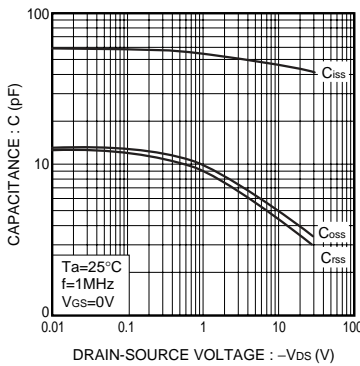


Fig.7 Typical Capacitance vs. Drain-Source Voltage

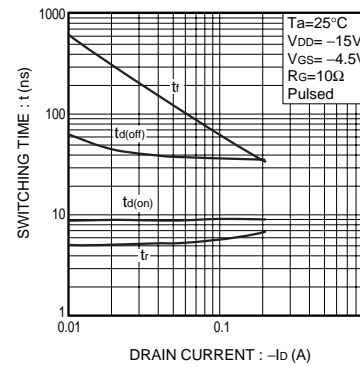


Fig.8 Switching Characteristics

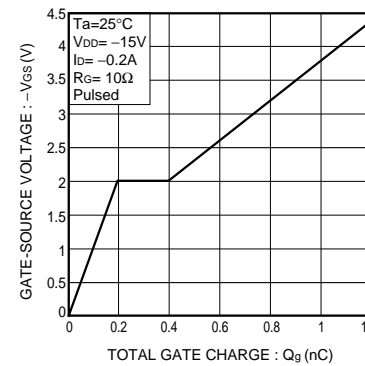


Fig.9 Dynamic Input Characteristics

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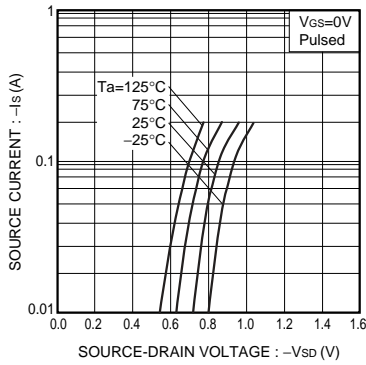


Fig.10 Source Current vs. Source-Drain Voltage

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●Measurement circuit

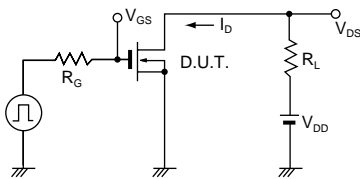


Fig.9 Switching Time Test Circuit

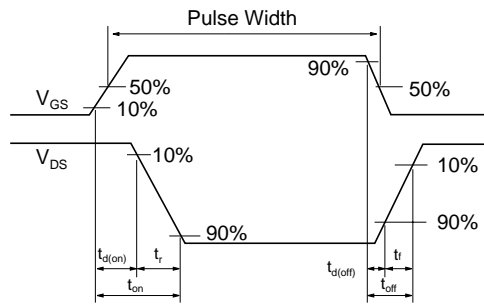


Fig.10 Switching Time Waveforms

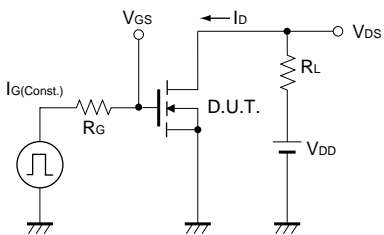


Fig.11 Gate Charge Measurement Circuit

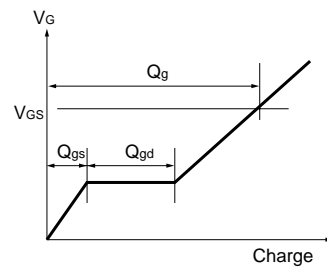


Fig.12 Gate Charge Waveform

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● Measurement circuit

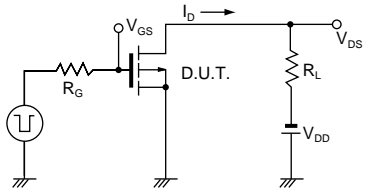


Fig.11 Switching Time Test Circuit

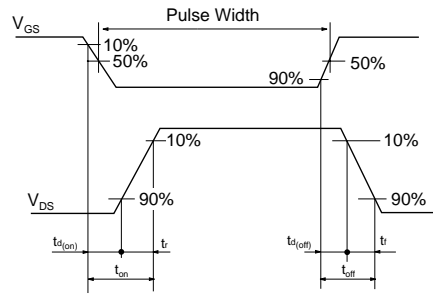


Fig.12 Switching Time Waveforms

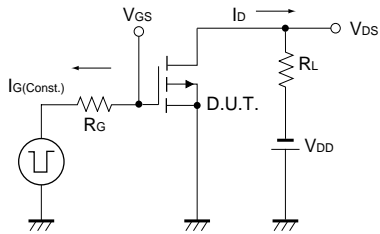


Fig.13 Gate Charge Measurement Circuit

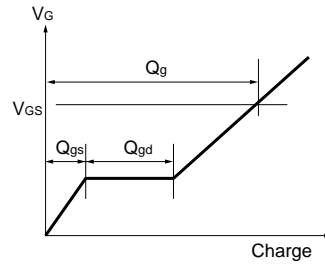


Fig.14 Gate Charge Waveform

Notes

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