

# BLF2043F

UHF power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

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Ampleon

# UHF power LDMOS transistor

# BLF2043F

### FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 2.2 GHz).

### APPLICATIONS

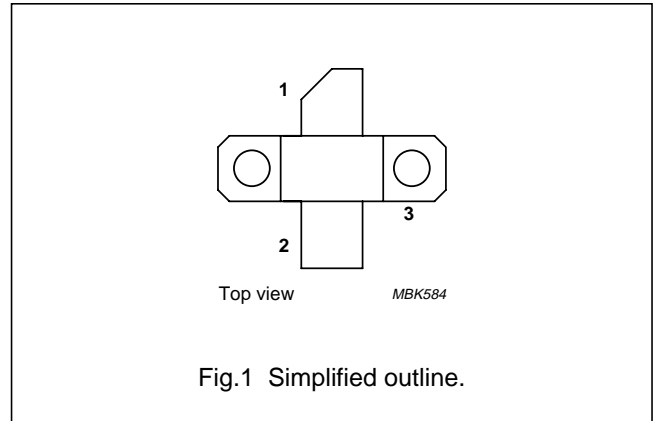
- Communication transmitter applications in the UHF frequency range.

### DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT467C) with a ceramic cap. The common source is connected to the mounting flange.

### PINNING - SOT467C

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange



### QUICK REFERENCE DATA

RF performance at  $T_h = 25\text{ °C}$  in a common source test circuit.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$P_L$ (W)	$G_p$ (dB)	$\eta_D$ (%)	$d_{im}$ (dBc)
CW, class-AB (2-tone)	$f_1 = 2200; f_2 = 2200.1$	26	10 (PEP)	>11	>30	$\leq -26$

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage	–	65	V
$V_{GS}$	gate-source voltage	–	$\pm 15$	V
$I_D$	drain current (DC)	–	2.2	A
$T_{stg}$	storage temperature	–65	+150	°C
$T_j$	junction temperature	–	200	°C

### CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25\ ^\circ\text{C}$ ; note 1	5	K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink		0.5	K/W

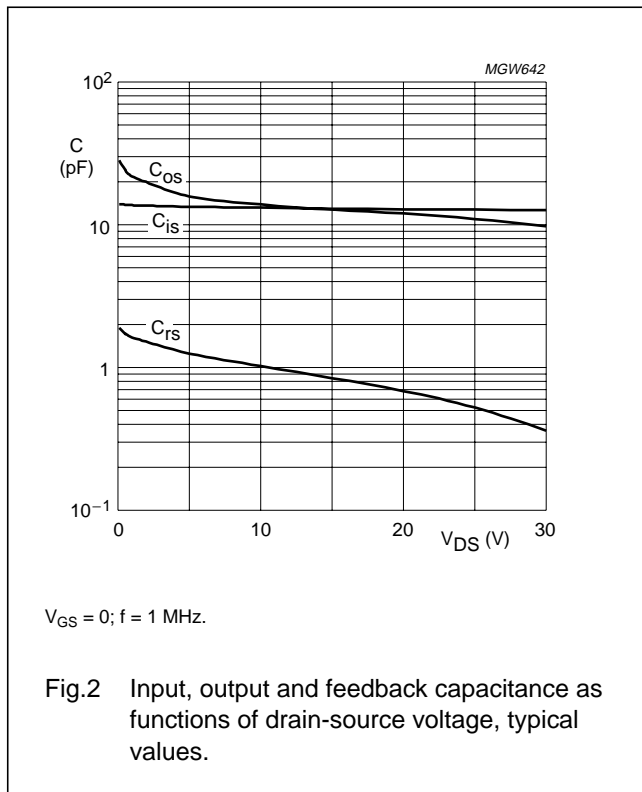
**Note**

1. Thermal resistance is determined under RF operating conditions.

**CHARACTERISTICS**

$T_j = 25\ ^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$ ; $I_D = 0.2\ \text{mA}$	75	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = 10\ \text{V}$ ; $I_D = 20\ \text{mA}$	4	–	5	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0$ ; $V_{DS} = 26\ \text{V}$	–	–	1.5	$\mu\text{A}$
$I_{DSX}$	on-state drain current	$V_{GS} = V_{GSth} + 9\ \text{V}$ ; $V_{DS} = 10\ \text{V}$	2.8	–	–	A
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 15\ \text{V}$ ; $V_{DS} = 0$	–	–	40	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\ \text{V}$ ; $I_D = 0.75\ \text{A}$	–	0.5	–	S
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$ ; $I_D = 0.75\ \text{A}$	–	1.2	–	$\Omega$
$C_{is}$	input capacitance	$V_{GS} = 0$ ; $V_{DS} = 26\ \text{V}$ ; $f = 1\ \text{MHz}$	–	13	–	pF
$C_{os}$	output capacitance	$V_{GS} = 0$ ; $V_{DS} = 26\ \text{V}$ ; $f = 1\ \text{MHz}$	–	11	–	pF
$C_{rs}$	feedback capacitance	$V_{GS} = 0$ ; $V_{DS} = 26\ \text{V}$ ; $f = 1\ \text{MHz}$	–	0.5	–	pF



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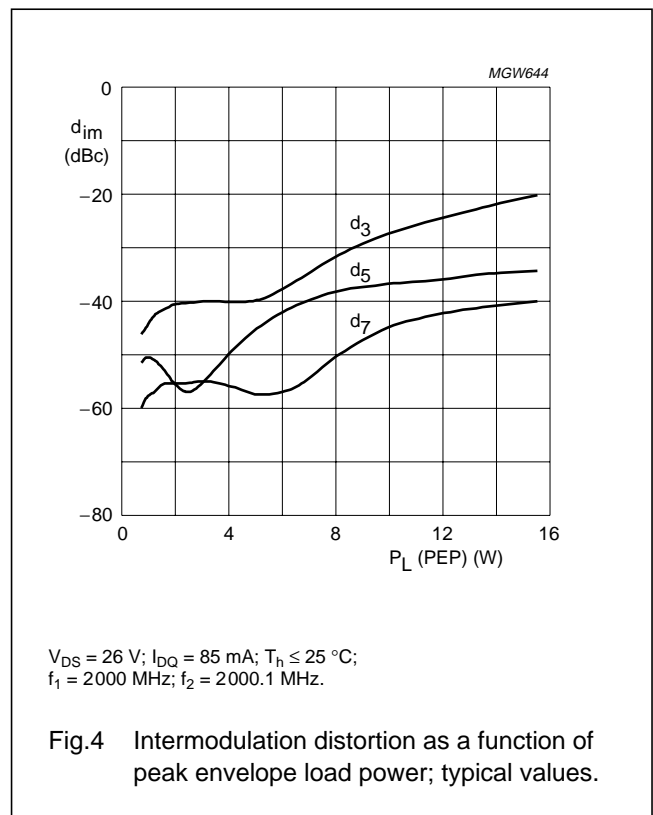
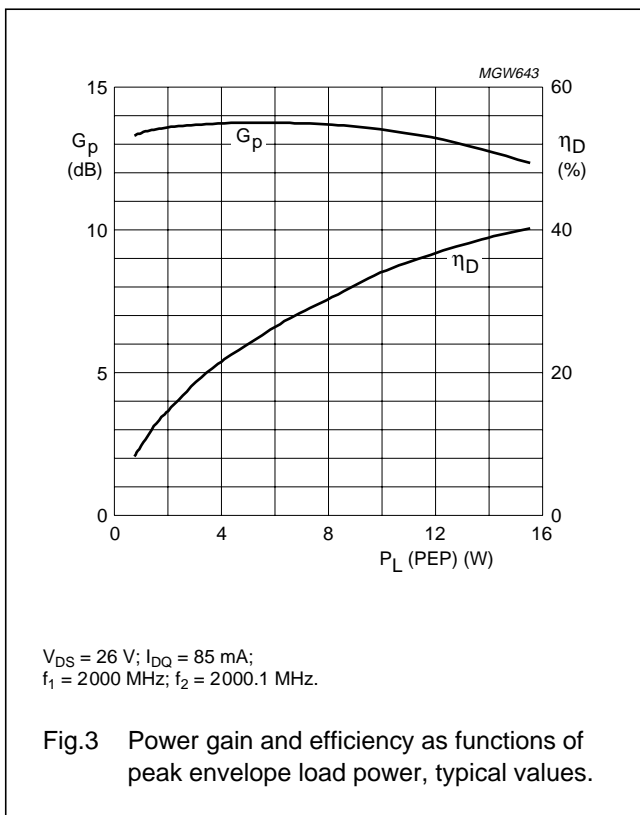
APPLICATION INFORMATION

RF performance in a common source class-AB circuit.  $T_h = 25\text{ }^\circ\text{C}$ ;  $R_{th\text{ mb-h}} = 0.4\text{ K/W}$ ; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	I <sub>DQ</sub> (mA)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	d <sub>im</sub> (dBc)
CW, class-AB (2-tone)	f <sub>1</sub> = 2200; f <sub>2</sub> = 2200.1	26	85	10 (PEP)	>11	>30	≤-26

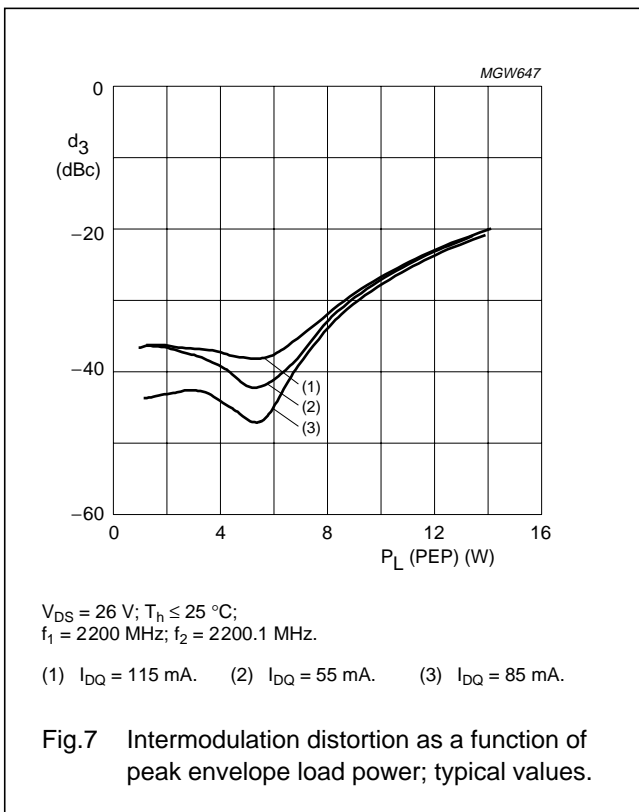
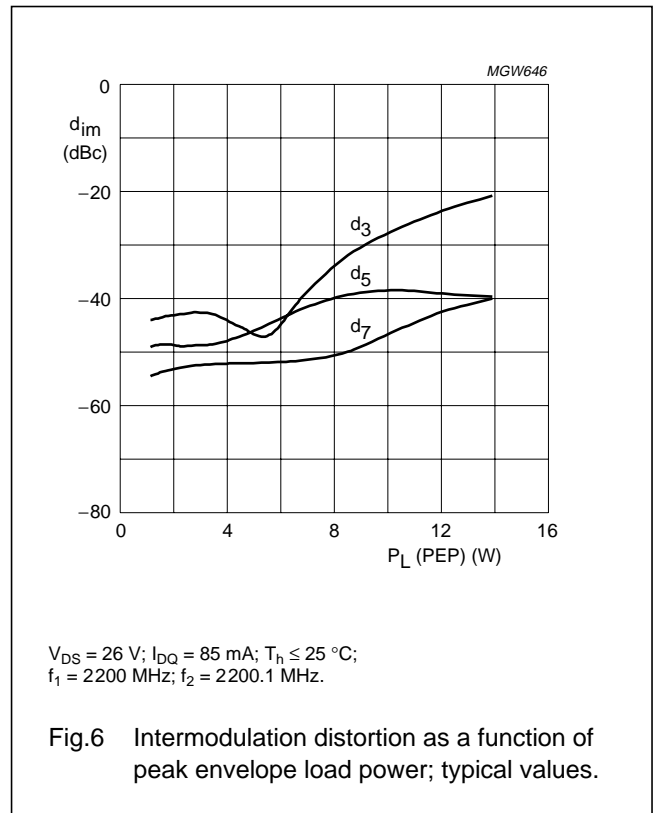
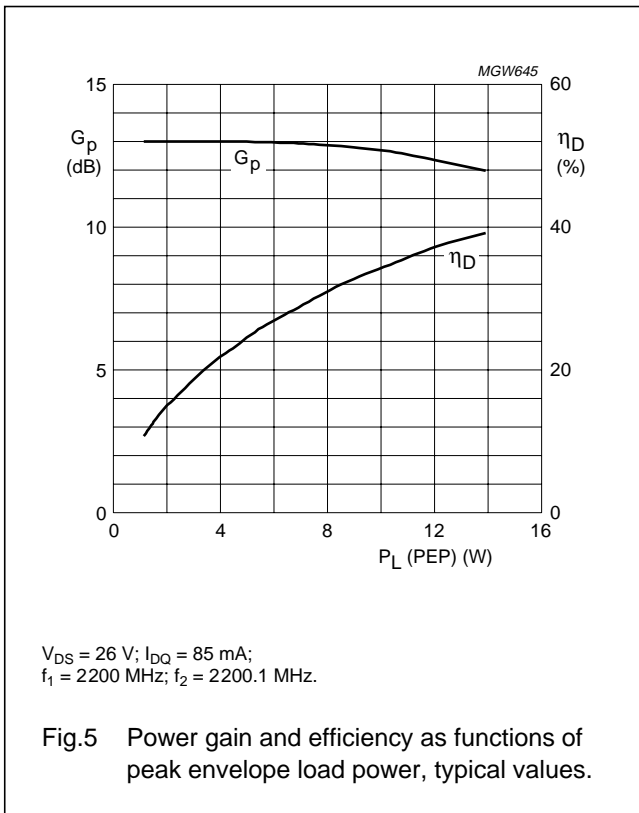
Ruggedness in class-AB operation

The BLF2043F is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V<sub>DS</sub> = 26 V; f = 2200 MHz at rated load power.



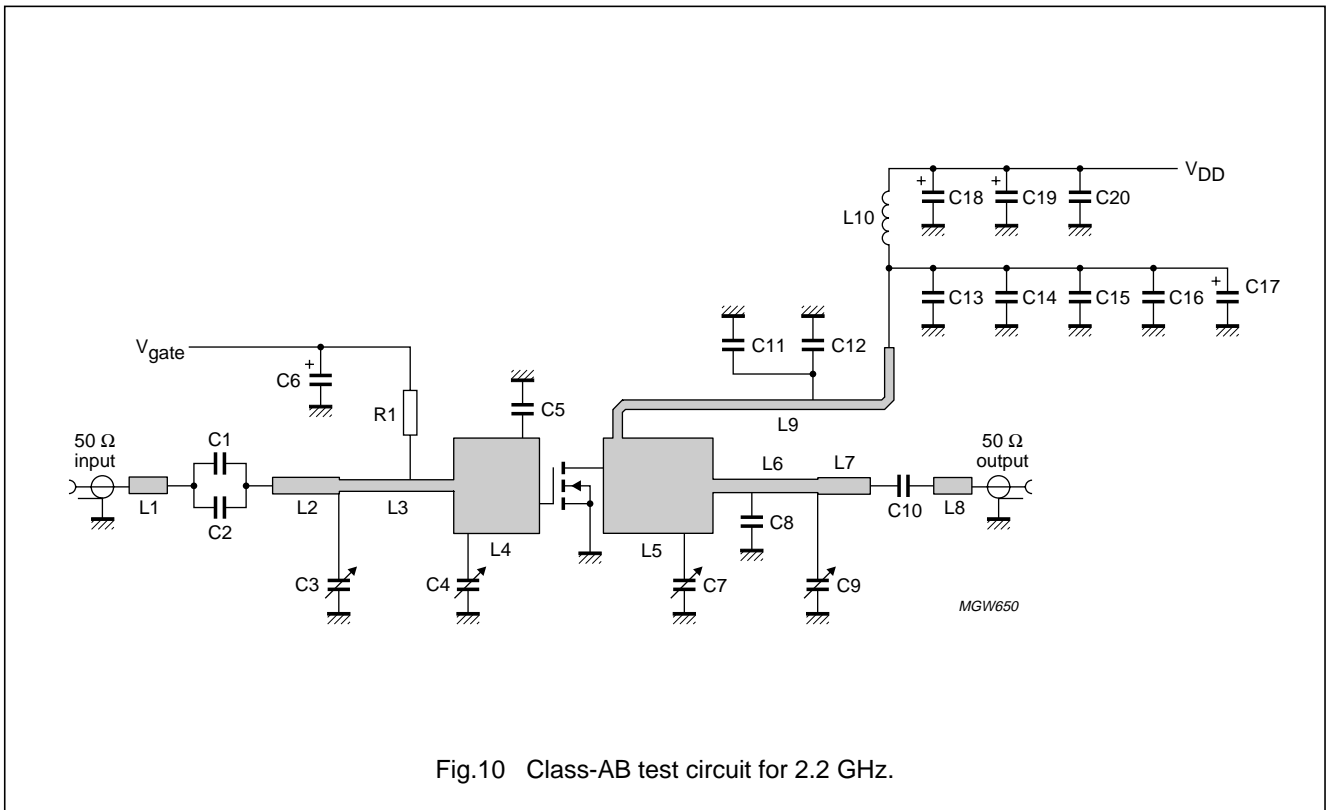
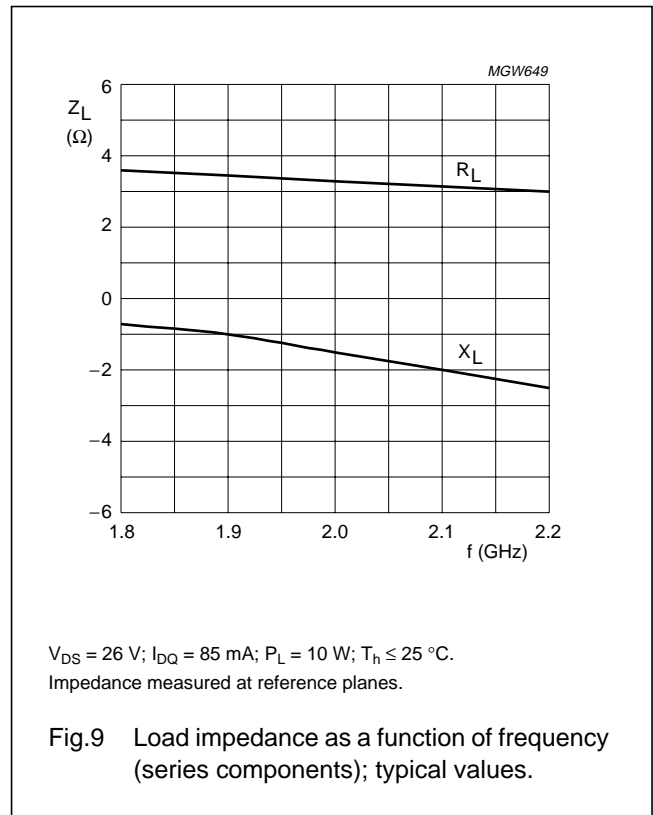
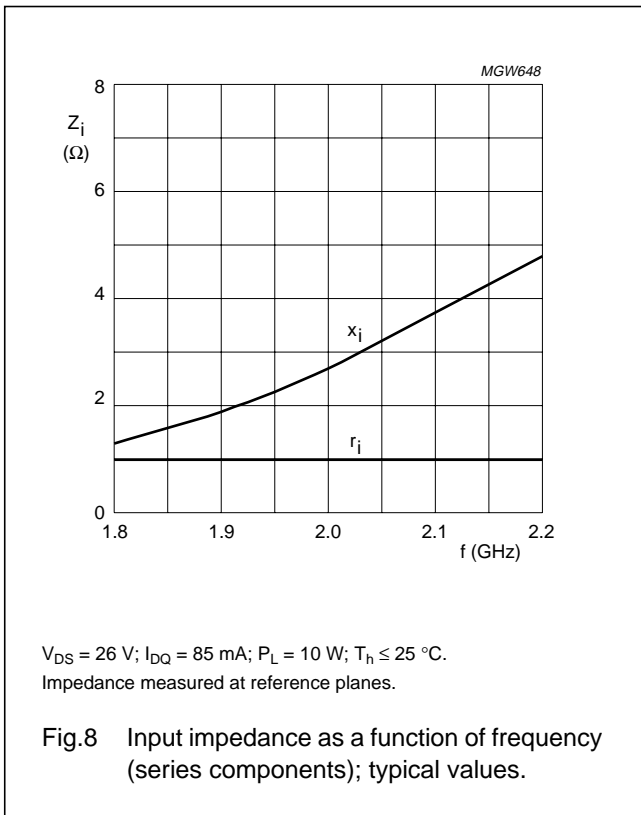
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## UHF power LDMOS transistor

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## List of components (see Figs 10 and 11)

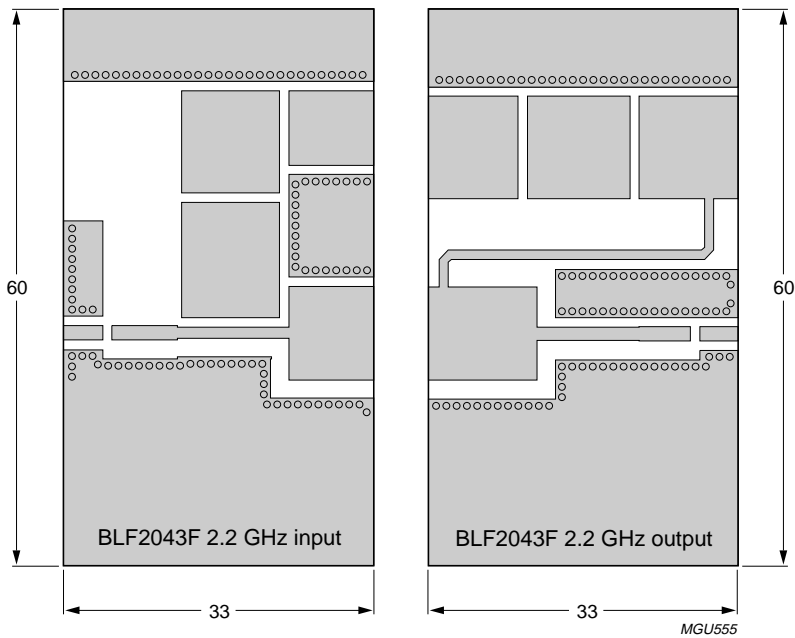
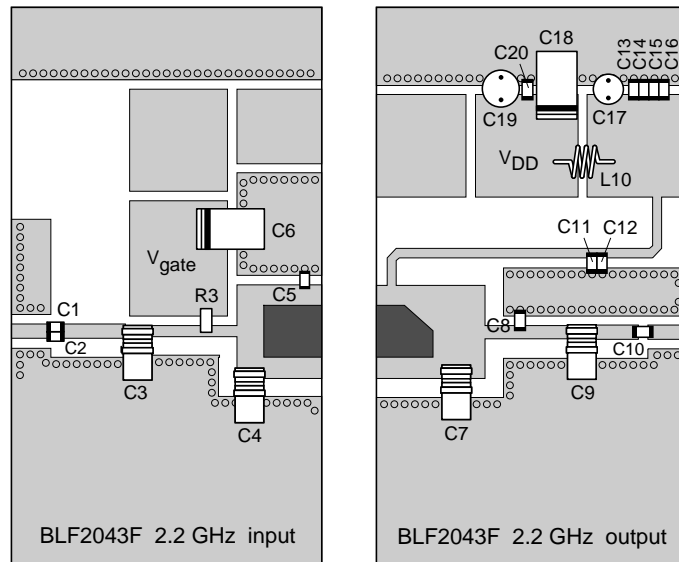
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C10, C11	multilayer ceramic chip capacitor; note 1	6.8 pF		
C3, C4, C7, C9	Tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C5	multilayer ceramic chip capacitor; note 1	2.4 pF		
C6, C18	tantalum SMD capacitor	10 $\mu$ F; 35 V		
C8	multilayer ceramic chip capacitor; note 1	1.5 pF		
C12, C20	multilayer ceramic chip capacitor; note 2	1 nF		
C13	multilayer ceramic chip capacitor; note 1	10 pF		
C14	multilayer ceramic chip capacitor; note 1	51 pF		
C15	multilayer ceramic chip capacitor; note 1	120 pF		
C16	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C17	electrolytic capacitor	47 $\mu$ F; 35 V		2222 036 90094
C19	electrolytic capacitor	100 $\mu$ F; 63 V		2222 037 58101
L1, L8	stripline; note 3	50 $\Omega$	4 $\times$ 1.5 mm	
L2	stripline; note 3	50 $\Omega$	7 $\times$ 1.5 mm	
L3	stripline; note 3	58.1 $\Omega$	12 $\times$ 1.2 mm	
L4	stripline; note 3	11.3 $\Omega$	9 $\times$ 10 mm	
L5	stripline; note 3	11.3 $\Omega$	11.5 $\times$ 10 mm	
L6	stripline; note 3	52.8 $\Omega$	11 $\times$ 1.4 mm	
L7	stripline; note 3	50 $\Omega$	5.5 $\times$ 1.5 mm	
L9	stripline; note 3	64.7 $\Omega$	38 $\times$ 1 mm	
L10	2 turns enamelled 0.5 mm copper wire		int. dia. = 3 mm; length = 3 mm	
R1	metal film resistor	390 $\Omega$ ; 0.6 W		2322 156 11009

## Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Rogers 5880 dielectric ( $\epsilon_r = 2.2$ ); thickness 0.51 mm.

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Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ( $\epsilon_r = 2.2$ ), thickness 0.51 mm. The other side is unetched and serves as a ground plane.

Fig.11 Component layout for 2.2 GHz class-AB test circuit.



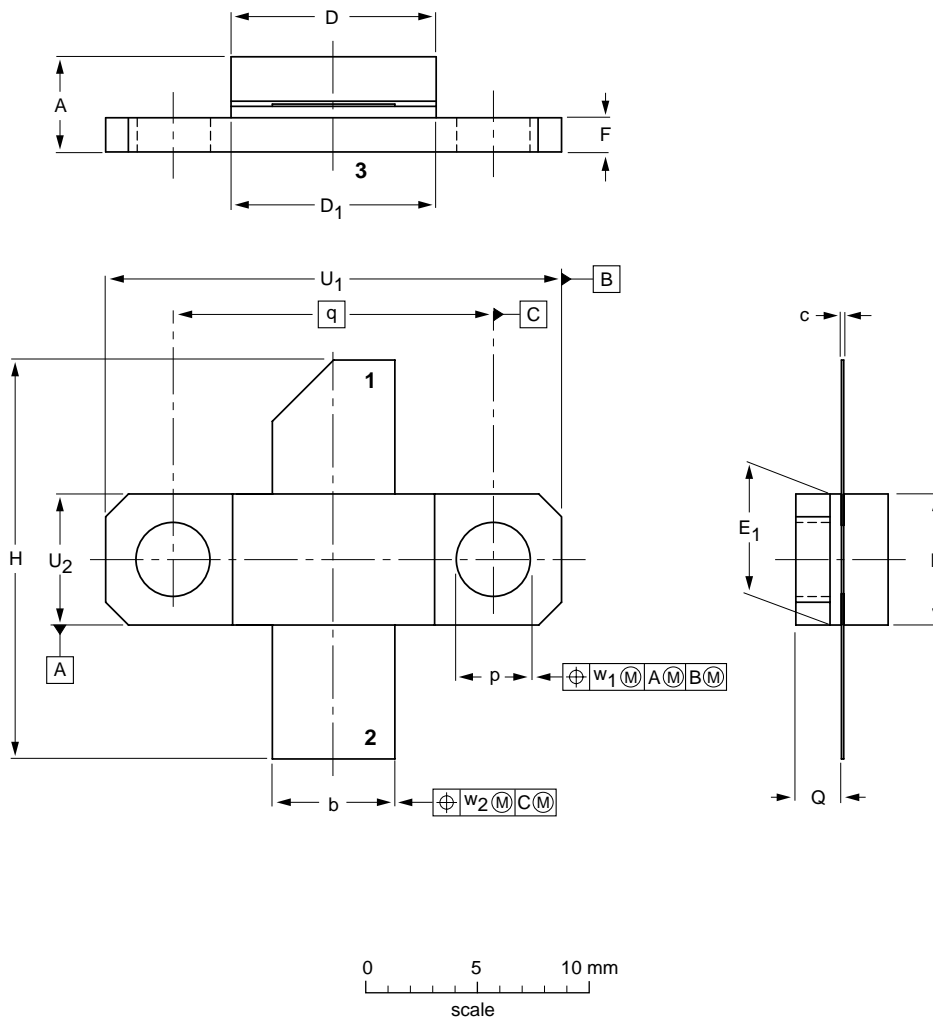
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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT467C



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						99-12-06 99-12-28

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## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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