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MOSFET - Power, Single N-Channel, Shielded Gate, PowerTrench®

150 V, 22 mΩ, 37.2 A

NTTFS022N15MC

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Features

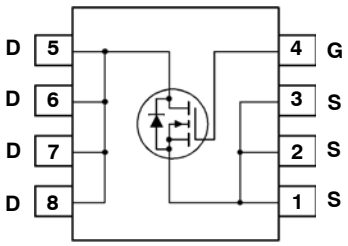
- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

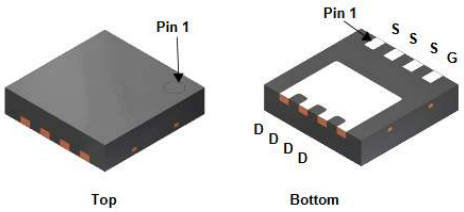
Typical Applications

- Primary DC−DC MOSFET
- Synchronous Rectifier in DC−DC and AC−DC
- Motor Drive
- Capable of 175°C Tj Max Rating

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
150 V	22 mΩ @ 10 V	37.2 A

N−CHANNEL MOSFET





WDFN8
CASE 483AW

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	150	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 5)	Steady State	T_C = 25°C	I_D	37.2	A
Power Dissipation $R_{\theta JC}$ (Note 5)		T_C = 25°C	P_D	71.4	W
Continuous Drain Current (Notes 1, 5)		T_A = 25°C	I_D	7.4	A
Power Dissipation (Notes 1, 5)		T_A = 25°C	P_D	2.8	W
Power Dissipation (Notes 2, 5)		T_A = 25°C	P_D	1.2	W
Pulsed Drain Current (Note 3)		T_C = 25°C	I_{DM}	158	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 8 A) (Note 4)			E_{AS}	96	mJ
Maximum Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR−4 board using 1 in^2 pad of 2 oz copper.
2. Surface mounted on a FR−4 board using the minimum recommended pad of 2 oz copper.
3. Pulsed ID please refer to Figure 12 SOA graph for more details
4. E_{AS} of 96 mJ is based on starting T_J = 25°C; L = 3 mH, I_{AS} = 8 A, V_{DD} = 150 V, V_{GS} = 10 V.
5. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

MARKING DIAGRAM

22MC = Specific Device Code
&Z = Assembly Location
&3 = 3−Digit Date Code
&K = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS022N15MC	WDFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance Junction−to−Case − Steady State (Note 5)	$R_{\theta JC}$	2.1	°C/W
Thermal Resistance Junction−to−Ambient − Steady State (Notes 1, 5)	$R_{\theta JA}$	53	°C/W
Thermal Resistance Junction−to−Ambient − Steady State (Notes 2, 5)	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	150			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, referenced to 25°C		75		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V, T_J = 25°C			1	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 100 μA	2.5		4.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 100 μA, referenced to 25°C		−8.4		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 18 A		17.1	22	mΩ
		V_{GS} = 8 V, I_D = 9 A		19	25.3	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 18 A		37		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz V_{DS} = 75 V		1315		pF
Output Capacitance	C_{OSS}			380		
Reverse Transfer Capacitance	C_{RSS}			6		
Gate−Resistance	R_G			0.6	1.2	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 75 V, I_D = 18 A		17		nC
Threshold Gate Charge	$Q_{G(TH)}$			4.4		
Gate−to−Source Charge	Q_{GS}			7.2		
Gate−to−Drain Charge	Q_{GD}			2.7		
Plateau Voltage	V_{GP}			5.6		V
Output Charge	Q_{OSS}	V_{GS} = 0 V, V_{DD} = 75 V		41		nC
RESISTIVE SWITCHING CHARACTERISTICS (Note 6)						
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 75 V, I_D = 18 A, R_G = 6 Ω		14		ns
Rise Time	t_r			2.8		
Turn−Off Delay Time	$t_{d(off)}$			17		
Fall Time	t_f			2.9		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 18 A, T_J = 25°C		0.86	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V dI_S/dt = 300 A/μs, I_S = 18 A		45		ns
Reverse Recovery Charge	Q_{RR}			155		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 75 V dI_S/dt = 1000 A/μs, I_S = 18 A		28		ns
Reverse Recovery Charge	Q_{RR}			242		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Switching characteristics are independent of operating junction temperature

TYPICAL CHARACTERISTICS

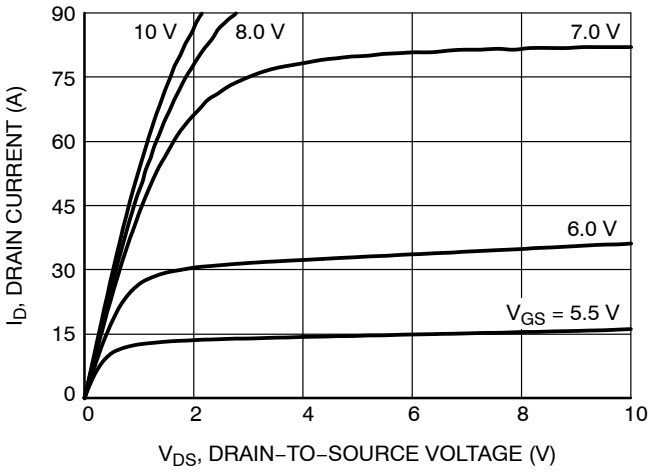


Figure 1. On−Region Characteristics

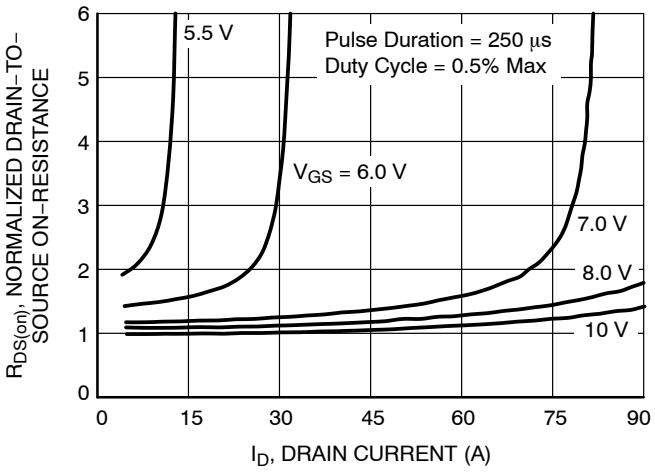


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

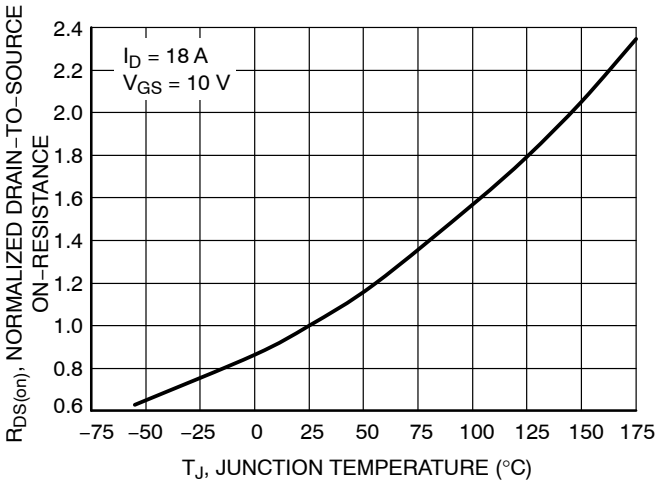


Figure 3. Normalized On−Resistance vs. Junction Temperature

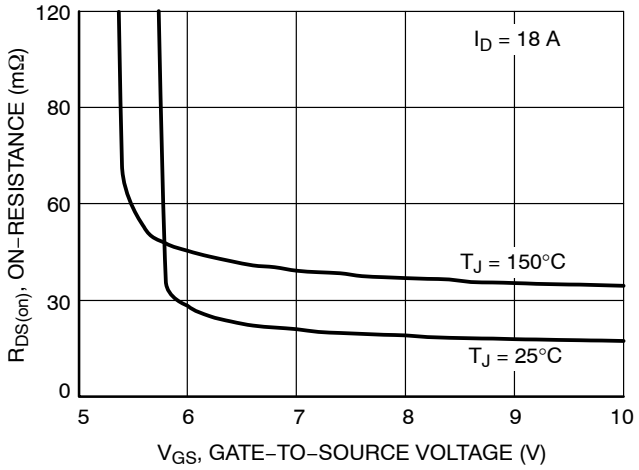


Figure 4. On−Resistance vs. Gate−to−Source Voltage

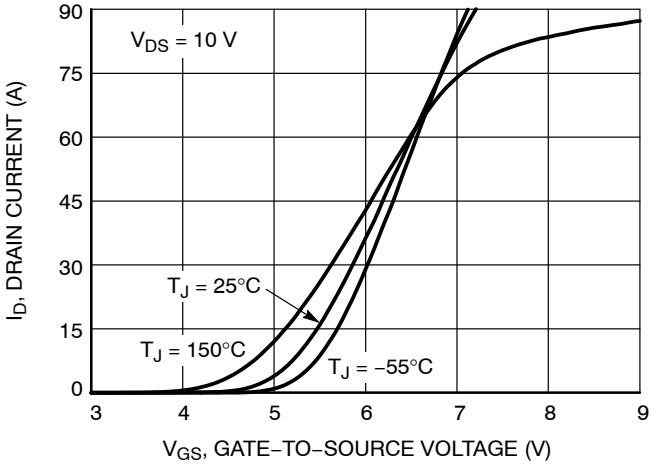


Figure 5. Transfer Characteristics

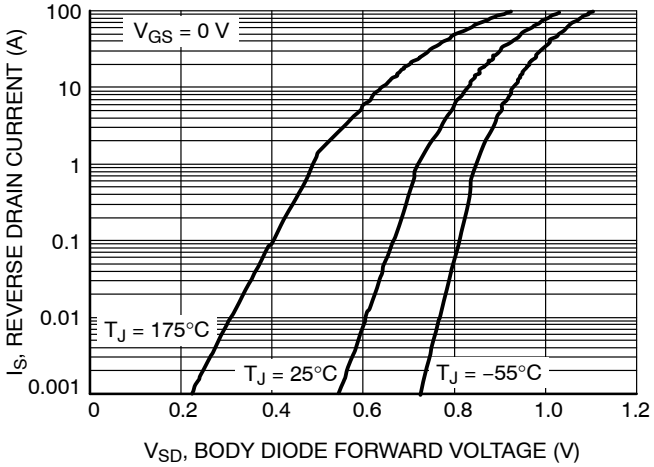


Figure 6. Source−to−Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

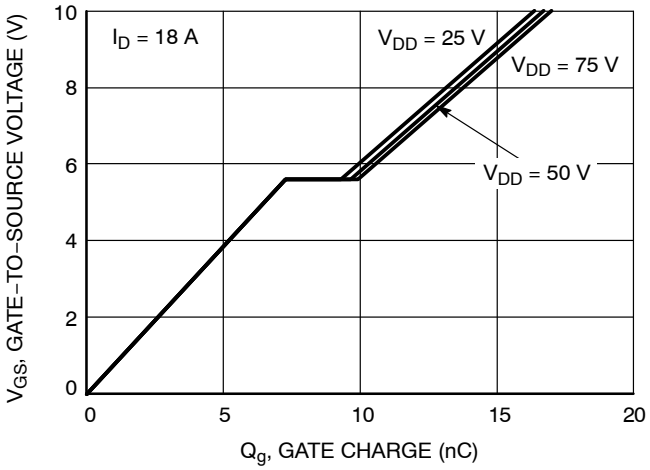


Figure 7. Gate Charge Characteristics

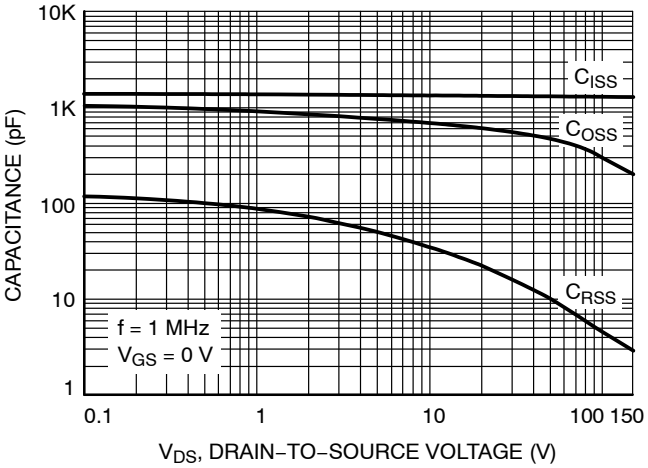


Figure 8. Capacitance vs. Drain−to−Source Voltage

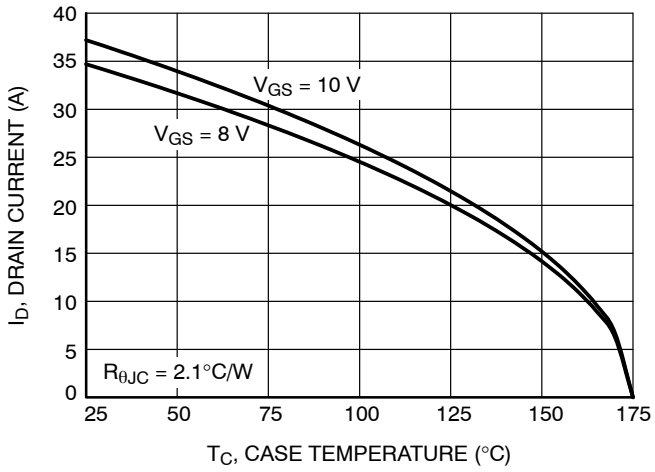


Figure 9. Drain Current vs. Case Temperature

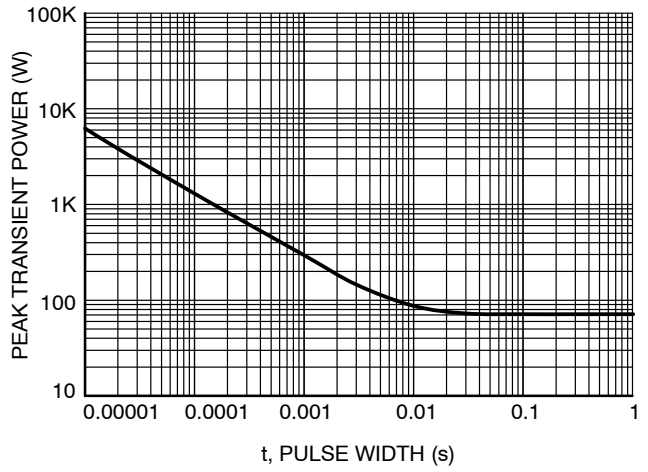


Figure 10. Peak Power

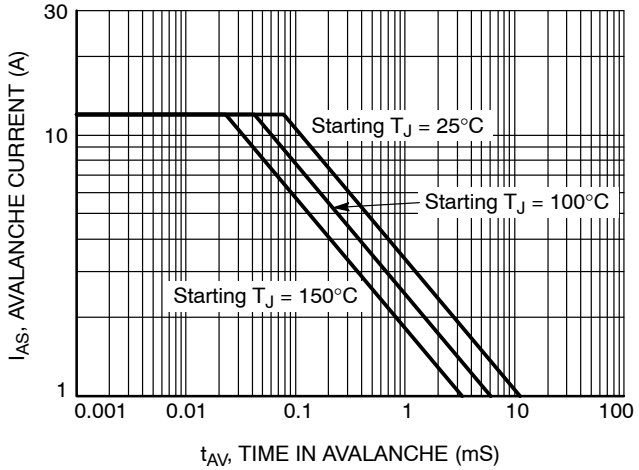


Figure 11. Unclamped Inductive Switching Capability

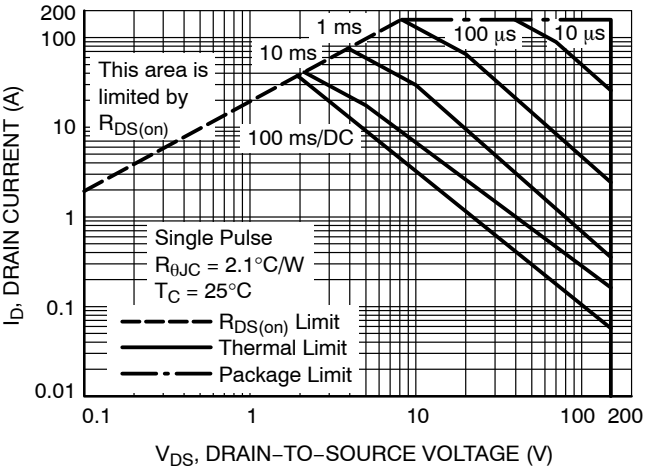


Figure 12. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS

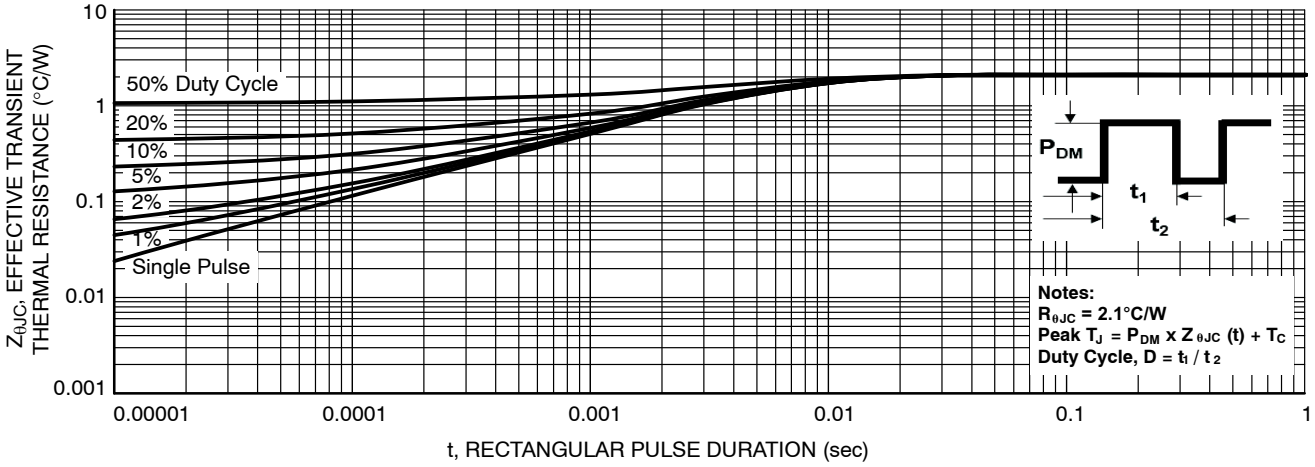
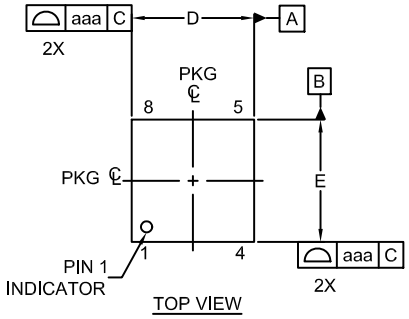


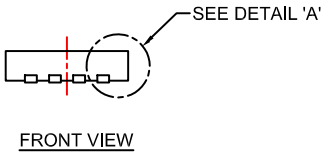
Figure 13. Transient Thermal Impedance

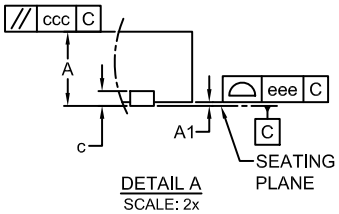
NTTFS022N15MC

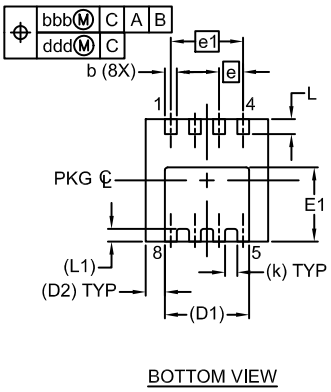
PACKAGE DIMENSIONS

WDFN8 3.3X3.3, 0.65P
CASE 483AW
ISSUE A

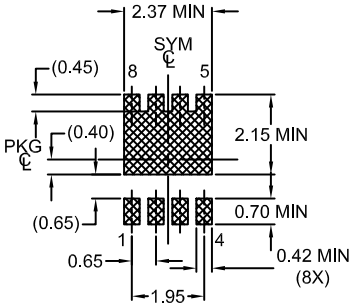








LAND PATTERN RECOMMENDATION*



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

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