

MM54HC257/MM74HC257



T-67-21-51

# MM54HC257/MM74HC257 Quad 2-Channel TRI-STATE® Multiplexer

## General Description

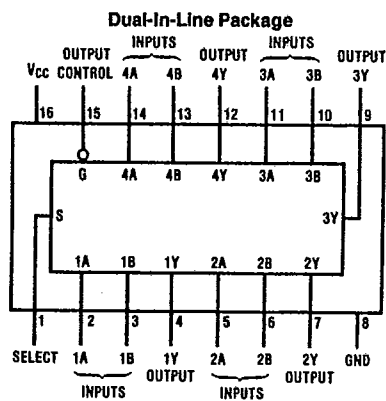
This QUAD 2-TO-1 line data selector/multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive up to 15 LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make this device ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, the SELECT input chooses whether the A or B input is used.

The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

## Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V-6V
- Low quiescent current: 80 μA maximum (74HC Series)
- TRI-STATE outputs for connection to system buses.

## Connection and Logic Diagrams

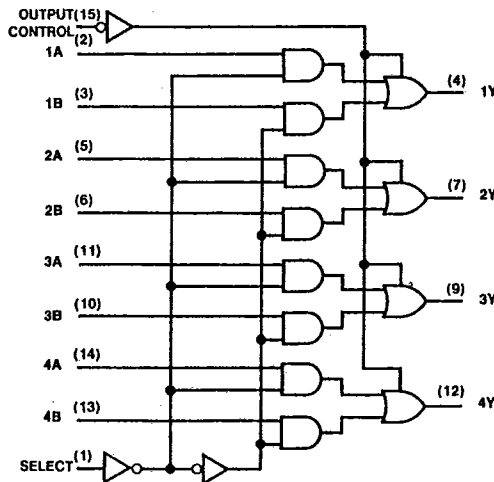


TL/F/5329-1

Top View

Order Number MM54HC257\* or MM74HC257\*

\*Please look into Section 8, Appendix D for availability of various package types.



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## Truth Table

Output Control	Inputs		Output Y
	Select	A B	
H	X	X X	Z
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

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**Absolute Maximum Ratings** (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V <sub>CC</sub> )	-0.5 to +7.0V
DC Input Voltage (V <sub>IN</sub> )	-1.5 to V <sub>CC</sub> +1.5V
DC Output Voltage (V <sub>OUT</sub> )	-0.5 to V <sub>CC</sub> +0.5V
Clamp Diode Current (I <sub>IK</sub> , I <sub>OK</sub> )	±20 mA
DC Output Current, per pin (I <sub>OUT</sub> )	±35 mA
DC V <sub>CC</sub> or GND Current, per pin (I <sub>CC</sub> )	±70 mA
Storage Temperature Range (T <sub>STG</sub> )	-65°C to +150°C
Power Dissipation (P <sub>D</sub> )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T <sub>L</sub> ) (Soldering 10 seconds)	260°C

**Operating Conditions**

	Min	Max	Units
Supply Voltage (V <sub>CC</sub> )	2	6	V
DC Input or Output Voltage (V <sub>IN</sub> , V <sub>OUT</sub> )	0	V <sub>CC</sub>	V
Operating Temp. Range (T <sub>A</sub> )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t <sub>r</sub> , t <sub>f</sub> )			
V <sub>CC</sub> =2.0V		1000	ns
V <sub>CC</sub> =4.5V		500	ns
V <sub>CC</sub> =6.0V		400	ns

**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = 25°C			74HC	54HC	Units
				Typ	Guaranteed Limits		T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	
V <sub>IH</sub>	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V	
			4.5V		3.15	3.15	3.15	V	
			6.0V		4.2	4.2	4.2	V	
V <sub>IL</sub>	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V	
			4.5V		1.35	1.35	1.35	V	
			6.0V		1.8	1.8	1.8	V	
V <sub>OH</sub>	Minimum High Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	5.9	V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5V	4.2	3.98	3.84	3.7	V	
			6.0V	5.7	5.48	5.34	5.2	V	
V <sub>OL</sub>	Maximum Low Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V	
			4.5V	0	0.1	0.1	0.1	V	
			6.0V	0	0.1	0.1	0.1	V	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5V	0.2	0.26	0.33	0.4	V	
			6.0V	0.2	0.26	0.33	0.4	V	
I <sub>IN</sub>	Maximum Input Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0V		±0.1	±1.0	±1.0	μA	
I <sub>OZ</sub>	Maximum TRI-STATE Output Leakage	V <sub>OUT</sub> = V <sub>CC</sub> or GND OC = V <sub>IH</sub>	6.0V		±0.5	±5.0	±10	μA	
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0V		8.0	80	160	μA	

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V<sub>OH</sub> and V<sub>OL</sub>) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub> = 5.5V and 4.5V respectively. (The V<sub>IH</sub> value at 5.5V is 3.85V.) The worst case leakage current (I<sub>IN</sub>, I<sub>CC</sub>, and I<sub>OZ</sub>) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\*V<sub>IL</sub> limits are currently tested at 20% of V<sub>CC</sub>. The above V<sub>IL</sub> specification (30% of V<sub>CC</sub>) will be implemented no later than Q1, CY'89.

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**AC Electrical Characteristics**  $V_{CC}=5V, T_A=25^{\circ}C, t_r=t_f=6\text{ ns}$

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Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Select to any Y Output	$C_L = 45\text{ pF}$	12	18	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, A or B to any Y Output	$C_L = 50\text{ pF}$	13	21	ns
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L = 1\text{ k}\Omega$ $C_L = 45\text{ pF}$	17	28	ns
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L = 1\text{ k}\Omega$ $C_L = 5\text{ pF}$	15	25	ns

**AC Electrical Characteristics**  $V_{CC}=2.0V\text{ to }6.0V, C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^{\circ}C$		74HC $T_A = -40\text{ to }85^{\circ}C$		54HC $T_A = -55\text{ to }125^{\circ}C$		Units
				Typ	Guaranteed Limits					
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Select to any Y Output	$C_L = 50\text{ pF}$	2.0V	50	100	125		150		ns
			2.0V	70	150	189		224		ns
		$C_L = 150\text{ pF}$	4.5V	10	20	25		30		ns
			4.5V	15	30	38		45		ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, A or B to any Y Output	$C_L = 50\text{ pF}$	6.0V	9	17	21		25		ns
			6.0V	13	26	32		38		ns
		$C_L = 150\text{ pF}$	2.0V	50	100	125		150		ns
			2.0V	70	150	190		221		ns
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L = 1\text{ k}\Omega$	2.0V	75	150	189		224		ns
				100	200	252		298		ns
		$C_L = 50\text{ pF}$	4.5V	15	30	38		45		ns
			4.5V	20	40	50		60		ns
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L = 1\text{ k}\Omega$	2.0V	75	150	189		224		ns
				15	30	38		45		ns
		$C_L = 50\text{ pF}$	4.5V	13	26	32		38		ns
			6.0V	17	34	43		51		ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time	$C_L = 50\text{ pF}$	2.0V	60		75		90		ns
			4.5V	12		15		18		ns
			6.0V	10		13		15		ns
				10		20		20		20
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per mux) Enable Disabled		30 8					pF pF	
$C_{IN}$	Maximum Input Capacitance			5	10	10		10		pF
$C_{OUT}$	Maximum Output Capacitance			10	20	20		20		pF

Note 5:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .