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Team Nexperia

74AUP2T1326

Low-power dual supply buffer/line driver; 3-state

Rev. 2 — 3 July 2012 Product data sheet

1. General description

The 74AUP2T1326 is a high-performance, dual supply, low-power, low-voltage, dual buffer/line driver with output enable circuitry.

The 74AUP2T1326 is designed for logic-level translation and combines the functions of the 74AUP1G32 and 74AUP2G126. The buffer/line driver is controlled by two output enable inputs (1OE and 2OE). A logic LOW on input 1OE causes the output 2Y to assume a high-impedance OFF-state, a logic LOW on 2OE causes the output 3Y to assume a high-impedance OFF-state. The output 1Y is the result of a logic OR of the two output enable inputs.

The output enable inputs (1OE and 2OE) are Schmitt trigger inputs, they switch at different voltages for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the input hysteresis voltage V_H. The output enable inputs accept standard input signals and are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals

Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.1 V and 3.6 V making the device suitable for interfacing between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V) with compatible input levels. Pins 1OE, 2OE and 1Y are referenced to $V_{CC(A)}$ and pins A, 2Y and 3Y are referenced to $V_{CC(B)}$.

The device ensures low static and dynamic power consumption and is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing any damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.1 V to 3.6 V; $V_{CC(B)}$: 1.1 V to 3.6 V.
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F Class 2A exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; I_{CC} = 0.9 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II

- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from −40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2T1326GF	−40 °C to +85 °C	XSON10	plastic extremely thin small outline package; no leads; 10 terminals; body 1 x 1.7 x 0.5 mm	SOT1081-2

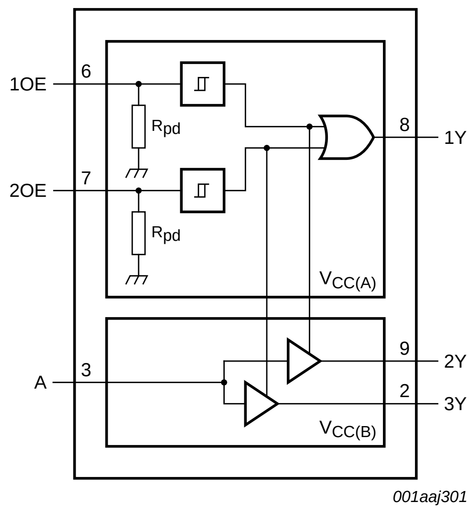
4. Marking

Table 2. Marking

Type number	Marking code[1]
74AUP2T1326GF	pf

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



R_{pd} = Internal pull-down resistor.

Fig 1. Logic symbol

6. Pinning information

6.1 Pinning

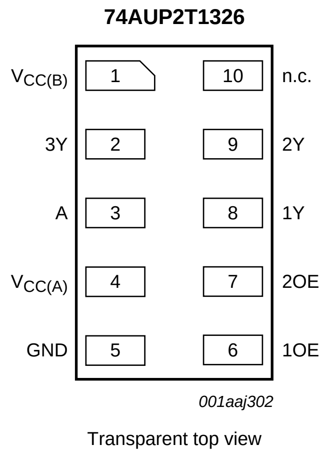


Fig 2. Pin configuration SOT1081-2 (XSON10)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{CC(B)}$	1	supply voltage B
3Y	2	data output
A	3	data input
$V_{CC(A)}$	4	supply voltage A
GND	5	ground (0 V)
1OE	6	output enable input (Schmitt trigger input)
2OE	7	output enable input (Schmitt trigger input)
1Y	8	data output
2Y	9	data output
n.c.	10	not connected

7. Functional description

Table 4. Function table[1]

Input			Output		
1OE	2OE	A	1Y	2Y	3Y
L	L	X	L	Z	Z
L	H	L	H	Z	L
L	H	H	H	Z	H
H	L	L	H	L	Z
H	L	H	H	H	Z
H	H	L	H	L	L
H	H	H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			–0.5	+4.6	V
$V_{CC(B)}$	supply voltage B			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	–0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	[2]	–50	-	mA
V_O	output voltage	Active mode and Power-down mode	[1]	–0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CCO}	[2]	-	±20	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	[3]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with an output pin.

[3] For XSON10 package: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			1.1	3.6	V
$V_{CC(B)}$	supply voltage B			1.1	3.6	V
V_I	input voltage			0	3.6	V
V_O	output voltage		[1]	0	V_{CCO}	V

Table 6. Recommended operating conditions *...continued*

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	ambient temperature			–40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	input A; V_{CCI} = 1.1 V to 3.6 V	[2]	-	200	ns/V
		input nOE; V_{CCI} = 1.1 V to 3.6 V	[2]	-	30	ms/V

[1] V_{CCO} is the supply voltage associated with an output pin.

[2] V_{CCI} is the supply voltage associated with an input pin.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	input A;	[1][3]						
		V_{CCI} = 1.65 V to 1.95 V		0.65V_{CCI}	-	-	0.65V_{CCI}	-	V
		V_{CCI} = 2.3 V to 2.7 V		1.6	-	-	1.6	-	V
V_{IL}	LOW-level input voltage	input A;	[1][3]						
		V_{CCI} = 1.65 V to 1.95 V		-	-	0.35V_{CCI}	-	0.35V_{CCI}	V
		V_{CCI} = 2.3 V to 2.7 V		-	-	0.7	-	0.7	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IL}$ or V_I or $V_I = V_{T+}$ or V_{T-}							
		I_O = –20 μA; V_{CCO} = 1.65 V to 2.7 V	[2]	V_{CCO} – 0.1	-	-	V_{CCO} – 0.1	-	V
		I_O = –3 mA; V_{CCO} = 1.65 V		1.2	-	-	1.2	-	V
		I_O = –2.3 mA; V_{CCO} = 2.3 V		1.97	-	-	1.97	-	V
		I_O = –4.0 mA; V_{CCO} = 2.3 V		2.0	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IL}$ or V_I or $V_I = V_{T+}$ or V_{T-}	[2]						
		I_O = 20 μA; V_{CCO} = 1.65 V to 2.7 V		-	-	0.10	-	0.10	V
		I_O = 3.0 mA; V_{CCO} = 1.65 V		-	-	0.45	-	0.45	V
		I_O = 2.3 mA; V_{CCO} = 2.3 V		-	-	0.33	-	0.33	V
		I_O = 4.0 mA; V_{CCO} = 2.3 V		-	-	0.40	-	0.40	V
I_I	input leakage current	input A; V_I = 0 V to 2.7 V; V_{CCI} = 1.65 V to 2.7 V	[1]	-	-	±0.1	-	±0.5	μA
I_{OZ}	OFF-state output current	output 2Y, 3Y; $V_I = V_{IH}$ or V_{IL}; V_O = 0 V to 2.7 V; $V_{CC(A)}$ = 1.65 V to 2.7 V; $V_{CC(B)}$ = 1.65 V to 2.7 V		-	-	±0.1	-	±0.5	μA
I_{OFF}	power-off leakage current	1Y; $V_{CC(A)}$ = 0 V; V_O = 0 V to 2.7 V; $V_{CC(B)}$ = 1.65 V to 2.7 V		-	-	±0.2	-	±0.5	μA
		A, 2Y, 3Y; $V_{CC(B)}$ = 0 V; V_I or V_O = 0 V to 2.7 V; $V_{CC(A)}$ = 1.65 V to 2.7 V		-	-	±0.2	-	±0.5	μA

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
ΔI_{OFF}	additional power-off leakage current	1Y; $V_{CC(A)}$ = 0 V to 0.2 V; V_O = 0 V to 2.7 V; $V_{CC(B)}$ = 1.65 V to 2.7 V		-	-	±0.2	-	±0.6	μA
		A, 2Y, 3Y; $V_{CC(B)}$ = 0 V to 0.2 V; V_I or V_O = 0 V to 2.7 V; $V_{CC(A)}$ = 1.65 V to 2.7 V		-	-	±0.2	-	±0.6	μA
$I_{CC(A)}$	supply current A	V_I = 0 V or $V_{CC(A)}$; I_O = 0 A	[1]						
		$V_{CC(A)}$ = 1.65 V to 2.7 V; $V_{CC(B)}$ = 0 V to 2.7 V		-	-	0.5	-	0.9	μA
$I_{CC(B)}$	supply current B	V_I = 0 V or $V_{CC(B)}$; I_O = 0 A	[1]						
		$V_{CC(A)}$ = $V_{CC(B)}$ = 1.65 V to 2.7 V;		-	-	0.5	-	0.9	μA
		$V_{CC(A)}$ = 1.71 V; $V_{CC(B)}$ = 2.6 V		-	-	500	-	750	μA
ΔI_{CC}	additional supply current	nOE; $V_{CC(A)}$ = $V_{CC(B)}$ = 2.7 V; V_I = $V_{CC(A)}$ – 0.6 V		-	-	40	-	50	μA
		A; $V_{CC(A)}$ = $V_{CC(B)}$ = 2.7 V; V_I = $V_{CC(B)}$ – 0.6 V;		-	-	80	-	100	μA
		A; V_I = GND to 2.7 V; nOE = GND; $V_{CC(A)}$ = 1.65 V to 2.7 V; $V_{CC(B)}$ = 1.65 V to 2.7 V	[4]	-	-	2	-	2	μA
R_{pd}	pull-down resistance			145	200	255	140	260	kΩ
C_I	input capacitance	input A; V_I = 0 V or V_{CCI}; V_{CCI} = 1.65 V to 2.7 V	[1]	-	0.9	-	-	-	pF
		input nOE; V_I = 0 V or V_{CCI}; V_{CCI} = 1.65 V to 2.7 V	[1]	-	0.8	-	-	-	pF
C_O	output capacitance	1Y; V_O = GND; V_{CCO} = 0 V	[2]	-	1.7	-	-	-	pF
		2Y, 3Y enabled; V_O = GND; V_{CCO} = 0 V	[2]	-	1.7	-	-	-	pF
		2Y, 3Y disabled; V_{CCO} = 0 V to 2.7 V; V_O = GND or V_{CCO}	[2]	-	1.5	-	-	-	pF

[1] V_{CCI} is the supply voltage associated with the input pin.

[2] V_{CCO} is the supply voltage associated with the output pin.

[3] For V_{CCI} values not specified in the data sheet: minimum $V_{IH} = 0.7 \times V_{CCI}$ and maximum $V_{IL} = 0.3 \times V_{CCI}$.

[4] To show I_{CC} remains very low when the input-disable feature is enabled.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 5.

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		Unit
				Min	Typ[1]	Max	Min	Max	
C_L = 5 pF									
t_{pd}	propagation delay	A to 2Y, 3Y; see Figure 3	[2]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		1.9	3.2	4.5	1.7	5.0	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		1.5	2.6	3.4	1.3	3.8	ns
		nOE to 1Y; see Figure 3							
		$V_{CC(A)}$ = 1.65 V to 1.95 V		2.4	4.0	5.4	2.2	6.0	ns
		$V_{CC(A)}$ = 2.3 V to 2.7 V		2.2	3.2	3.9	2.0	4.3	ns
C_L = 10 pF									
t_{pd}	propagation delay	A to 2Y, 3Y; see Figure 3	[2]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.3	3.8	5.3	2.0	5.8	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		1.8	3.2	4.1	1.5	4.5	ns
		nOE to 1Y; see Figure 3							
		$V_{CC(A)}$ = 1.65 V to 1.95 V		2.9	4.6	6.1	2.5	6.7	ns
		$V_{CC(A)}$ = 2.3 V to 2.7 V		2.5	3.7	4.6	2.2	5.0	ns
C_L = 5 pF; $V_{CC(A)}$ = 1.65 V to 1.95 V									
t_{en}	enable time	nOE to 2Y, 3Y; see Figure 4	[3]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.4	4.4	9.7	2.1	10.1	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		2.2	3.9	8.2	1.9	8.8	ns
t_{dis}	disable time	nOE to 2Y, 3Y; see Figure 4	[4]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.4	4.5	8.9	2.1	9.4	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		2.2	3.8	7.8	1.9	8.4	ns
C_L = 5 pF; $V_{CC(A)}$ = 2.3 V to 2.7 V									
t_{en}	enable time	nOE to 2Y, 3Y; see Figure 4	[3]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.4	4.0	8.7	2.1	9.0	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		2.2	3.4	7.2	1.9	7.7	ns
t_{dis}	disable time	nOE to 2Y, 3Y; see Figure 4	[4]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.4	4.2	7.9	2.1	8.3	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		2.2	3.5	6.8	1.9	7.3	ns
C_L = 10 pF; $V_{CC(A)}$ = 1.65 V to 1.95 V									
t_{en}	enable time	nOE to 2Y, 3Y; see Figure 4	[3]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.9	4.9	11.0	2.5	11.7	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		2.5	4.4	9.7	2.2	10.5	ns
t_{dis}	disable time	nOE to 2Y, 3Y; see Figure 4	[4]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.9	5.6	10.8	2.5	11.5	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		2.5	4.6	9.5	2.2	10.1	ns

Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 5.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ[1]	Max	Min	Max	
C_L = 10 pF; $V_{CC(A)}$ = 2.3 V to 2.7 V									
t_{en}	enable time	nOE to 2Y, 3Y; see Figure 4	[3]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.9	4.5	10.0	2.5	10.5	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		2.5	3.9	8.7	2.2	9.3	ns
t_{dis}	disable time	nOE to 2Y, 3Y; see Figure 4	[4]						
		$V_{CC(B)}$ = 1.65 V to 1.95 V		2.9	5.3	9.8	2.5	10.3	ns
		$V_{CC(B)}$ = 2.3 V to 2.7 V		2.5	4.3	8.4	2.2	8.9	ns
C_L = 5 pF and 10 pF									
C_{PD}	power dissipation capacitance	per active output; output 2Y, 3Y; f_i = 1 MHz; V_I = 0 V to V_{CC}	[5]						
		$V_{CC(A)} = V_{CC(B)}$ = 1.8 V		-	3.0	-	-	-	pF
		$V_{CC(A)} = V_{CC(B)}$ = 2.5 V		-	3.6	-	-	-	pF

[1] All typical values are measured at nominal $V_{CC(A)}$ and $V_{CC(B)}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZH} and t_{PZL}.

[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

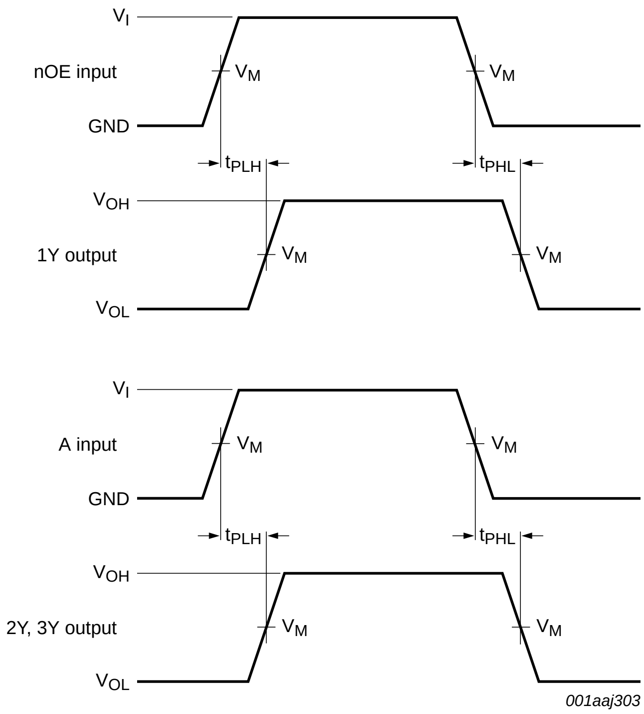
C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

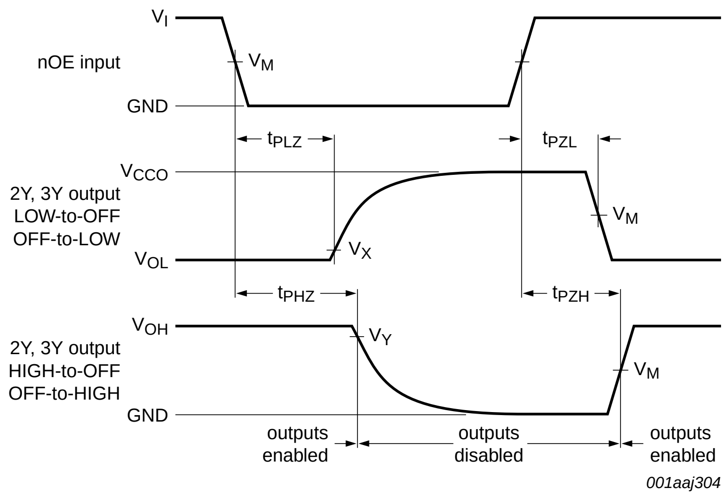
12. Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 3. Input nOE to output 1Y and A to output 2Y, 3Y propagation delay times



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

V_{CCO} is the supply voltage associated with the output pin.

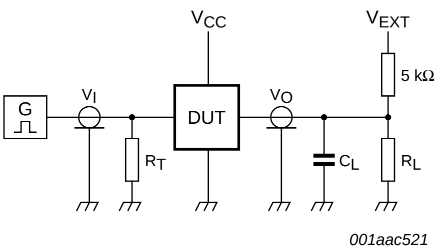
Fig 4. Enable and disable times

Table 9. Measurement points

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load[2]		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I[1]	$t_r = t_f$	C_L	R_L[3]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[4]
1.65 V to 2.7 V	V_{CCI}	≤ 3.0 ns	5 pF, 10 pF	5 kΩ or 1 MΩ	open	GND	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] For measuring enable and disable times, C_L and R_L are connected to pin 2Y and 3Y.

[3] For measuring enable and disable times R_L = 5 kΩ, for measuring propagation delays R_L = 1 MΩ.

[4] V_{CCO} is the supply voltage associated with the output port.

13. Transfer characteristics

Table 11. Transfer characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 5.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{T+}	positive-going threshold voltage	nOE inputs; see Figure 6 and Figure 7						
		$V_{CC(A)}$ = 1.65 V	0.91	-	1.29	0.91	1.29	V
		$V_{CC(A)}$ = 2.3 V	1.37	-	1.77	1.37	1.77	V
V_{T-}	negative-going threshold voltage	nOE inputs; see Figure 6 and Figure 7						
		$V_{CC(A)}$ = 1.65 V	0.47	-	0.84	0.47	0.84	V
		$V_{CC(A)}$ = 2.3 V	0.69	-	1.04	0.69	1.04	V
V_H	hysteresis voltage	nOE inputs; ($V_{T+} - V_{T-}$); see Figure 6, Figure 7 and Figure 8						
		$V_{CC(A)}$ = 1.65 V	0.27	-	0.66	0.27	0.66	V
		$V_{CC(A)}$ = 2.3 V	0.53	-	0.92	0.53	0.92	V

14. Waveforms transfer characteristics

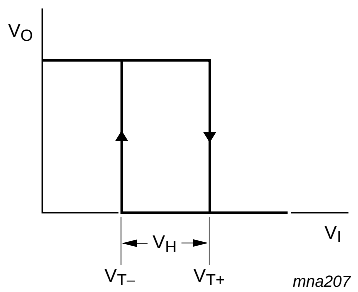
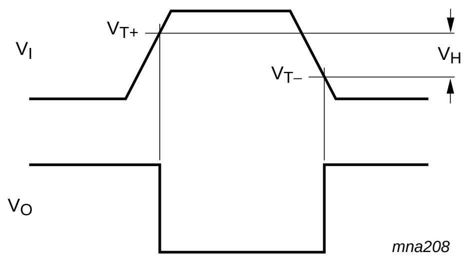


Fig 6. Transfer characteristic



V_{T+} and V_{T-} limits at 70 % and 20 %.

Fig 7. Definition of V_{T+}, V_{T-} and V_H

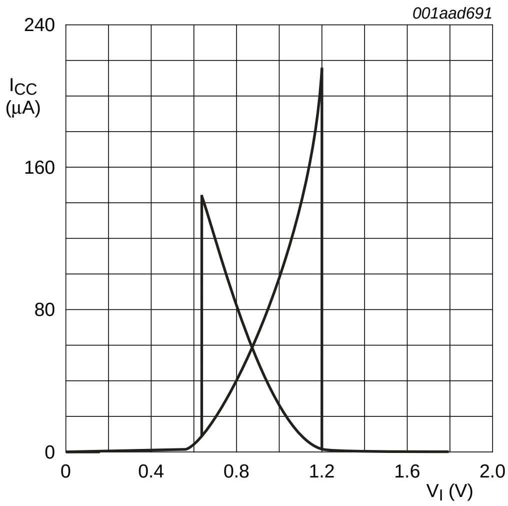
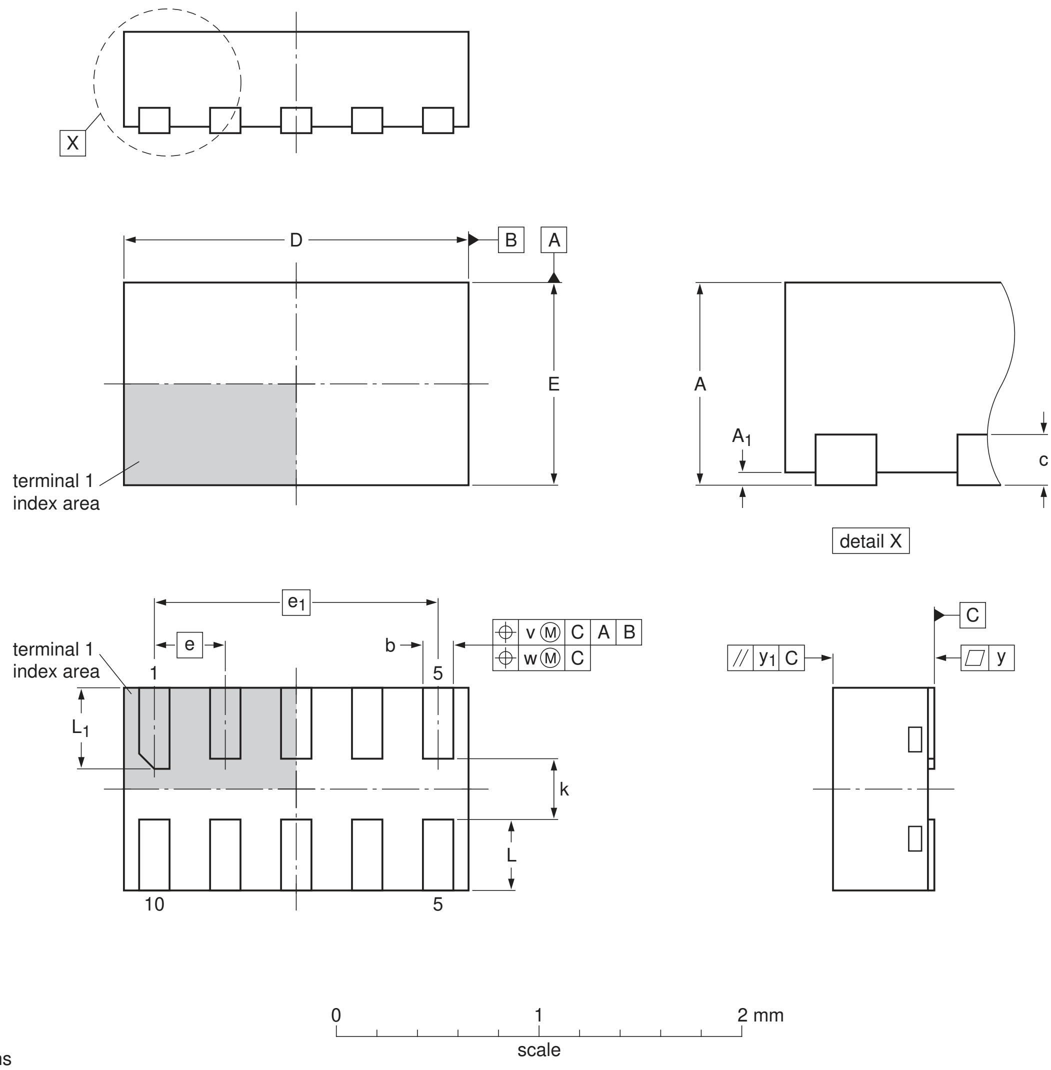


Fig 8. Typical transfer characteristics; $V_{CC(A)}$ = 1.8 V

15. Package outline

XSON10: plastic extremely thin small outline package; no leads;
10 terminals; body 1.0 x 1.7 x 0.5 mm **SOT1081-2**



Dimensions

Unit[1]		A	A_1	b	c	D	E	e	e_1	k	L	L_1	v	w	y	y_1
	max	0.5	0.05	0.20		1.8	1.1				0.40	0.45				
mm	nom			0.15	0.127	1.7	1.0	0.35	1.4		0.35	0.40	0.1	0.05	0.05	0.05
	min		0.00	0.10		1.6	0.9			0.2	0.30	0.35				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1081-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1081-2	- - -	- - -	- - -			~~10-11-08~~ 11-03-30

Fig 9. Package outline SOT1081-2 (XSON10)

16. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2T1326 v.2	20120703	Product data sheet	-	74AUP2T1326 v.1
Modifications:	• For type number 74AUP2T1326GF the sot code has changed to SOT1081-2.			
74AUP2T1326 v.1	20090701	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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