



High-Bandwidth, T1/E1, SPST Analog Switches

General Description

The MAX4815/MAX4816/MAX4817 high-bandwidth, low-on-resistance, quad-SPST analog switches are designed to serve as integrated T1/E1 protection switches for 1+1 and N+1 line-card redundancy applications. Each MAX4815/MAX4816/MAX4817 replaces four electromechanical relays, significantly reducing board space, simplifying PC board routing, and reducing power consumption. These devices operate with $\pm 3.3\text{V}$ or $\pm 5\text{V}$ dual supplies for applications requiring T1/E1 signal switching in the line side of the interface transformer. Internal voltage multipliers drive the analog switches, yielding excellent linearity and low 3.7Ω typical on-resistance within the T1/E1 analog signal range. This high-bandwidth (550MHz typical) family of products is optimized for low return loss and matched pulse template performance in T1/E1 long-haul and short-haul applications.

The MAX4815/MAX4816/MAX4817 are available in a tiny 16-pin, 5mm x 5mm, thin QFN package and are specified over the extended -40°C to $+85^\circ\text{C}$ temperature range.

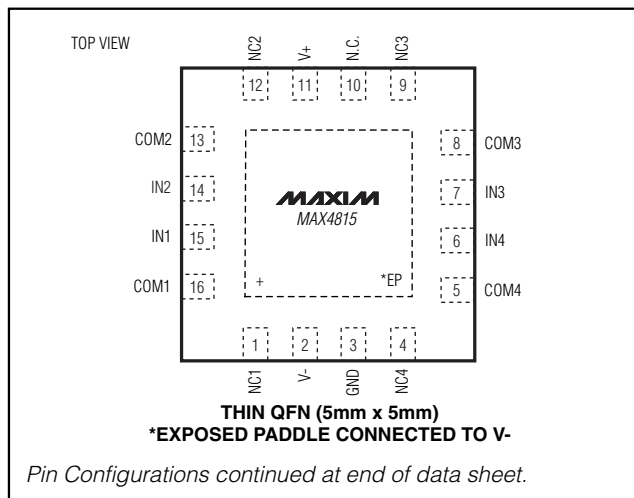
Applications

T1/E1 Redundancy Switching
 Base Stations and Base-Station Controllers
 Add and Drop Multiplexers
 Multiservice Provisioning Platforms
 Edge Routers
 Multiservice Switches (MSSs)
 Digital Loop Carriers
 Industrial Applications
 Data Acquisition
 Telecom Signal Switching
 Test Equipment
 Avionics

Features

- ◆ Quad-SPST NO, NC, and NC/NO Configurations
- ◆ Dual-Supply Operation from $\pm 3.3\text{V}$ to $\pm 5\text{V}$
- ◆ Single-Supply Operation from $+6\text{V}$ to $+11\text{V}$
- ◆ Hot Insertion Tolerant with No DC Path to the Supplies
- ◆ Low On-Resistance, $R_{ON} = 3.7\Omega$ (typ) and 6Ω (max)
- ◆ Over 550MHz, -3dB Signal Bandwidth
- ◆ Excellent Crosstalk and Off-Isolation Performance Over the T1/E1 Signal Spectrum: 110dB Crosstalk Attenuation at 1MHz
- ◆ Low Current Consumption of 2mA (max)
- ◆ -40°C to $+85^\circ\text{C}$ Extended Temperature Range
- ◆ Space-Saving, 16-Pin, 5mm x 5mm Thin QFN

Pin Configurations



Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | CONFIGURATION | PKG CODE |
|-------------|--|-------------|----------------|----------|
| MAX4815ETE+ | -40°C to $+85^\circ\text{C}$ | 16 TQFN-EP* | 4 x SPST NC | T1655-3 |
| MAX4816ETE+ | -40°C to $+85^\circ\text{C}$ | 16 TQFN-EP* | 4 x SPST NO | T1655-3 |
| MAX4817ETE+ | -40°C to $+85^\circ\text{C}$ | 16 TQFN-EP* | 4 x SPST NC/NO | T1655-3 |

*EP = Exposed paddle.

Devices are available in lead-free packaging.



High-Bandwidth, T1/E1, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND unless otherwise noted.)

| | |
|--|---------------------------|
| V+ |-0.3V to +6V |
| V- |-6V to +0.3V |
| V+ to V- |-0.3V to +12V |
| IN |-0.3V to (V+ + 0.3V) |
| NO ₋ , NC ₋ , COM ₋ |-12V to +12V |
| NO ₋ to COM ₋ , NC ₋ to COM ₋ |-18V to +18V |
| Continuous Current (NO ₋ , NC ₋ , COM ₋) | ±100mA |
| Continuous Current (any other terminal) | ±30mA |

| | |
|--|--|
| Peak Current (NO ₋ , NC ₋ , COM ₋) | (pulsed at 1ms, 10% duty cycle)..... ±300mA |
| Continuous Power Dissipation (T _A = +70°C) | 16-Pin Thin QFN 5mm x 5mm (derate 33.3mW/°C above +70°C)2667mW |
| Operating Temperature Range |-40°C to +85°C |
| Storage Temperature Range |-65°C to +150°C |
| Junction Temperature |+150°C |
| Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual ±3.3V Supplies

(V+ = +3.3V ±10%, V- = -3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|-----|-----|-------|
| ANALOG SWITCH | | | | | | |
| Fault-Free Analog Signal Range | V _{COM-} V _{NO-} V _{NC-} | | V- | | V+ | V |
| On-Resistance (Note 2) | R _{ON} | V+ = +3V, V- = -3V, I _{COM-} = 30mA, V _{NO-} or V _{NC-} = +3V | T _A = +25°C | 3.7 | 5 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 6 | |
| On-Resistance Match Between Channels (Notes 2, 3) | ΔR _{ON} | V+ = +3V, V- = -3V, I _{COM-} = 30mA, V _{NO-} or V _{NC-} = +3V | T _A = +25°C | 0.1 | 0.6 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 0.8 | |
| On-Resistance Flatness (Notes 2, 4) | R _{FLAT(ON)} | V+ = +3V, V- = -3V, I _{COM-} = 30mA; V _{NO-} or V _{NC-} = -3V, 0V, +3V | T _A = +25°C | 0.4 | 1.2 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 1.5 | |
| NO or NC Off-Leakage Current | I _{NO-(OFF)} I _{NC-(OFF)} | V+ = +3.6V, V- = -3.6V; V _{COM-} = -3V, +3V; V _{NO-} or V _{NC-} = +3V, -3V | -10 | | +10 | nA |
| COM Off-Leakage Current | I _{COM-(OFF)} | V+ = +3.6V, V- = -3.6V; V _{COM-} = -3V, +3V; V _{NO-} or V _{NC-} = +3V, -3V | -10 | | +10 | nA |
| COM On-Leakage Current | I _{COM-(ON)} | V+ = +3.6V, V- = -3.6V; V _{COM-} = -3V, +3V; NO ₋ or NC ₋ unconnected | -15 | | +15 | nA |
| FAULT | | | | | | |
| Fault Analog Signal Range | V _{COM-} | V+ = +3.3V, V- = -3.3V | -11 | | +11 | V |

High-Bandwidth, T1/E1, SPST Analog Switches

MAX4815/MAX4816/MAX4817

ELECTRICAL CHARACTERISTICS—Dual ±3.3V Supplies (continued)

(V+ = +3.3V ±10%, V- = -3.3V ±10%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|--------------|---|-------------------|-----|------|-------|
| NO or NC Off-Leakage Current | INO_ INC_ | V+ = +3.3V, V- = -3.3V; VNO_ or VNC_ = +11V, -11V; VCOM_ = -5.5V, +5.5V | -1 | | +1 | μA |
| COM Off-Leakage Current | ICOM_ | V+ = +3.3V, V- = -3.3V; VCOM_ = +11V, -11V; VNO_ or VNC_ = -5.5V, +5.5V | -1 | | +1 | μA |
| SWITCH DYNAMIC CHARACTERISTICS | | | | | | |
| Crosstalk (Note 5) | VCT1 | RL = 50Ω, f = 1.024MHz, Figure 4 | | 110 | | dB |
| | VCT2 | RL = 50Ω, f = 30MHz, Figure 4 | | 77 | | |
| Off-Isolation (Note 6) | VISO1 | VCOM_ to VNO_ or VNC_, RL = 50Ω, f = 1.024MHz, Figure 4 | | 60 | | dB |
| | VISO2 | VCOM_ to VNO_ or VNC_, RL = 50Ω, f = 30MHz, Figure 4 | | 30 | | |
| On-Channel -3dB Bandwidth | BW | RS = RL = 50Ω, Figure 4 | | 550 | | MHz |
| COM On-Capacitance | CON(COM_) | f = 1MHz, Figure 5 | | 10 | | pF |
| COM Off-Capacitance | COFF(COM_) | f = 1MHz, Figure 5 | | 7 | | pF |
| NC/NO Off-Capacitance | COFF | f = 1MHz, Figure 5 | | 7 | | pF |
| Charge Injection | Q | CL = 1.0nF, VGEN = 0, RGEN = 0, Figure 3 | | 55 | | pC |
| Fault Recovery Time | tREC | VNO_, VNC_, VCOM_ = -11V | | 128 | | μs |
| Turn-On Time | tON | VNO_ or VNC_ = +3V, RL = 300Ω, CL = 35pF, Figure 2 | TA = +25°C | 20 | 40 | μs |
| | | | TA = TMIN to TMAX | | | |
| Turn-Off Time | tOFF | VNO_ or VNC_ = +3V, RL = 300Ω, CL = 35pF, Figure 2 | TA = +25°C | 0.5 | 1 | μs |
| | | | TA = TMIN to TMAX | | | |
| Power-Up Delay | tDEL | | | 128 | | μs |
| LOGIC INPUT (IN_) | | | | | | |
| Input-Voltage Low | VIL | | | | 0.8 | V |
| Input-Voltage High | VIH | | 2.4 | | | V |
| Input Leakage Current | IIN | VIN = 0 or V+ | -1 | | +1 | μA |
| POWER SUPPLY | | | | | | |
| Quiescent Positive Supply Current | I+ | V+ = +3.6V, V- = -3.6V, VIN_ = 0 or V+ | | 0.8 | 2 | mA |
| Quiescent Negative Supply Current | I- | V+ = +3.6V, V- = -3.6V, VIN_ = 0 or V+ | | 0.8 | 2 | mA |
| Negative Supply Voltage | V- | | -3.6 | | -3.0 | V |
| Positive Supply Voltage | V+ | | 3.0 | | 3.6 | V |

High-Bandwidth, T1/E1, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Dual $\pm 5V$ Supplies

($V_+ = +5V \pm 10\%$, $V_- = -5V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|--|-----|-----|-----|----------|
| ANALOG SWITCH | | | | | | |
| Fault-Free Analog Signal Range | $V_{COM_}$ $V_{NO_}$ $V_{NC_}$ | | V- | | V+ | V |
| On-Resistance (Note 2) | R_{ON} | $V_+ = +4.5V$, $V_- = -4.5V$, $I_{COM_} = 30mA$, $V_{NO_}$ or $V_{NC_} = +3V$ | | 3.7 | 5 | Ω |
| | | $T_A = +25^\circ C$ $T_A = T_{MIN}$ to T_{MAX} | | | 6 | |
| On-Resistance Match Between Channels (Notes 2, 3) | ΔR_{ON} | $V_+ = +4.5V$, $V_- = -4.5V$, $I_{COM_} = 30mA$, $V_{NO_}$ or $V_{NC_} = +3V$ | | 0.1 | 0.6 | Ω |
| | | $T_A = +25^\circ C$ $T_A = T_{MIN}$ to T_{MAX} | | | 0.8 | |
| On-Resistance Flatness (Notes 2, 4) | $R_{FLAT(ON)}$ | $V_+ = +4.5V$, $V_- = -4.5V$, $I_{COM_} = 30mA$; $V_{NO_}$ or $V_{NC_} = -3V, 0V$, $+3V$ | | 0.4 | 1.2 | Ω |
| | | $T_A = +25^\circ C$ $T_A = T_{MIN}$ to T_{MAX} | | | 1.5 | |
| NO or NC Off-Leakage Current | $I_{NO_(OFF)}$ $I_{NC_(OFF)}$ | $V_+ = +5.5V$, $V_- = -5.5V$; $V_{COM_} = -5V, +5V$; $V_{NO_}$ or $V_{NC_} = +5V, -5V$ | -10 | | +10 | nA |
| COM Off-Leakage Current | $I_{COM_(OFF)}$ | $V_+ = +5.5V$, $V_- = -5.5V$; $V_{COM_} = -5V, +5V$; $V_{NO_}$ or $V_{NC_} = +5V, -5V$ | -10 | | +10 | nA |
| COM On-Leakage Current | $I_{COM_(ON)}$ | $V_+ = +5.5V$, $V_- = -5.5V$; $V_{COM_} = -5V, +5V$; NO_- or NO_- unconnected | -15 | | +15 | nA |
| FAULT | | | | | | |
| Fault Analog Signal Range | $V_{COM_}$ $V_{NO_}$ $V_{NC_}$ | $V_+ = +5V$, $V_- = -5V$ | -11 | | +11 | V |
| NO or NC Off-Leakage Current | $I_{NO_}$ $I_{NC_}$ | $V_+ = +5V$, $V_- = -5V$; $V_{NO_}$ or $V_{NC_} = +11V, -11V$; $V_{COM_} = -5.5V, +5.5V$ | -1 | | +1 | μA |
| COM Off-Leakage Current | $I_{COM_}$ | $V_+ = +5V$, $V_- = -5V$; $V_{COM_} = +11V, -11V$; $V_{NO_}$ or $V_{NC_} = -5.5V, +5.5V$ | -1 | | +1 | μA |
| SWITCH DYNAMIC CHARACTERISTICS | | | | | | |
| Crosstalk (Note 5) | V_{CT1} | $R_L = 50\Omega$, $f = 1.024MHz$, Figure 4 | | 110 | | dB |
| | V_{CT2} | $R_L = 50\Omega$, $f = 30MHz$, Figure 4 | | 77 | | |

High-Bandwidth, T1/E1, SPST Analog Switches

MAX4815/MAX4816/MAX4817

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------------|------------|--|-------------------|-----|------|-------|
| Off-Isolation (Note 6) | VISO1 | VCOM_ to VNO_ or VNC_, RL = 50Ω, f = 1.024MHz, Figure 4 | | 60 | | dB |
| | VISO2 | VCOM_ to VNO_ or VNC_, RL = 50Ω, f = 30MHz, Figure 4 | | 30 | | |
| On-Channel -3dB Bandwidth | BW | RS = RL = 50Ω, Figure 4 | | 550 | | MHz |
| COM On-Capacitance | CON(COM_) | f = 1MHz, Figure 5 | | 10 | | pF |
| COM Off-Capacitance | COFF(COM_) | f = 1MHz, Figure 5 | | 7 | | pF |
| NC/NO Off-Capacitance | COFF | f = 1MHz, Figure 5 | | 7 | | pF |
| Charge Injection | Q | CL = 1.0nF, VGEN = 0, RGEN = 0, Figure 3 | | 55 | | pC |
| Fault Recovery Time | tREC | VNO_, VNC_, VCOM_ = -11V | | 128 | | μs |
| Turn-On Time | tON | VNO_ or VNC_ = +3V, RL = 300Ω, CL = 35pF, Figure 2 | TA = +25°C | 20 | 40 | μs |
| | | | TA = TMIN to TMAX | | 40 | |
| Turn-Off Time | tOFF | VNO_ or VNC_ = +3V, RL = 300Ω, CL = 35pF, Figure 2 | TA = +25°C | 0.5 | 1 | μs |
| | | | TA = TMIN to TMAX | | 1 | |
| Power-Up Delay | tDEL | | | 128 | | μs |
| LOGIC INPUT (IN_) | | | | | | |
| Input-Voltage Low | VIL | | | | 0.8 | V |
| Input-Voltage High | VIH | | 2.4 | | | V |
| Input Leakage Current | IIN | VIN = 0 or V+ | -1 | | +1 | μA |
| POWER SUPPLY | | | | | | |
| Quiescent Positive Supply Current | I+ | V+ = +5.5V, V- = -5.5V, VIN_ = 0 or V+ | | 0.9 | 2 | mA |
| Quiescent Negative Supply Current | I- | V+ = +5.5V, V- = -5.5V, VIN_ = 0 or V+ | | 0.9 | 2 | mA |
| Negative Supply Voltage | V- | | -5.5 | | -4.5 | V |
| Positive Supply Voltage | V+ | | 4.5 | | 5.5 | V |

Note 1: All parameters are production tested at TA = +85°C and guaranteed by design over specified temperature range.

Note 2: Guaranteed by design, not production tested.

Note 3: ΔRON = RON(MAX) - RON(MIN).

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

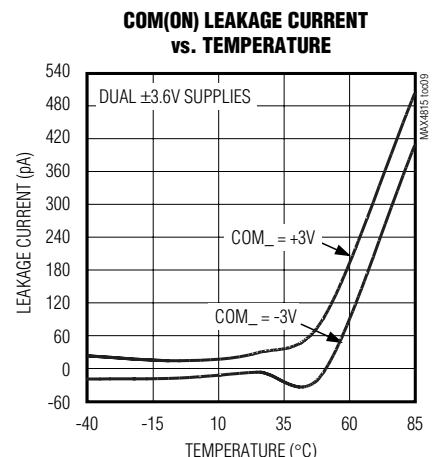
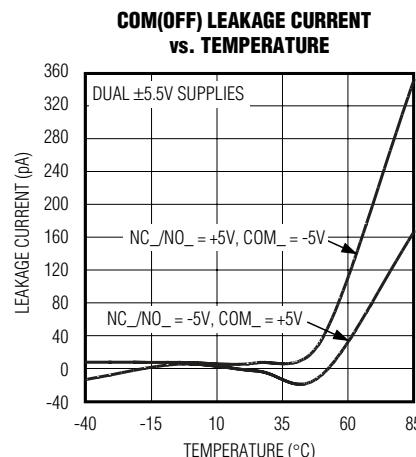
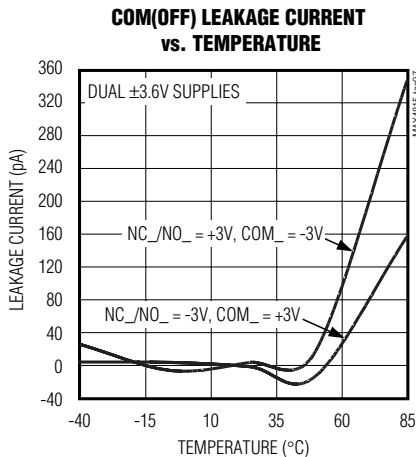
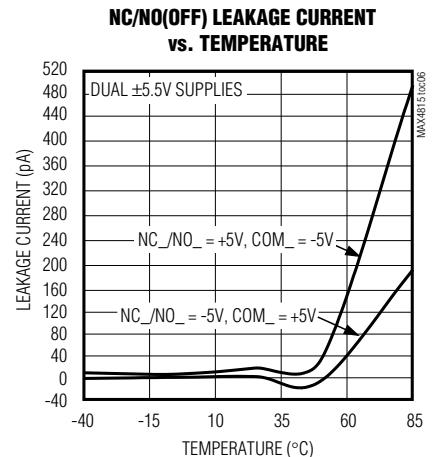
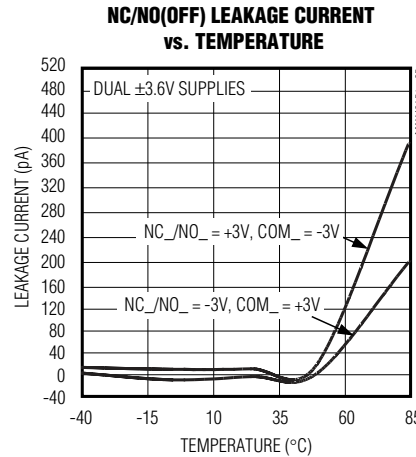
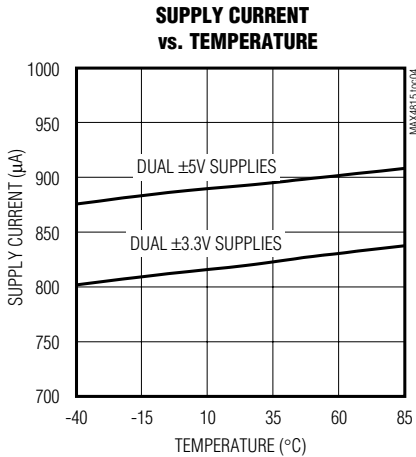
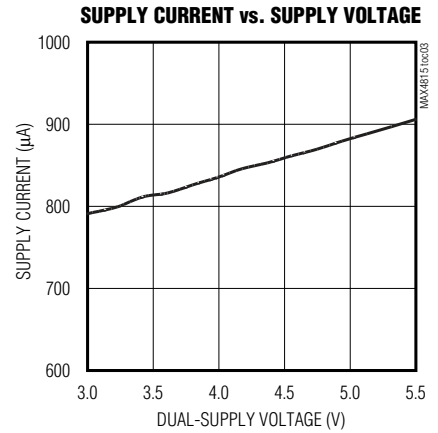
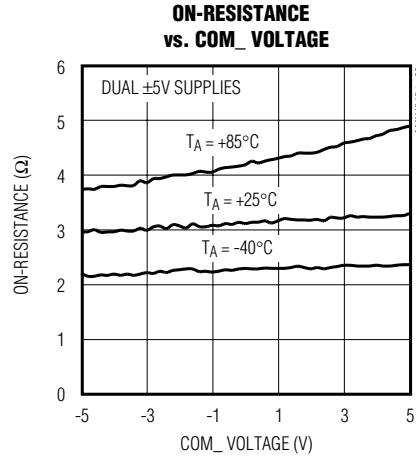
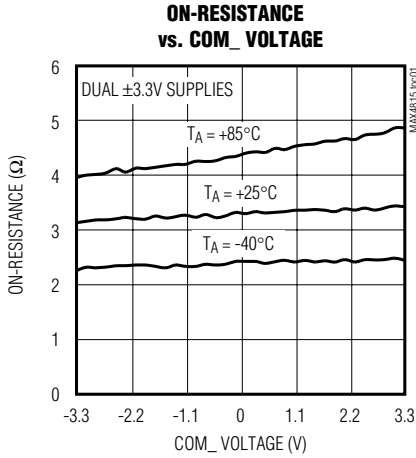
Note 5: Between any two switches.

Note 6: Off-isolation = 20 × log10 [VCOM_/(VNC_ or VNO_)], VCOM_ = output, VNC_ or VNO_ = input to OFF switch.

High-Bandwidth, T1/E1, SPST Analog Switches

Typical Operating Characteristics

(V+ = +3.3V, V- = -3.3V, T_A = +25°C, unless otherwise noted.)

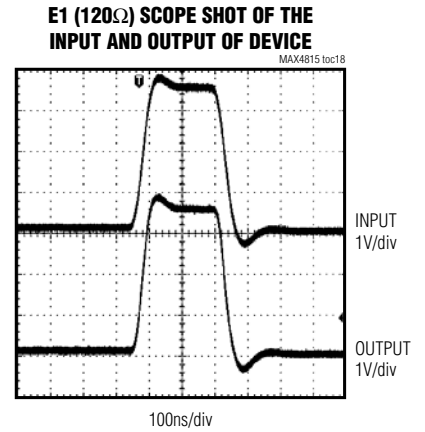
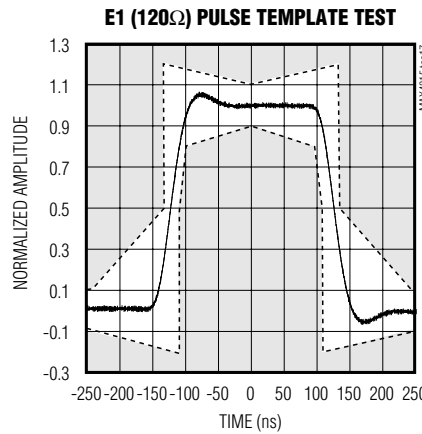
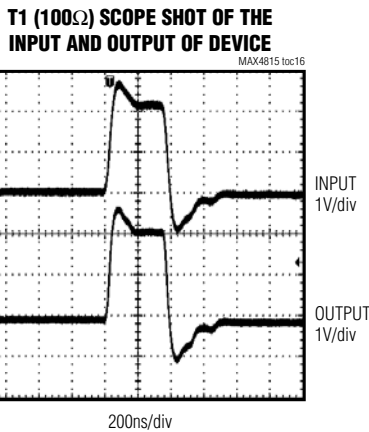
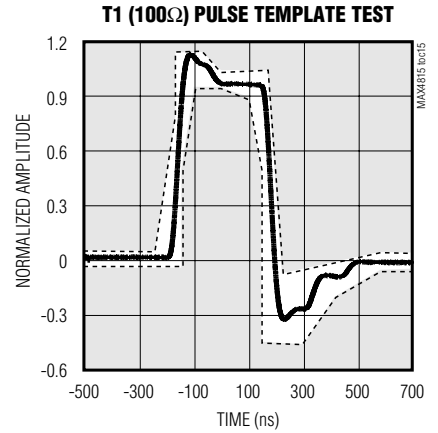
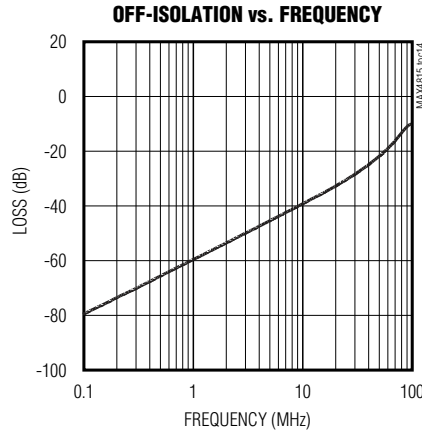
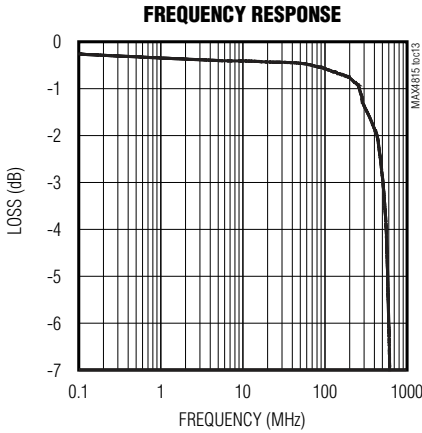
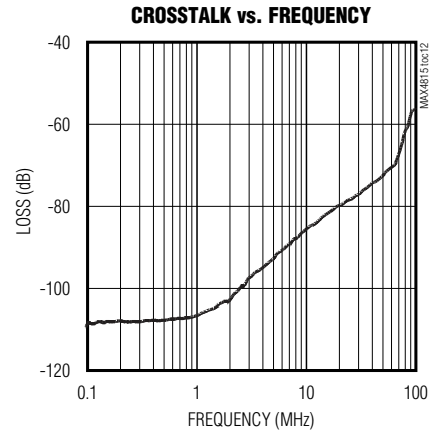
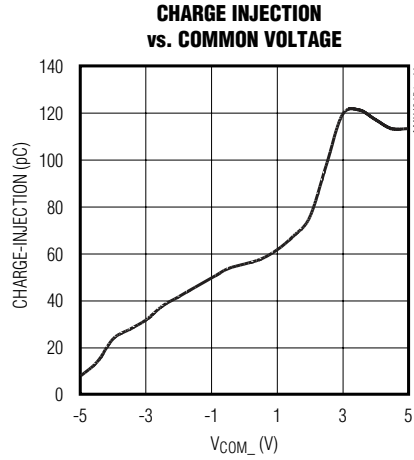
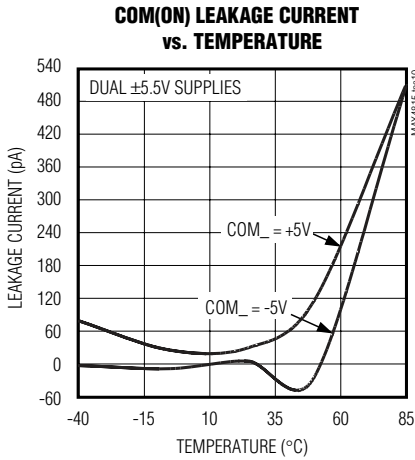


High-Bandwidth, T1/E1, SPST Analog Switches

Typical Operating Characteristics (continued)

(V+ = +3.3V, V- = -3.3V, T_A = +25°C, unless otherwise noted.)

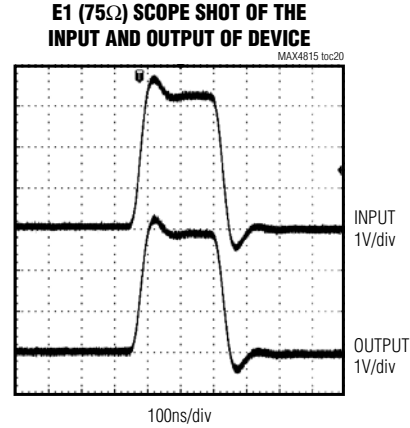
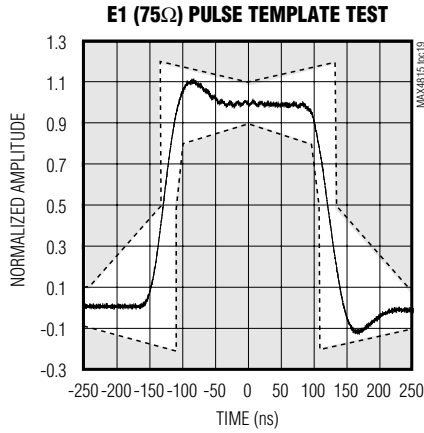
MAX4815/MAX4816/MAX4817



High-Bandwidth, T1/E1, SPST Analog Switches

Typical Operating Characteristics (continued)

(V+ = +3.3V, V- = -3.3V, T_A = +25°C, unless otherwise noted.)



Pin Description

| PIN | | | NAME | FUNCTION |
|---------|---------|---------|------|--|
| MAX4815 | MAX4816 | MAX4817 | | |
| 1 | — | — | NC1 | Analog Switch Normally Closed Terminal 1 |
| 2 | 2 | 2 | V- | Negative Supply Voltage. Bypass V- to ground with a 0.1μF ceramic capacitor. |
| 3 | 3 | 3 | GND | Ground |
| 4 | — | — | NC4 | Analog Switch Normally Closed Terminal 4 |
| 5 | 5 | 5 | COM4 | Analog Switch Common Terminal 4 |
| 6 | 6 | 6 | IN4 | Switch 4 Logic-Control Input |
| 7 | 7 | 7 | IN3 | Switch 3 Logic-Control Input |
| 8 | 8 | 8 | COM3 | Analog Switch Common Terminal 3 |
| 9 | — | 9 | NC3 | Analog Switch Normally Closed Terminal 3 |
| 10 | 10 | 10 | N.C. | No Connection. Not internally connected. |
| 11 | 11 | 11 | V+ | Positive Supply Voltage. Bypass V+ to ground with a 0.1μF ceramic capacitor. |
| 12 | — | 12 | NC2 | Analog Switch Normally Closed Terminal 2 |
| 13 | 13 | 13 | COM2 | Analog Switch Common Terminal 2 |
| 14 | 14 | 14 | IN2 | Switch 2 Logic-Control Input |
| 15 | 15 | 15 | IN1 | Switch 1 Logic-Control Input |
| 16 | 16 | 16 | COM1 | Analog Switch Common Terminal 1 |
| — | 1 | 1 | NO1 | Analog Switch Normally Open Terminal 1 |
| — | 4 | 4 | NO4 | Analog Switch Normally Open Terminal 4 |
| — | 9 | — | NO3 | Analog Switch Normally Open Terminal 3 |
| — | 12 | — | NO2 | Analog Switch Normally Open Terminal 2 |
| EP | EP | EP | EP | Exposed Paddle. Connect exposed paddle to V- or leave unconnected. |

High-Bandwidth, T1/E1, SPST Analog Switches

MAX4815/MAX4816/MAX4817

Detailed Description

The MAX4815/MAX4816/MAX4817 are high-bandwidth, low-on-resistance, quad-SPST analog switches targeted to serve as integrated T1/E1 analog protection switches for 1+1 and N+1 line-card redundancy applications. These devices are designed to replace electromechanical relays to save board space, reduce power consumption, and simplify PC board routing. The devices allow the user to live insert the boards with no adverse effects.

The MAX4815/MAX4816/MAX4817 support $\pm 3.3\text{V}$ or $\pm 5\text{V}$ dual-supply operation, which is required for E1/T1 signal switching in the line-side of the interface transformer. Internal voltage multipliers supply the switches yielding excellent linearity and low on-resistance, typically 3.7Ω , within the E1/T1 analog signal range. This high-bandwidth, typically 550MHz, family of devices is optimized for low return loss and matched pulse template performance in E1/T1 short-haul and long-haul applications.

Analog Signal Levels

The on-resistance of the MAX4815/MAX4816/MAX4817 is very low and stable as the analog signals are swept from V- to V+ (see the *Typical Operating Characteristics*).

Fault Protection

The fault protection of the MAX4815/MAX4816/MAX4817 allows the devices to handle input signals of more than twice the supply voltage without clamping the signal, latching up, or disturbing other cards in the system. The device detects when the input voltage drops below the negative supply. As soon as a fault condition is detected, the switch is immediately turned off for 128 clock cycles (typically $128\mu\text{s}$). At the end of the $128\mu\text{s}$ timeout, the switch is turned back on for one clock cycle. At the end of the one clock cycle, if the signal is within the operating range, the switch will remain on. Otherwise, the device will turn the switch off again for 128 clock cycles. This will repeat until the signal is within the operating range. In T1/E1 redundancy applications, this can happen when the load resistor (R_L) is removed or disconnected for any reason, as shown in Figure 1. Without a load resistor, the output voltage when using a 1:2 transformer can be as high as $\pm 11\text{V}$.

Hot Insertion

The MAX4815/MAX4816/MAX4817 tolerate hot insertions, thus are not damaged when inserted into a live backplane. Competing devices can exhibit low impedance when plugged into a live backplane that can cause high power dissipation leading to damage of the device itself. The MAX4815/MAX4816/MAX4817 have relatively high input impedance when V+ and V- are

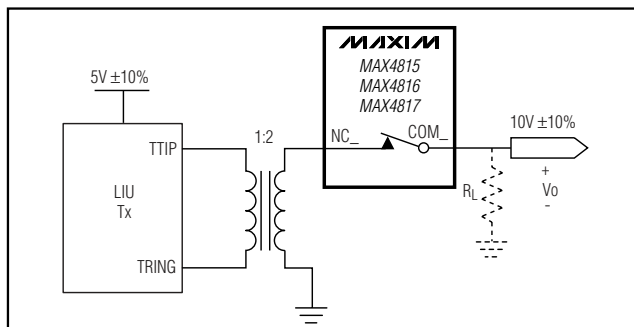


Figure 1. Fault Protection

unconnected or connected to GND. Therefore, the devices are not destroyed by a hot insertion. In order to guarantee data integrity, the V+ and V- supplies must be properly biased.

Applications Information

T1/E1 N+1 Redundancy

The MAX4815/MAX4816/MAX4817 are designed for adjacent line-card protection applications. Figures 6 and 7 show a basic architecture for twisted-pair interface (120Ω E1, or 100Ω T1). Coaxial cable interface (75Ω E1) can be illustrated with the same figures but without the single-ended-to-differential conversion stage. A single protection card can replace up to N line cards in a N+1 redundancy scheme. Figure 6 shows the MAX4815/MAX4816/MAX4817 sitting in the line cards where they can reroute any of the input/output signals to a protection line card. Figure 7 shows the MAX4815/MAX4816/MAX4817 sitting in a protection-switching card where the switches are always powered. These figures do not show the surge protection elements and resistors for line termination/impedance matching.

The low on-resistance and high bandwidth of the MAX4815/MAX4816/MAX4817 yield good pulse template and return-loss performance (see the *Typical Operating Characteristics*). The pulse template tests for E1 (twisted pair interface 120Ω and coaxial interface 75Ω) and T1 (twisted pair interface 100Ω) were tested using the Dallas DS2155 single-chip transceiver evaluation board, and twelve switches in parallel with one switch closed and the other eleven open. The internal transmit termination feature must be disabled when using this circuit. To use the same transmit resistors for E1 twisted pair and coaxial cables, the transmit line build out control register (TLBC) is set to the value 6Ah. This sets the driver voltage so the output pulse has the right amplitude for both 120Ω (twisted pair) and 75Ω (coaxial) loads. The analog switches were powered with dual power supplies at $\pm 5\text{V}$.

High-Bandwidth, T1/E1, SPST Analog Switches

Test Circuits/Timing Diagrams

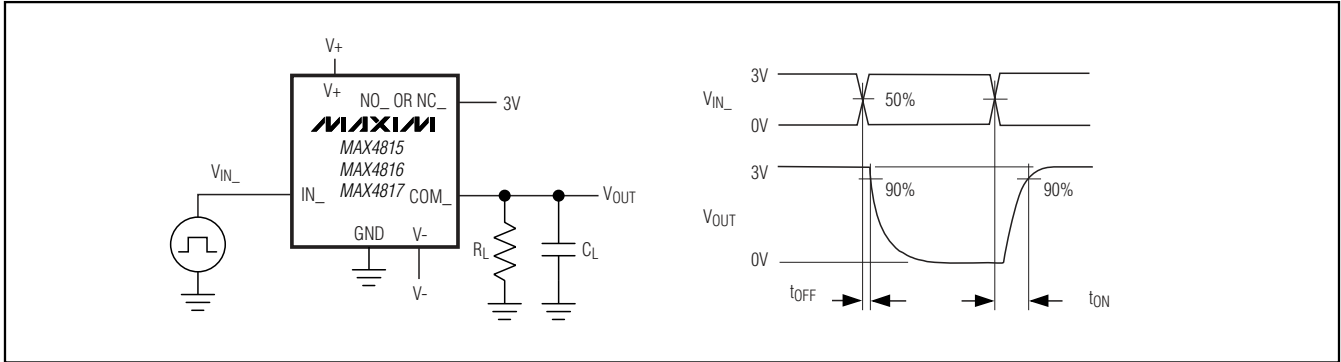


Figure 2. Switch Turn-On/Turn-Off Times

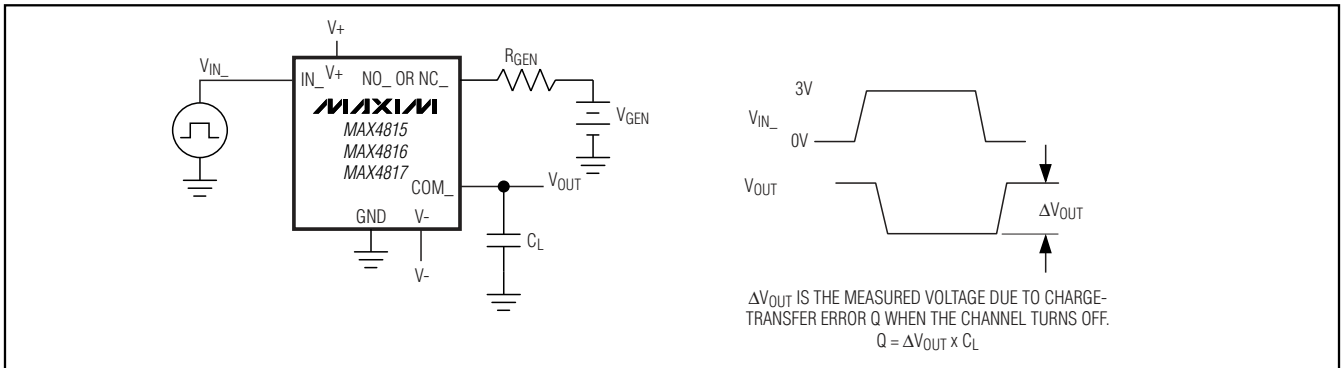


Figure 3. Charge Injection

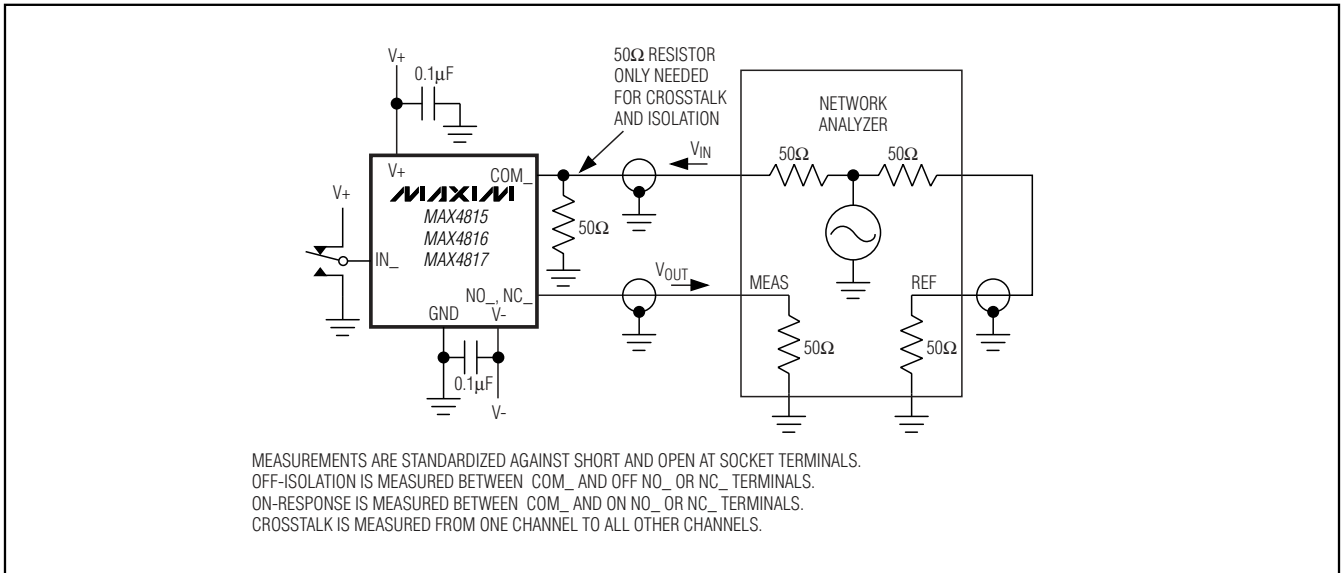


Figure 4. On-Loss, Off-Isolation, and Crosstalk

High-Bandwidth, T1/E1, SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

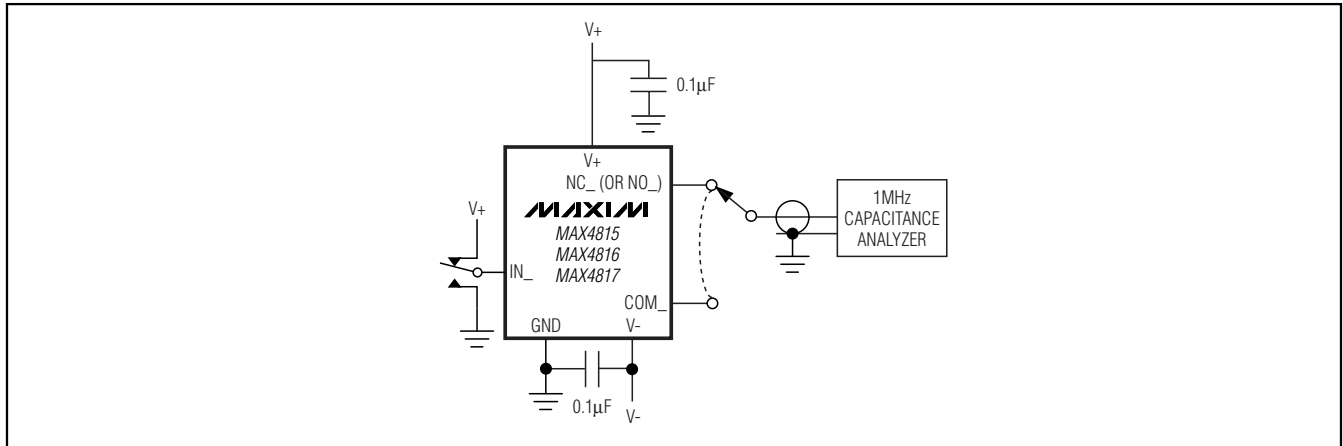


Figure 5. Channel Off-/On-Capacitance

MAX4815/MAX4816/MAX4817

High-Bandwidth, T1/E1, SPST Analog Switches

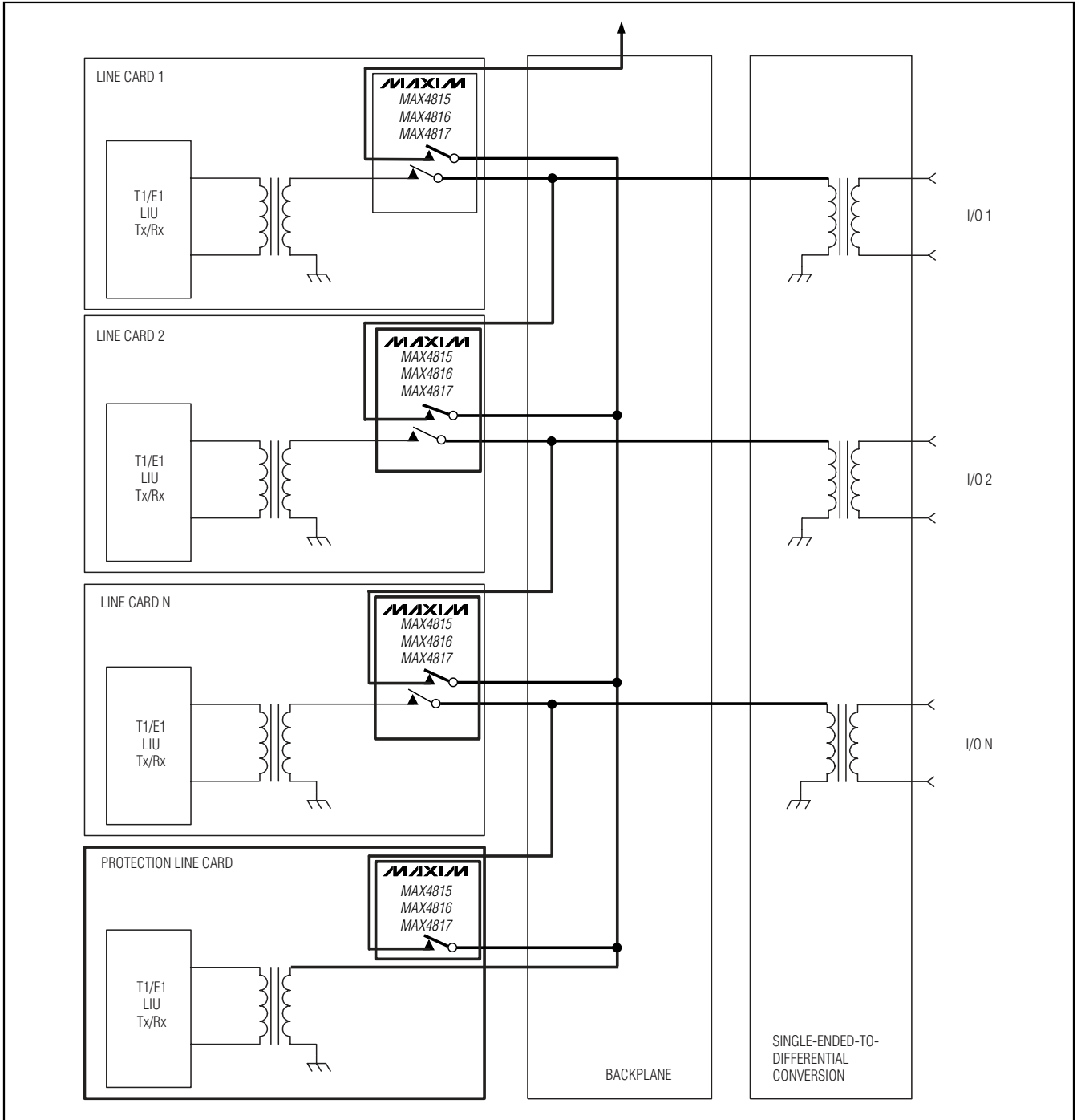


Figure 6. Adjacent Line-Card Protection Architecture with Switches in the Line Cards for Twisted Pair Cable (120Ω E1, or 100Ω T1). Figure for coaxial cable (75Ω E1) is the same without the single-ended-to-differential conversion.

High-Bandwidth, T1/E1, SPST Analog Switches

MAX4815/MAX4816/MAX4817

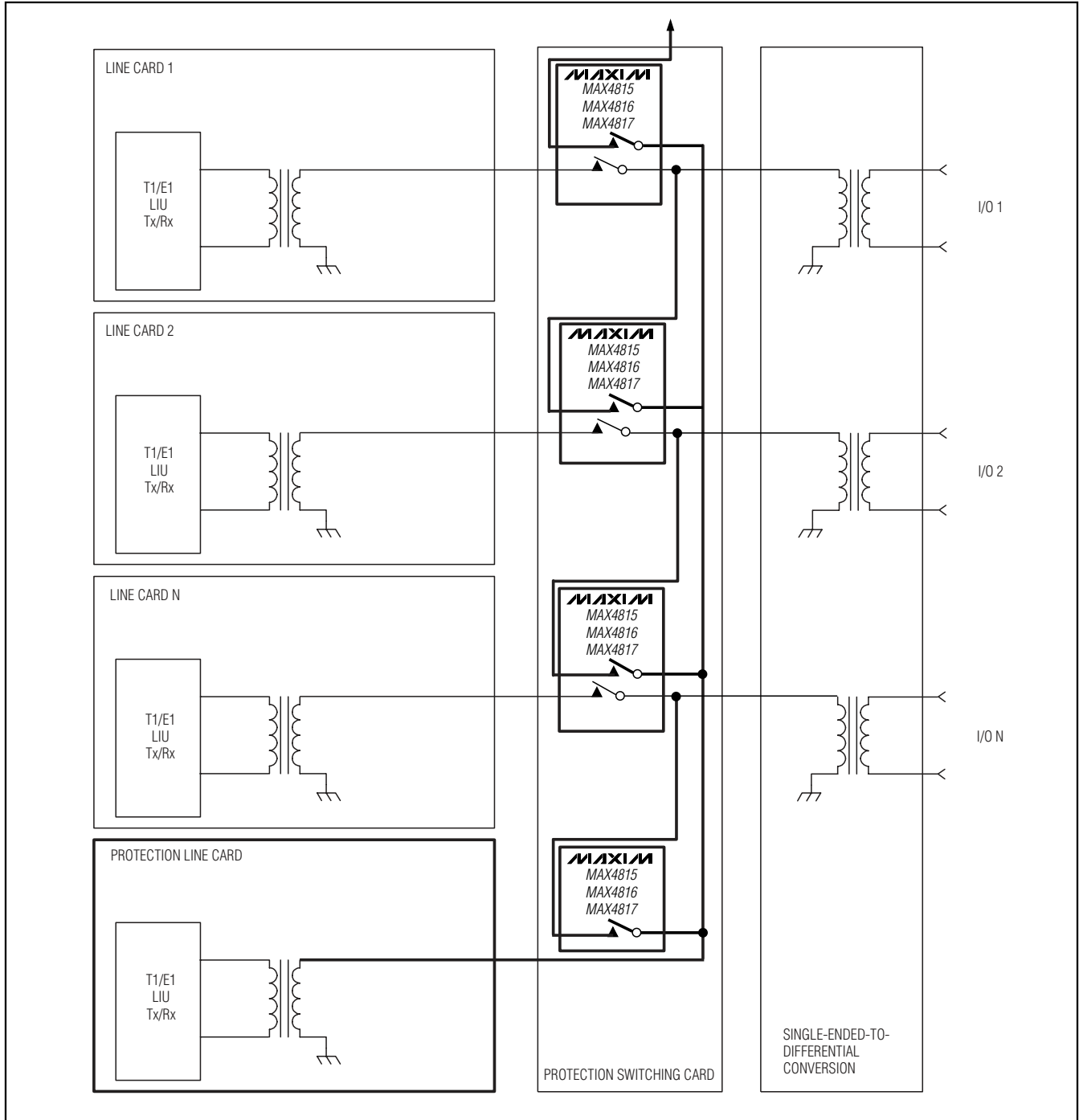
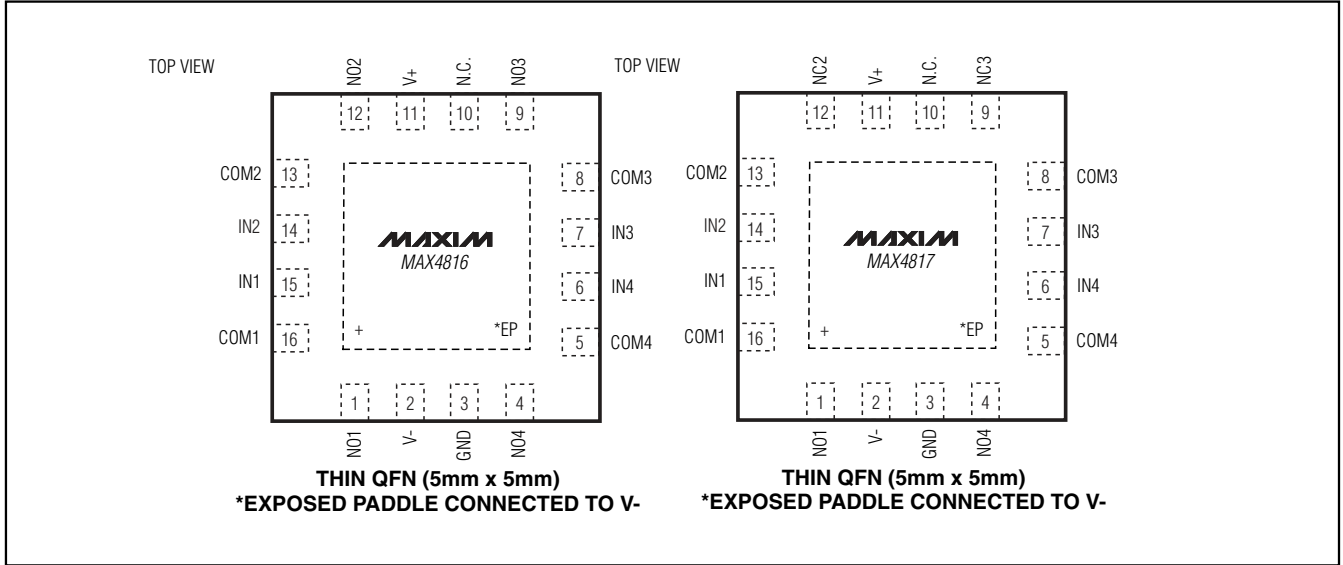


Figure 7. Adjacent Line-Card Protection Architecture with Switches out of the Line Cards for Twisted Pair Cable (120Ω E1, or 100Ω T1). Figure for coaxial cable (75Ω E1) is the same without the single-ended-to-differential conversion.

High-Bandwidth, T1/E1, SPST Analog Switches

Pin Configurations (continued)



Chip Information

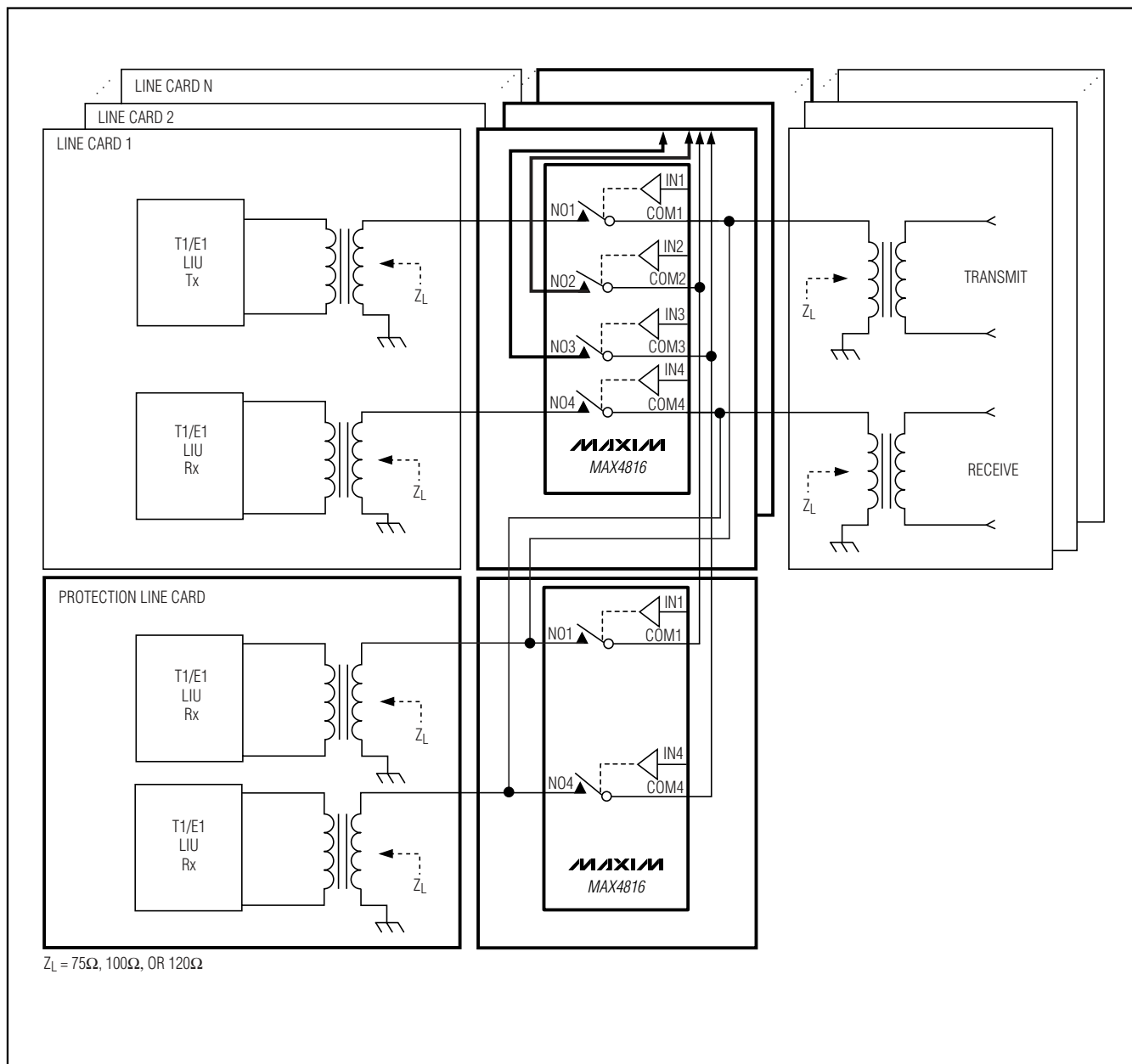
PROCESS: BiCMOS

CONNECT EXPOSED PADDLE TO V-.

High-Bandwidth, T1/E1, SPST Analog Switches

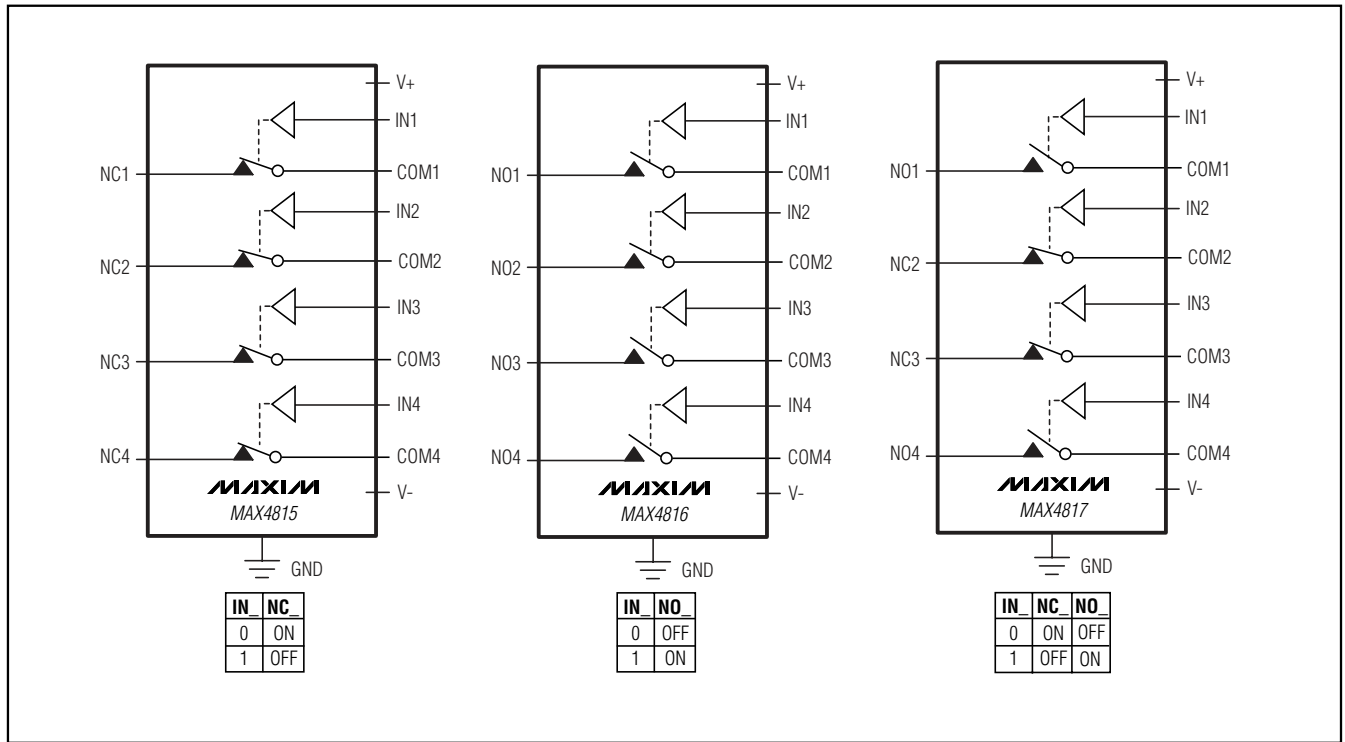
Typical Operating Circuit

MAX4815/MAX4816/MAX4817



High-Bandwidth, T1/E1, SPST Analog Switches

Functional Diagram

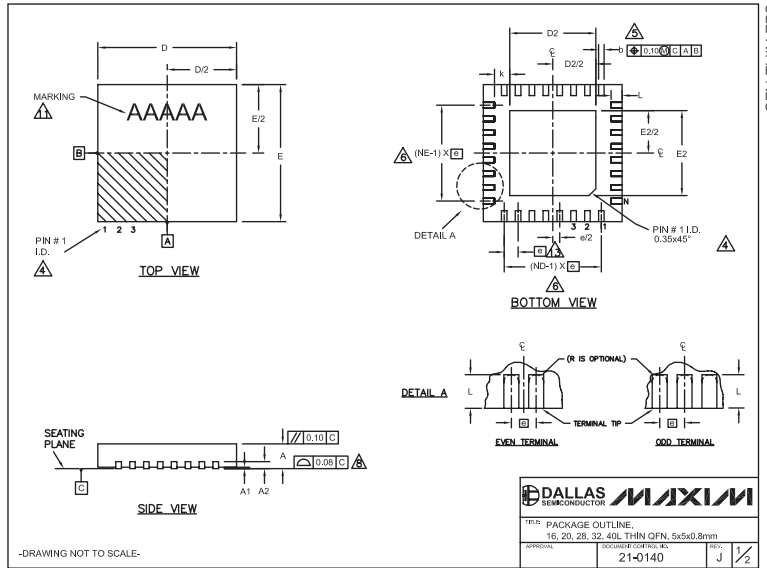


High-Bandwidth, T1/E1, SPST Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4815/MAX4816/MAX4817



| COMMON DIMENSIONS | | | | | | | | | | EXPOSED PAD VARIATIONS | | | | | | | | | | | | | | |
|-------------------|-----------|------|-----------|------|-----------|------|-----------|------|-----------|------------------------|-----------|------|----------|------|------|---------|------|---------|------|------|------|------|------|------|
| PKG | 16L 5x5 | | 20L 5x5 | | 28L 5x5 | | 32L 5x5 | | 40L 5x5 | | PKG CODES | D2 | | E2 | | | | | | | | | | |
| SYMBOL | MIN | NOM | MAX | MIN | NOM | MAX | MIN | NOM | MAX | MIN | NOM | MAX | MIN | NOM | MAX | | | | | | | | | |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | T1655-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | | | | |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | T1655-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | | | | |
| A2 | 0.20 REF. | | 0.20 REF. | | 0.20 REF. | | 0.20 REF. | | 0.20 REF. | | T1655N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | T2055-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 | T2055-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | T2055-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | |
| E | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | T2855-3 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | |
| e | 0.80 BSC. | | 0.65 BSC. | | 0.50 BSC. | | 0.50 BSC. | | 0.40 BSC. | | T2855-4 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | T2855-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| k | 0.25 | - | 0.25 | - | 0.25 | - | 0.25 | - | 0.25 | - | 0.25 | - | T2855-6 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | | | | |
| L | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 | T2855-7 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | | |
| ND | 16 | 16 | 20 | 20 | 28 | 28 | 32 | 32 | 40 | | | | T2855-8 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | | | | |
| NE | 4 | 4 | 5 | 5 | 7 | 7 | 8 | 8 | 10 | | | | T3255N-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 | | | | | |
| JEDEC | WH1B | | WH1C | | WH1D-1 | | WH1D-2 | | --- | | T3255-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | T3255-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| | | | | | | | | | | | | | T3255-5 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | | | | |
| | | | | | | | | | | | | | T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 | | | | | |
| | | | | | | | | | | | | | T4055-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 | | | | | |
| | | | | | | | | | | | | | T4055-2 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 | | | | | |

NOTES:
 1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
 2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
 3. N IS THE TOTAL NUMBER OF TERMINALS.
 4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 98-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
 5. DIMENSION 5 APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
 6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
 7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
 8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
 9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
 10. WARPAGE SHALL NOT EXCEED 0.10 mm.
 11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
 12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
 13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
 PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
 21-0140

Revision History

Pages changed at Rev 2: 1, 9, 17

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 17

© 2007 Maxim Integrated Products MAXIM is a registered trademark of Maxim Integrated Products, Inc.