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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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P-CHANNEL MOS FET FOR HIGH-SPEED SWITCH

The 2SJ358 is a P-channel vertical MOS FET that can be used as a switching element. The 2SJ358 can be directly driven by an IC operating at 5 V.

The 2SJ358 features a low on-resistance and excellent switching characteristics, and is suitable for applications such as actuator driver and DC/DC converter.

FEATURES

- New-type compact package
Has advantages of packages for small signals and for power transistors, and compensates those disadvantages
- Can be directly driven by an IC operating at 5 V.
- Low on-resistance
 $R_{DS(ON)} = 0.40 \Omega \text{ MAX. @ } V_{GS} = -4 \text{ V, } I_D = -1.5 \text{ A}$
 $R_{DS(ON)} = 0.30 \Omega \text{ MAX. @ } V_{GS} = -10 \text{ V, } I_D = -1.5 \text{ A}$

QUALITY GRADE

Standard

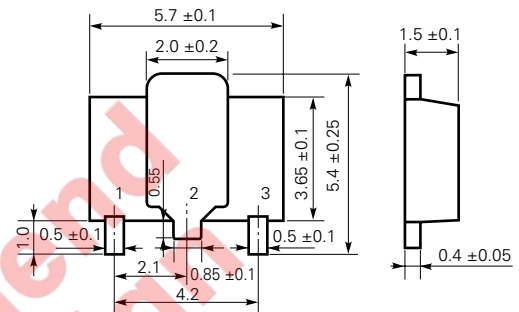
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C)

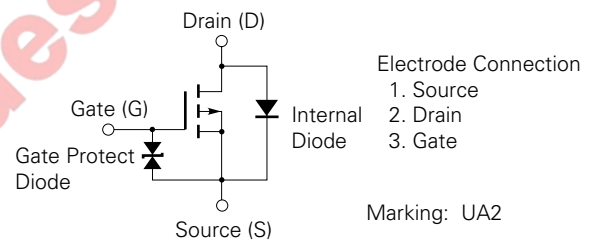
| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------|-----------------------|--|-------------|------|
| Drain-Source Voltage | V _{DSS} | V _{GS} = 0 | -60 | V |
| Gate-Source Voltage | V _{GSS} | V _{DS} = 0 | -20/+10 | V |
| Drain Current (DC) | I _{D(DC)} | | -/+3.0 | A |
| Drain Current (Pulse) | I _{D(pulse)} | PW ≤ 10 ms Duty Cycle ≤ 1 % | -/+6.0 | A |
| Total Power Loss | P _T | Mounted on ceramic board of 7.5 cm ² × 0.7 mm | 2.0 | W |
| Channel Temperature | T _{ch} | | 150 | °C |
| Storage Temperature | T _{stg} | | -55 to +150 | °C |

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Package Drawings (unit: mm)



Equivalent Circuit

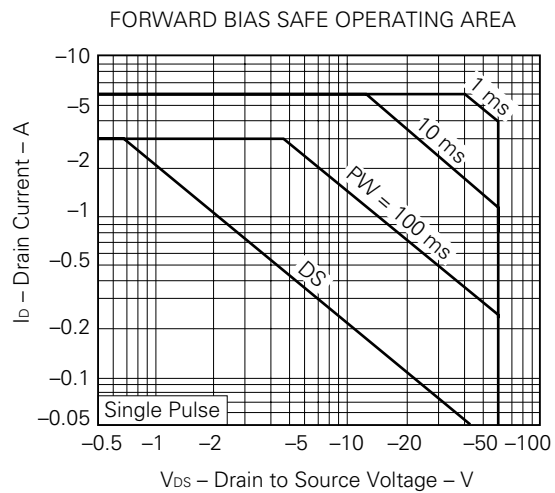
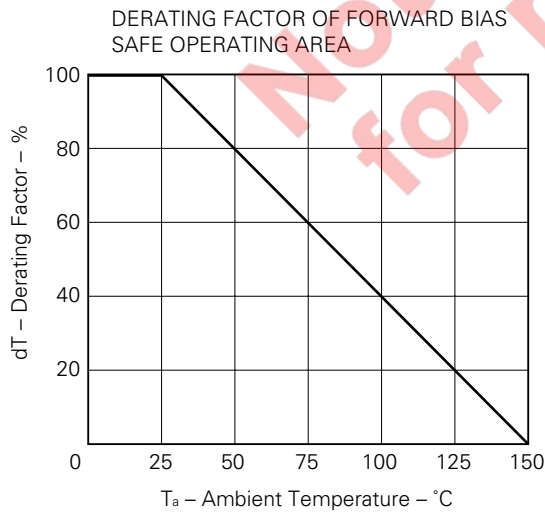


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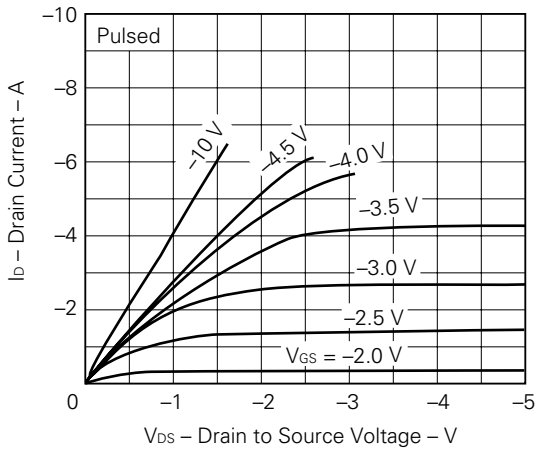
ELECTRICAL SPECIFICATIONS (T_a = +25 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|----------------------|--|------|------|-------|------|
| Drain Shut-down Current | I _{DSS} | V _{DS} = -60 V, V _{GS} = 0 | | | -10 | μA |
| Gate Leak Current | I _{GSS} | V _{GS} = -16/+10 V, V _{DS} = 0 | | | -/+10 | μA |
| Gate Cutoff Voltage | V _{GS(off)} | V _{DS} = -10 V, I _D = -1 mA | -1.0 | -1.4 | -2.0 | V |
| Forward Transfer Admittance | Y _{fs1} | V _{DS} = -10 V, I _D = -1.0 A | 1.8 | | | S |
| Drain-Source On-Resistance | R _{DS(on)1} | V _{GS} = -4 V, I _D = -1.5 A | | 0.29 | 0.40 | Ω |
| Drain-Source On-Resistance | R _{DS(on)2} | V _{GS} = -10 V, I _D = -1.5 A | | 0.18 | 0.30 | Ω |
| Input Capacitance | C _{iss} | V _{DS} = -10 V, V _{GS} = 0, | | 600 | | pF |
| Output Capacitance | C _{oss} | f = 1.0 MHz | | 300 | | pF |
| Feedback Capacitance | C _{rss} | | | 120 | | pF |
| On-Time Delay | t _{d(on)} | V _{DD} = -25 V, I _D = -1.5 A | | 6 | | ns |
| Rise Time | t _r | V _{GS(on)} = -10 V | | 35 | | ns |
| Off-Time Delay | t _{d(off)} | R _G = 10 Ω, R _L = 17 Ω | | 155 | | ns |
| Fall Time | t _f | | | 95 | | ns |
| Gate Input Charge | Q _G | V _{DS} = -48 V, | | 23.9 | | nC |
| Gate-Source Charge | Q _{GS} | V _{GS} = -10 V, | | 1.5 | | nC |
| Gate-Drain Charge | Q _{GD} | I _D = -3.1 A, I _G = -2 mA | | 8.1 | | nC |
| Internal Diode Reverse Recovery Time | t _{rr} | I _F = 3.0 A di/dt = 50 A/μs | | 95 | | ns |
| Internal Diode Reverse Recovery Charge | Q _{rr} | | | 118 | | nC |

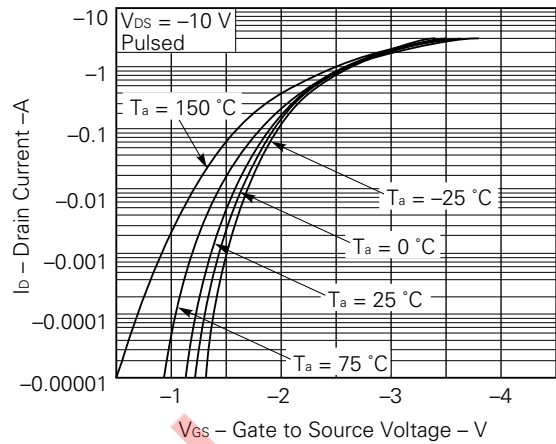
CHARACTERISTICS CURVES (T_a = +25 °C)



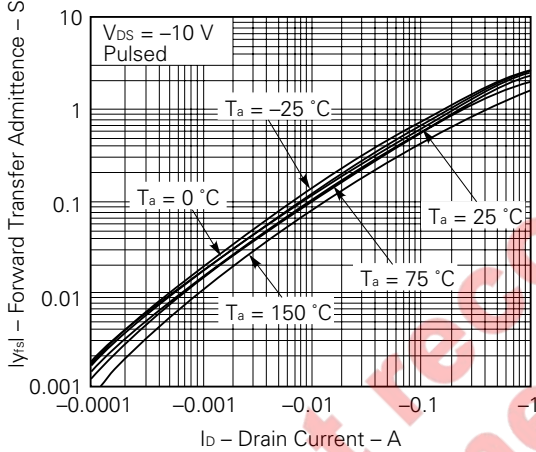
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



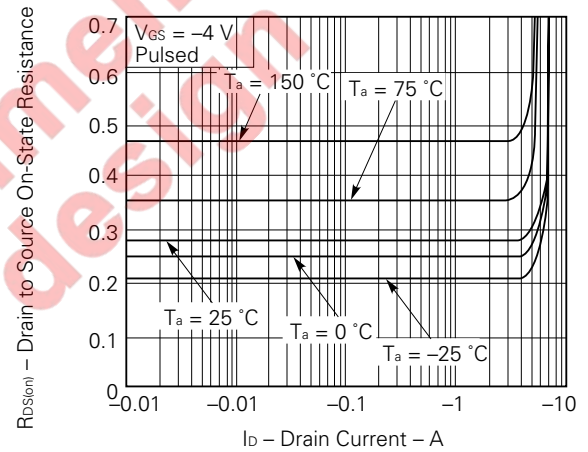
TRANSFER CHARACTERISTICS



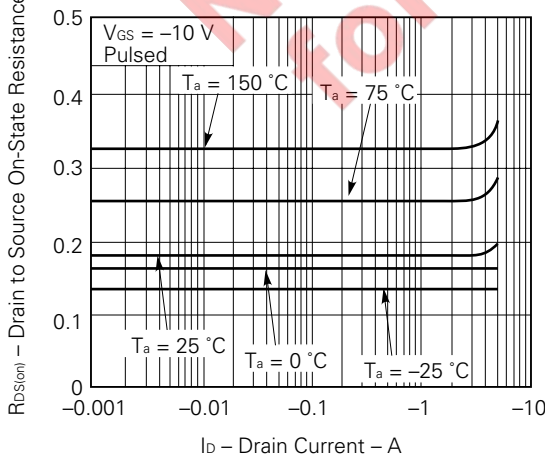
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



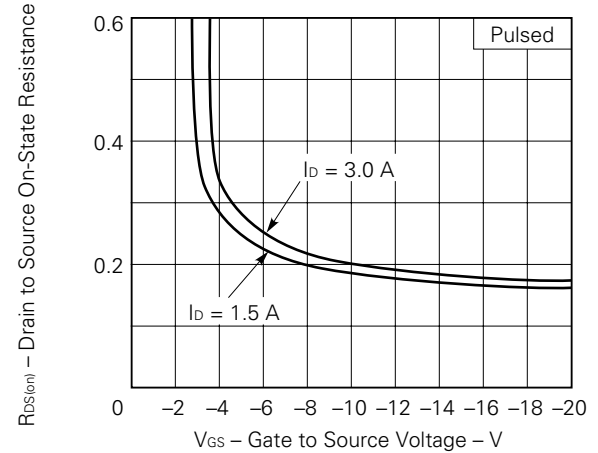
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



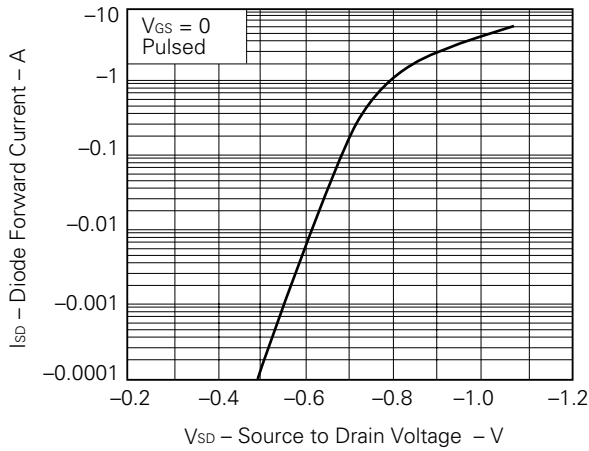
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



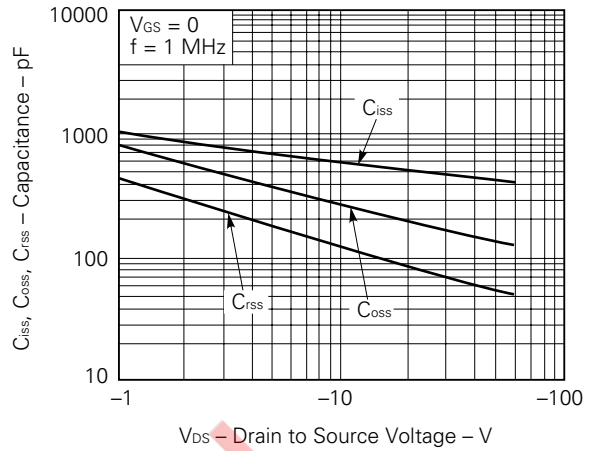
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



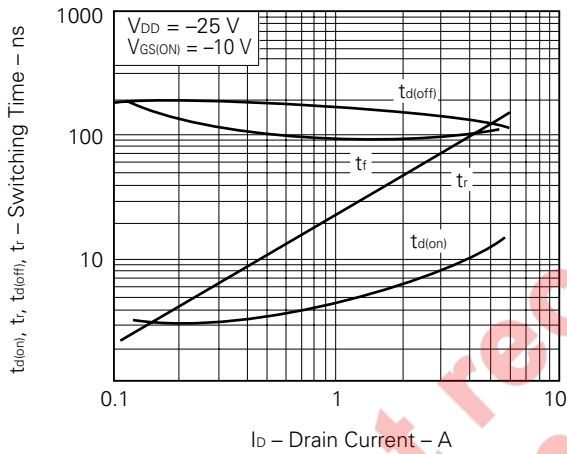
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



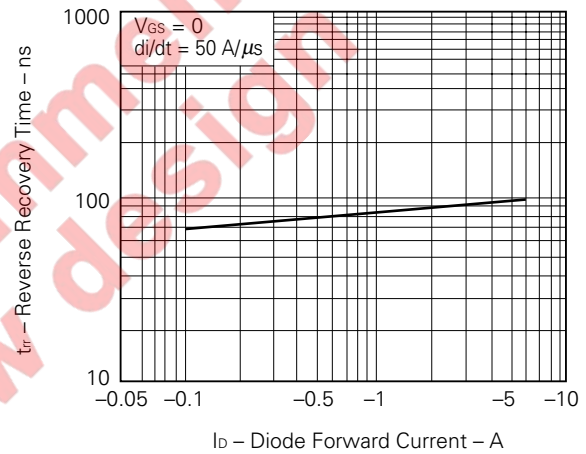
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



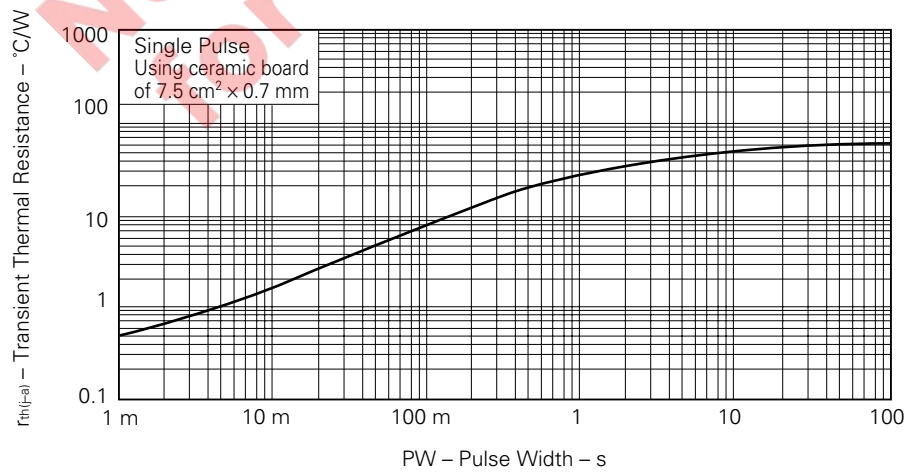
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



RELATED DOCUMENTS

| Document Name | Document No. |
|---|--------------|
| Semiconductor Device Mounting Technology Manual | IEI-1207 |
| NEC Semiconductor Device Reliability/Quality Control System | TEI-1202 |
| Guide to Quality Assurance for Semiconductor Device | MEI-1202 |

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