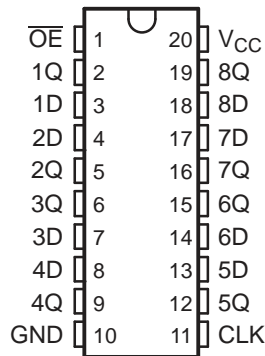
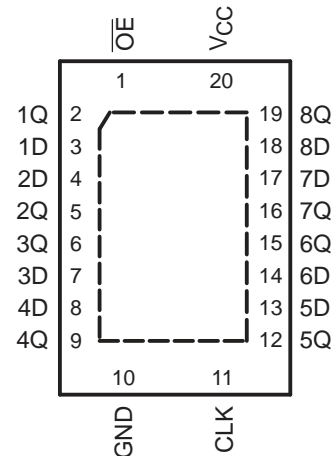


## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

Check for Samples: [SN74LV374AT](#)

### FEATURES

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Typical  $t_{pd}$  of 4.9 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**DB, DW, NS, OR PW PACKAGE  
(TOP VIEW)**

**RGY PACKAGE  
(TOP VIEW)**


### DESCRIPTION

The SN74LV374AT is an octal edge-triggered D-type flip-flop. This device features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

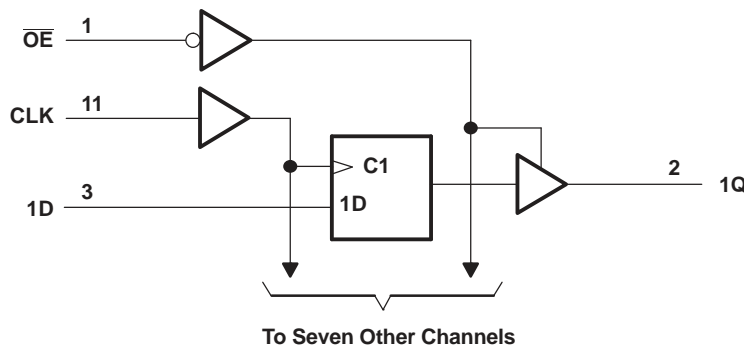
**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	QFN – RGY	Reel of 1000	SN74LV374ATRGYR	VV374
	SOIC – DW	Tube of 25	SN74LV374ATDW	LV374AT
		Reel of 2000	SN74LV374ATDWR	
	SOP – NS	Reel of 2000	SN74LV374ATNSR	74LV374AT
	SSOP – DB	Reel of 2000	SN74LV374ATDBR	LV374AT
	TSSOP – PW	Tube of 70	SN74LV374ATPW	LV374AT
		Reel of 2000	SN74LV374ATPWR	
		Tube of 250	SN74LV374ATPWT	

**FUNCTION TABLE  
(EACH FLIP-FLOP)**

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	
$V_O$	Output voltage range <sup>(2) (3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		$\pm 20$ mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		$\pm 50$ mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		$\pm 35$ mA
	Continuous current through $V_{CC}$ or GND			$\pm 70$ mA
$\theta_{JA}$	Package thermal impedance	DB package <sup>(4)</sup>		70
		DW package <sup>(4)</sup>		58
		NS package <sup>(4)</sup>		60
		PW package <sup>(4)</sup>		83
		RGY package <sup>(5)</sup>		37
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V		V
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	High or low state		0 $V_{CC}$
		3-state		0 5.5
$I_{OH}$	High-level output current	$V_{CC} = 4.5$ V to 5.5 V		-16 mA
$I_{OL}$	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V		16 mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 4.5$ V to 5.5 V		20 ns/V
$T_A$	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		T <sub>A</sub> = –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I <sub>OH</sub> = –16 mA	4.5 V	3.8			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0	0.1		0.1		V	
	I <sub>OL</sub> = 16 mA	4.5 V			0.55		0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±0.1		±1		μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20		μA	
ΔI <sub>CC</sub> <sup>(1)</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			40		50		μA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			0.5		5		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			4					pF	

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		T <sub>A</sub> = –40°C to 85°C		T <sub>A</sub> = –40°C to 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub> Clock frequency	C <sub>L</sub> = 15 pF		90		80		70	MHz
	C <sub>L</sub> = 50 pF		85		75		65	
t <sub>w</sub> Pulse duration, CLK high or low		6.5		8.5		8.5		ns
t <sub>su</sub> Setup time, data before CLK↑		2.5		2.5		5		ns
t <sub>h</sub> Hold time, data after CLK↑		2.5		2.5		2.5		ns

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		T <sub>A</sub> = –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			C <sub>L</sub> = 15 pF	90	140		80		70	MHz	
			C <sub>L</sub> = 50 pF	85	150		75		65		
t <sub>pd</sub>	CLK	Q	C <sub>L</sub> = 15 pF	3	4.9	8.1	1	10.5	1	11	ns
t <sub>en</sub>	$\overline{OE}$	Q		3.2	4.6	7.6	1	11.5	1	12	
t <sub>dis</sub>	$\overline{OE}$	Q		1.7	3.4	6.8	1	8	1	9	
t <sub>pd</sub>	CLK	Q	C <sub>L</sub> = 50 pF	4.2	5.9	10.1	1	11.5	1	13	ns
t <sub>en</sub>	$\overline{OE}$	Q		4.5	5.5	9.6	1	12.5	1	13	
t <sub>dis</sub>	$\overline{OE}$	Q		2.4	4	8.8	1	12	1	12.5	
t <sub>sk(o)</sub>							1		1	1	

**NOISE CHARACTERISTICS<sup>(1)</sup>**
 $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ 

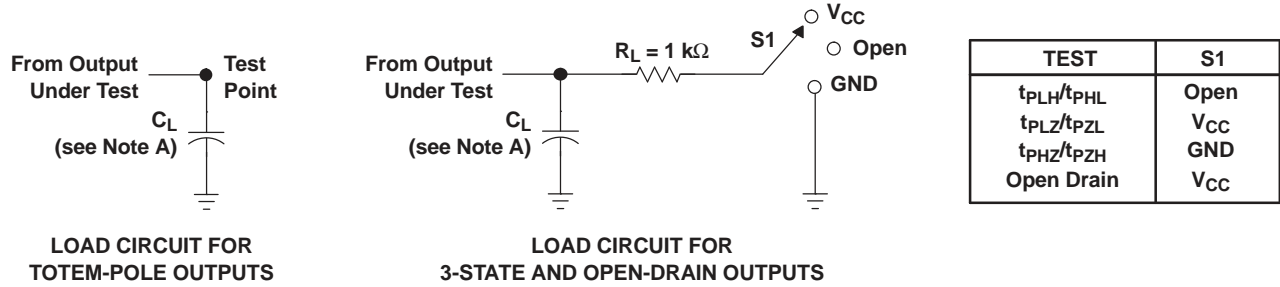
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		1.3	1.6	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.3	-1.65	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

**OPERATING CHARACTERISTICS**
 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

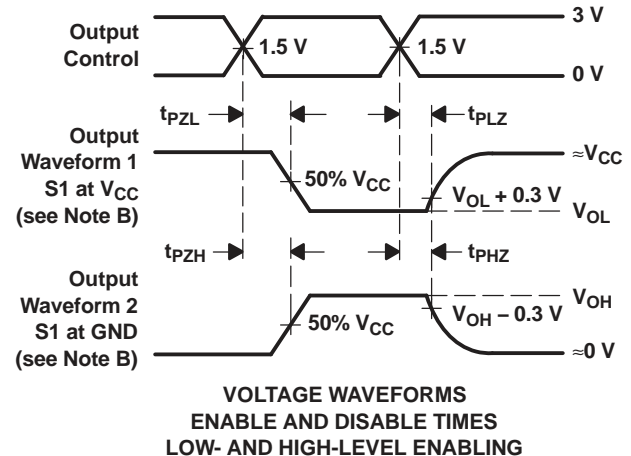
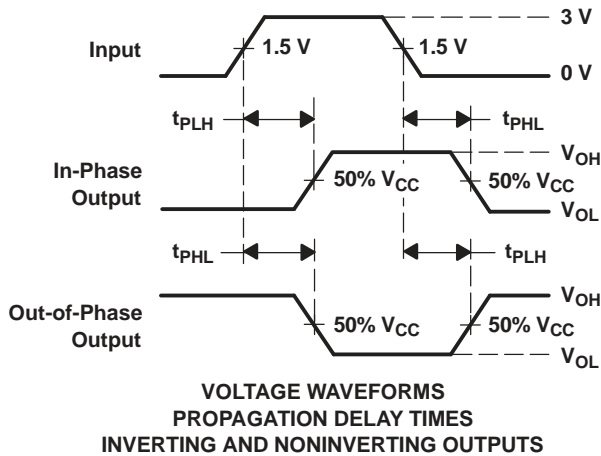
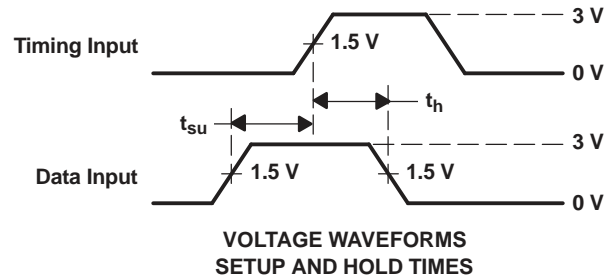
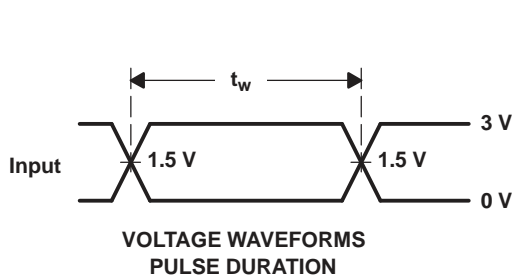
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	42.5	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV374ATDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV374AT	<a href="#">Samples</a>
SN74LV374ATNSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV374AT	<a href="#">Samples</a>
SN74LV374ATPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV374AT	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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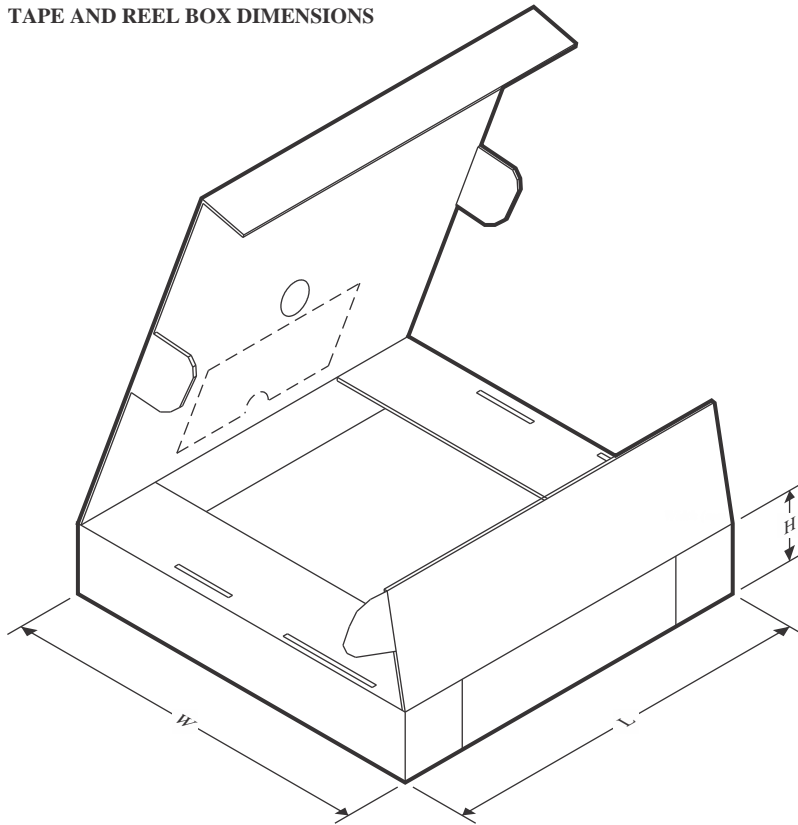


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

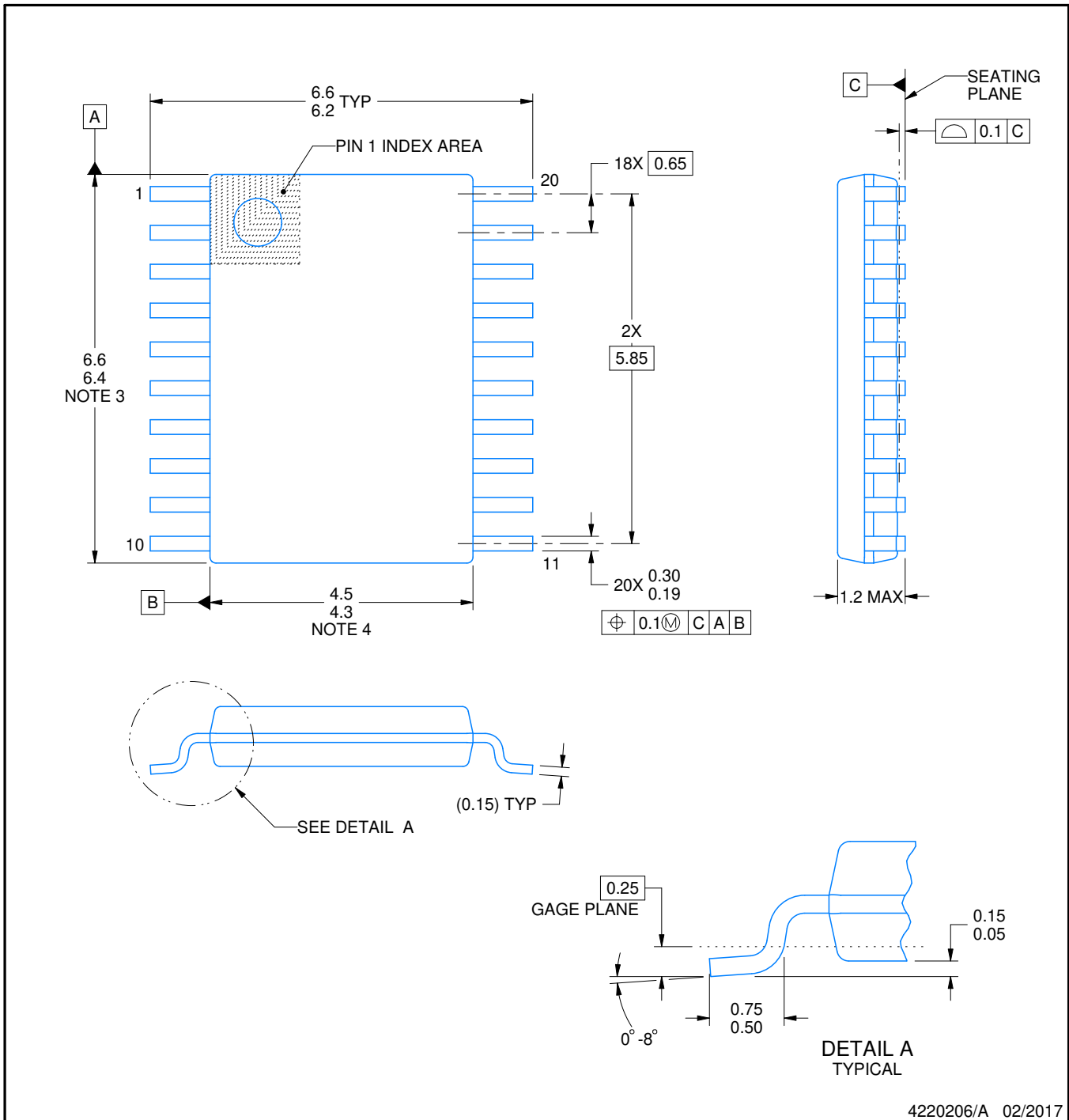

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV374ATDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV374ATNSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV374ATPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV374ATDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV374ATNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV374ATPWR	TSSOP	PW	20	2000	356.0	356.0	35.0



4220206/A 02/2017

NOTES:

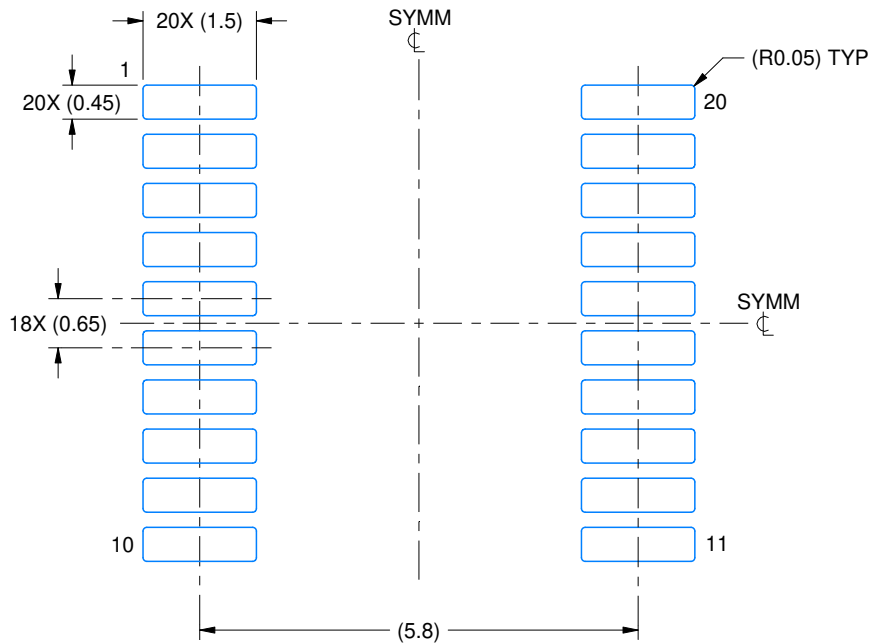
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

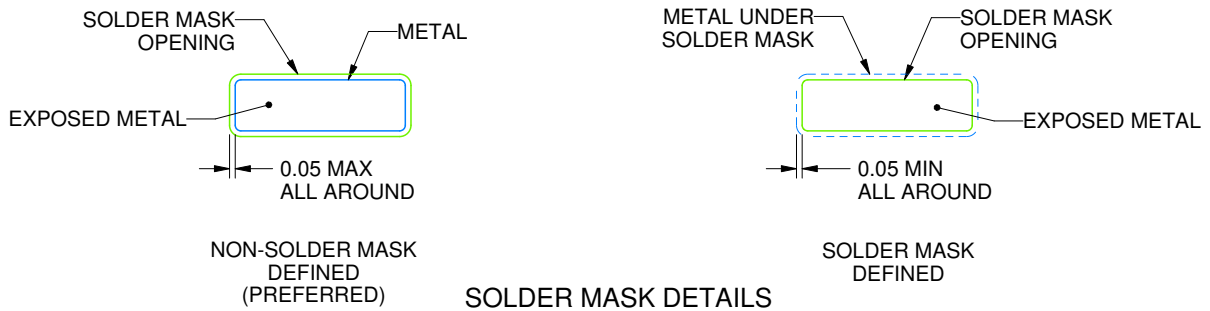
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

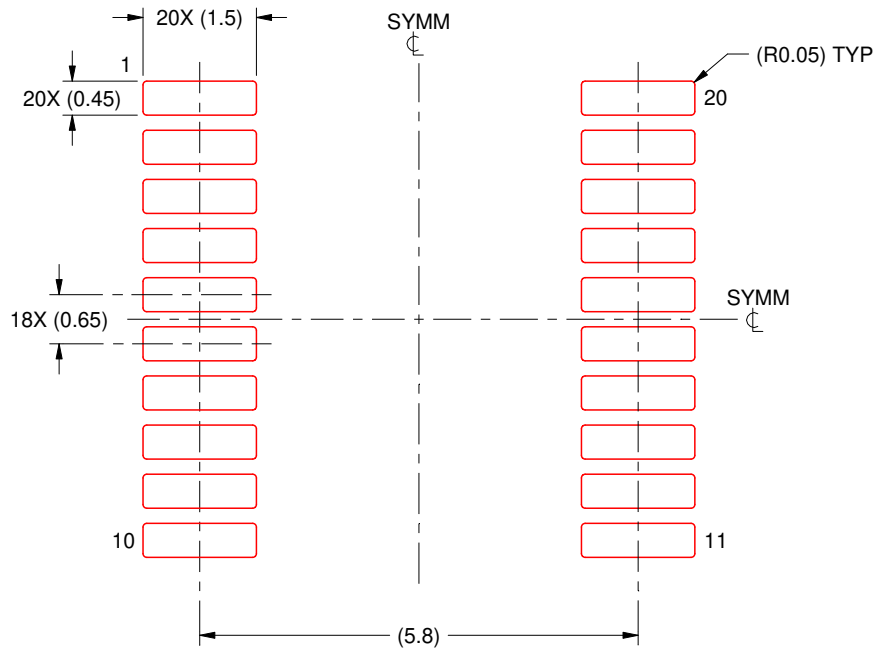
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

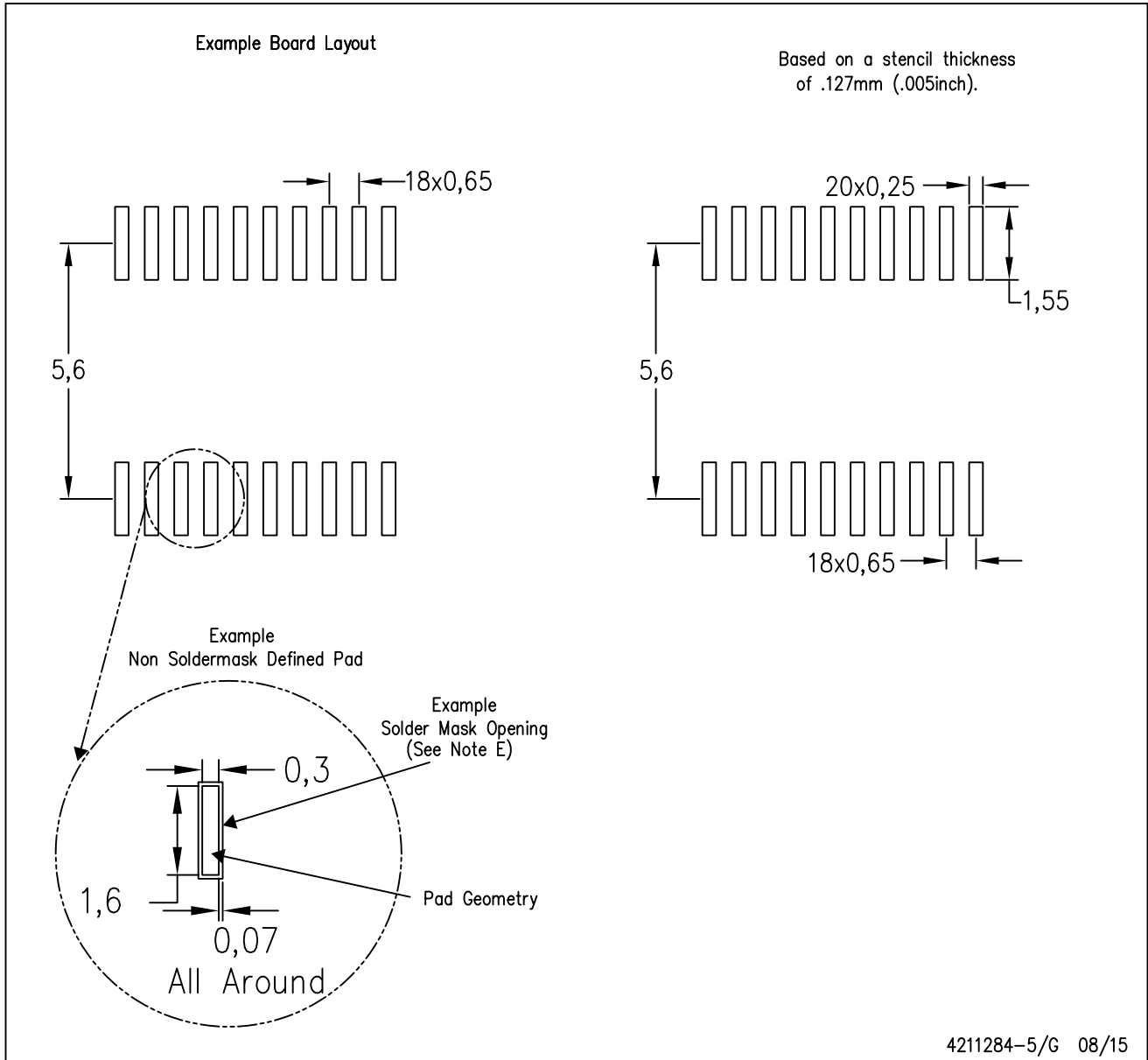
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



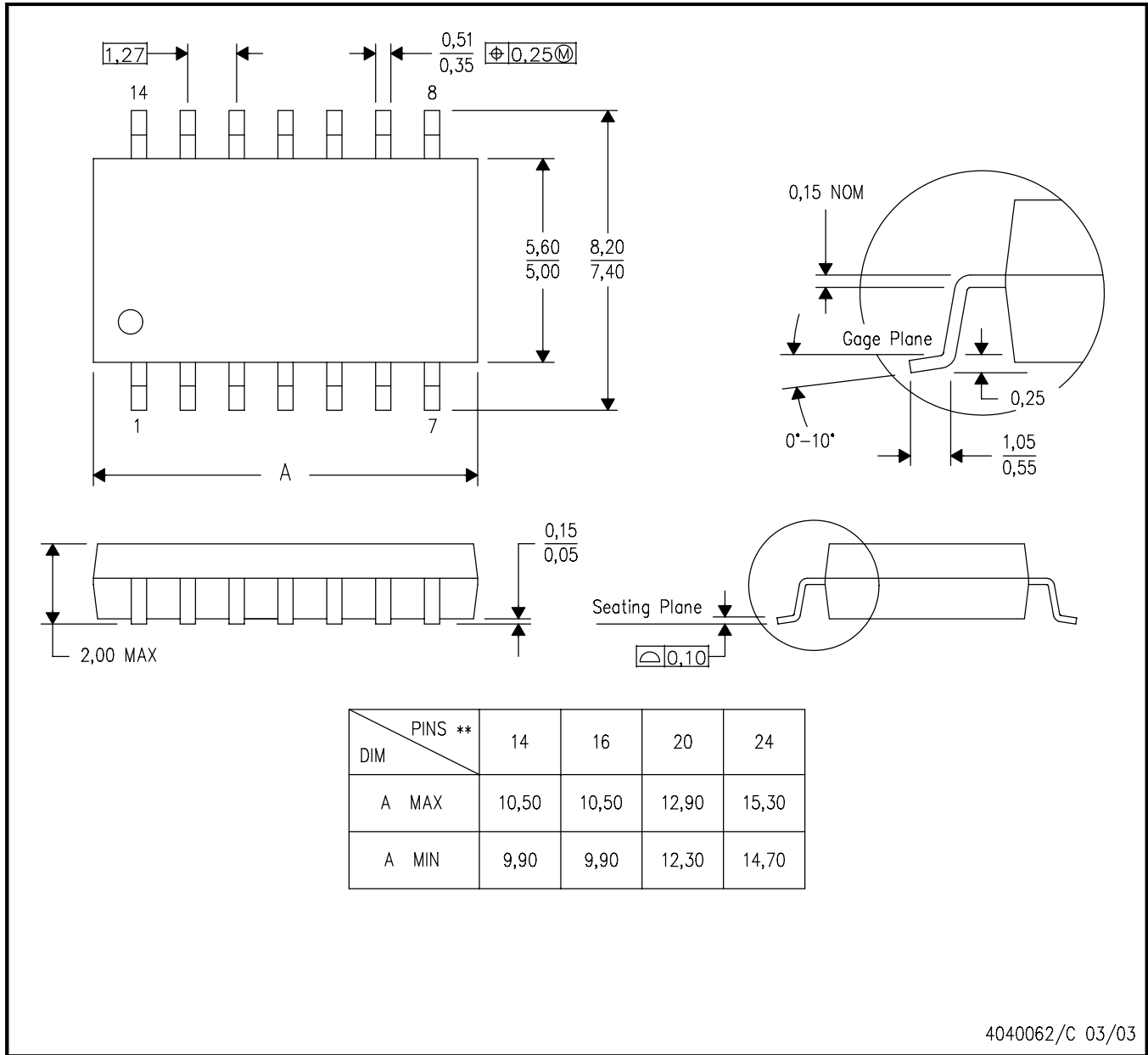
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

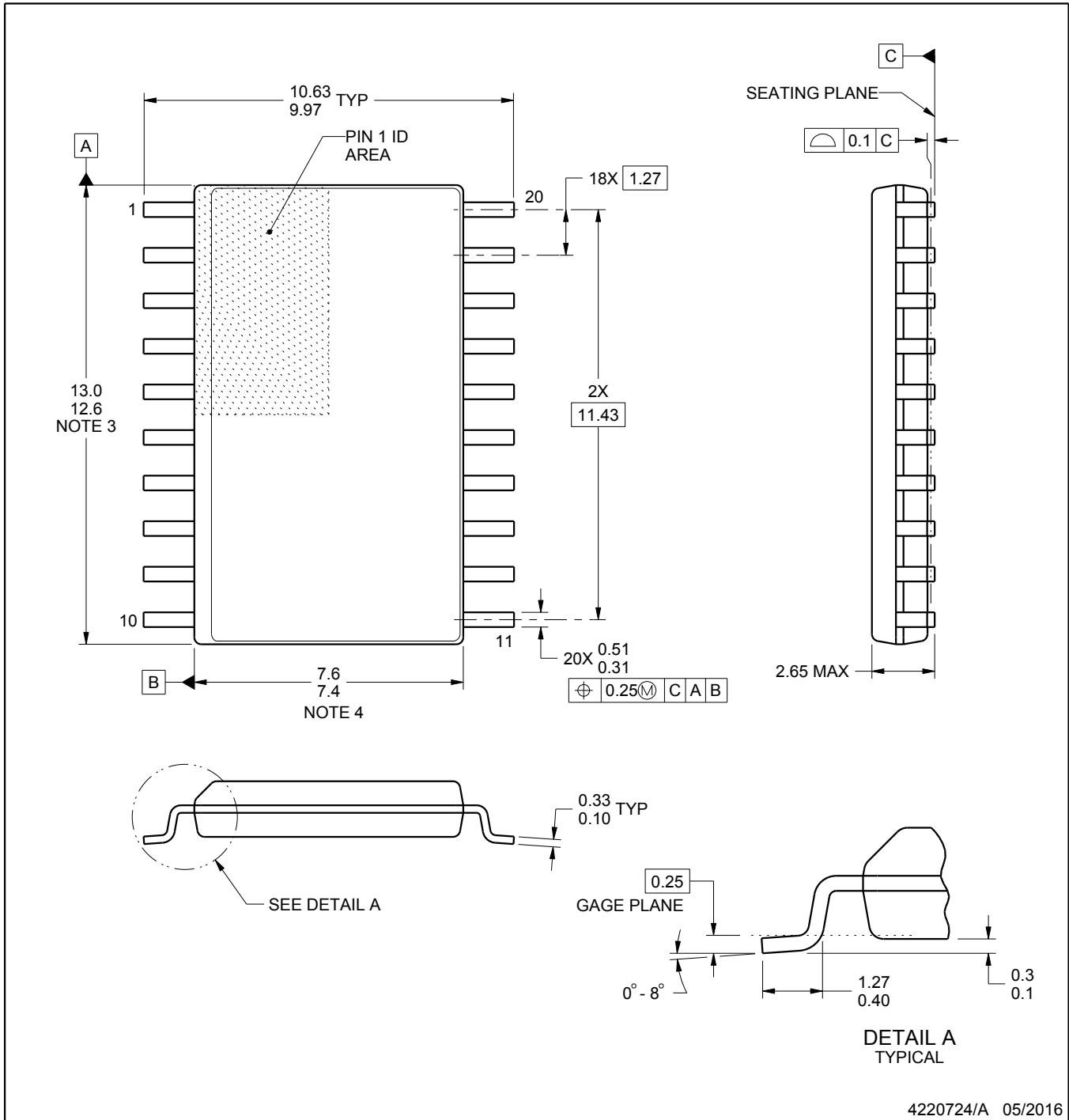
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

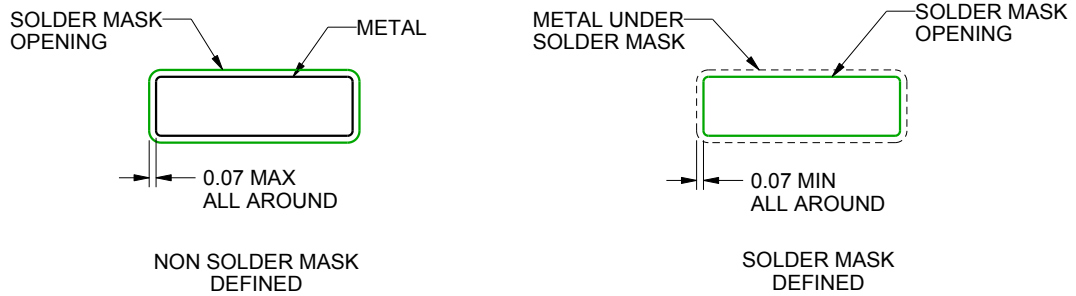
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

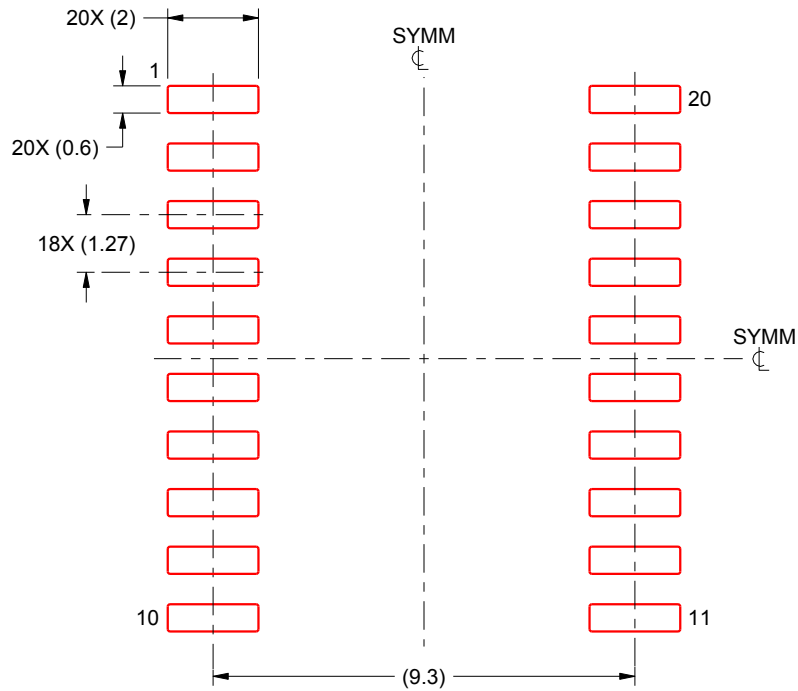
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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