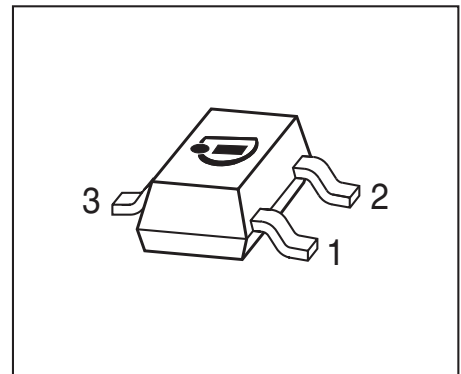


PNP Silicon AF Transistor

- Low collector-emitter saturation voltage
- Complementary type: SMBTA06 / MMBTA06(NPN)
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101



Type	Marking	Pin Configuration			Package
SMBTA56/MMBTA56	s2G	1=B	2=E	3=C	SOT23

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	80	V
Collector-base voltage	V_{CBO}	80	
Emitter-base voltage	V_{EBO}	4	
Collector current	I_C	500	mA
Peak collector current, $t_p \leq 10$ ms	I_{CM}	1	A
Base current	I_B	100	mA
Peak base current	I_{BM}	200	
Total power dissipation- $T_S \leq 79^\circ\text{C}$	P_{tot}	330	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}	≤ 215	K/W

¹⁾For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

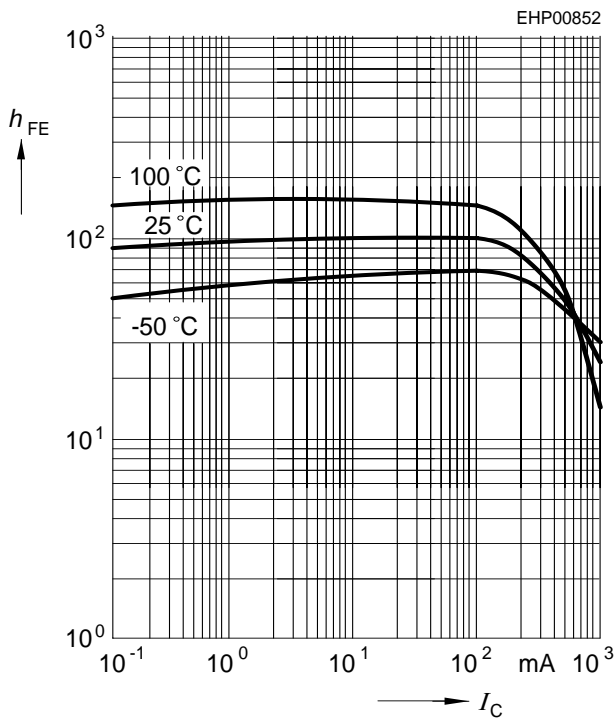
Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage $I_C = 1\text{ mA}, I_B = 0$	$V_{(BR)CEO}$	80	-	-	V
Collector-base breakdown voltage $I_C = 100\text{ }\mu\text{A}, I_E = 0$	$V_{(BR)CBO}$	80	-	-	
Emitter-base breakdown voltage $I_E = 10\text{ }\mu\text{A}, I_C = 0$	$V_{(BR)EBO}$	4	-	-	
Collector-base cutoff current $V_{CB} = 80\text{ V}, I_E = 0$ $V_{CB} = 80\text{ V}, I_E = 0, T_A = 150^\circ\text{C}$	I_{CBO}	-	-	0.1 20	μA
Collector-emitter cutoff current $V_{CE} = 60\text{ V}, I_B = 0$	I_{CEO}	-	-	0.1	
DC current gain ¹⁾ $I_C = 10\text{ mA}, V_{CE} = 1\text{ V}$ $I_C = 100\text{ mA}, V_{CE} = 1\text{ V}$	h_{FE}	100 100	- -	- -	-
Collector-emitter saturation voltage ¹⁾ $I_C = 100\text{ mA}, I_B = 10\text{ mA}$	V_{CEsat}	-	-	0.25	V
Base-emitter voltage ¹⁾ $I_C = 100\text{ mA}, V_{CE} = 1\text{ V}$	$V_{BE(ON)}$	-	-	1.2	
AC Characteristics					
Transition frequency $I_C = 20\text{ mA}, V_{CE} = 5\text{ V}, f = 20\text{ MHz}$	f_T	-	100	-	MHz
Collector-base capacitance $V_{CB} = 10\text{ V}, f = 1\text{ MHz}$	C_{cb}	-	7	-	pF

¹⁾Pulse test: $t < 300\mu\text{s}$; $D < 2\%$

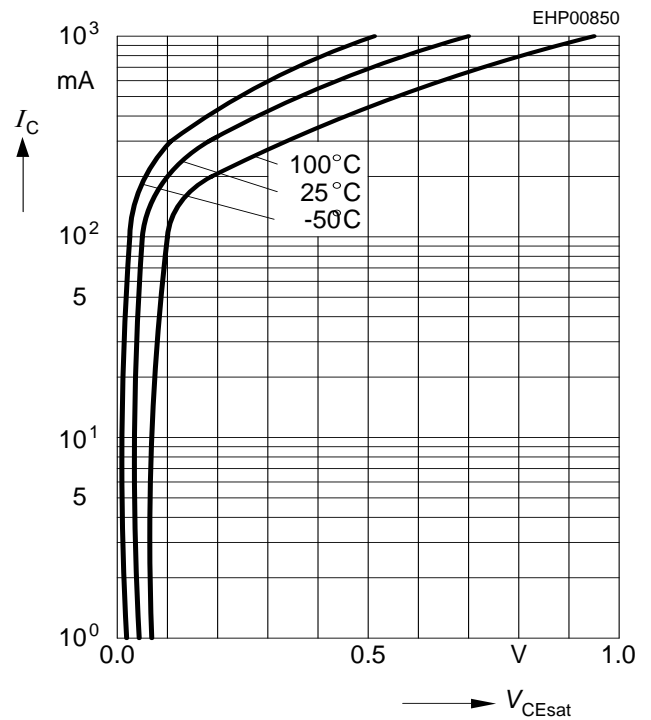
DC current gain $h_{FE} = f(I_C)$

$V_{CE} = 1\text{ V}$



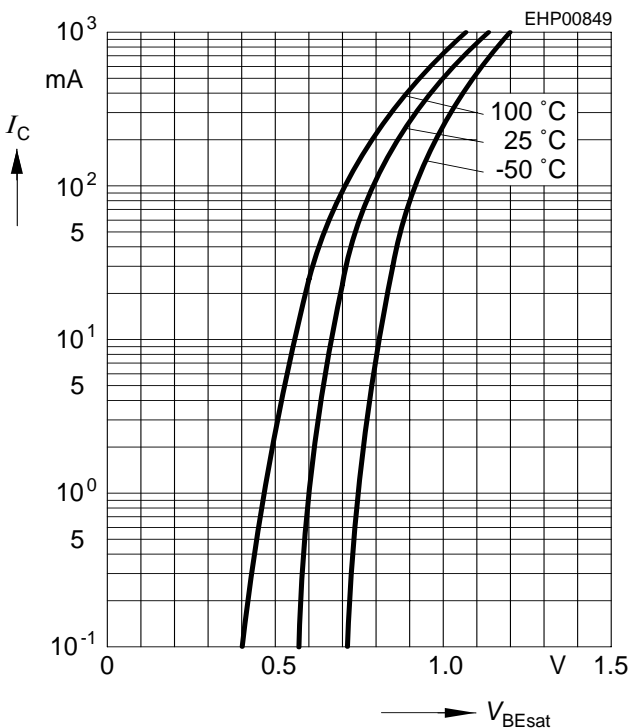
Collector-emitter saturation voltage

$I_C = f(V_{CEsat}), h_{FE} = 10$



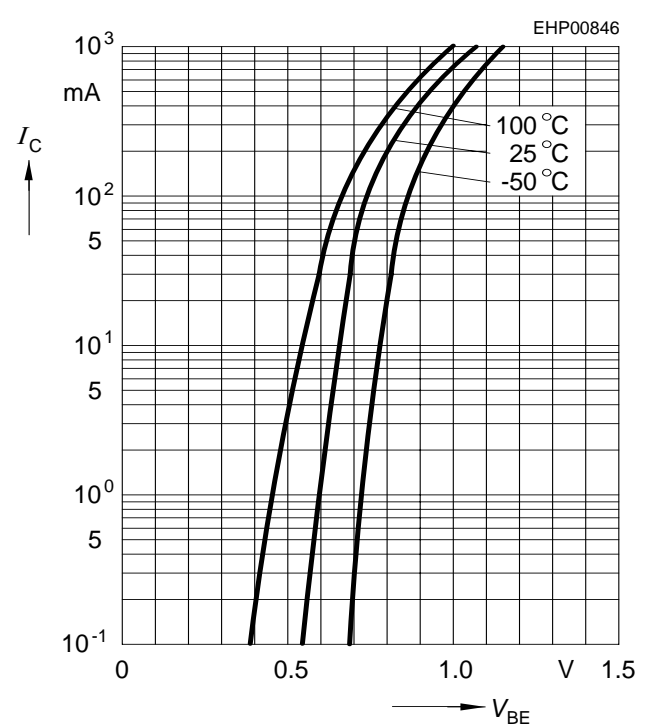
Base-emitter saturation voltage

$I_C = f(V_{BEsat}), h_{FE} = 10$



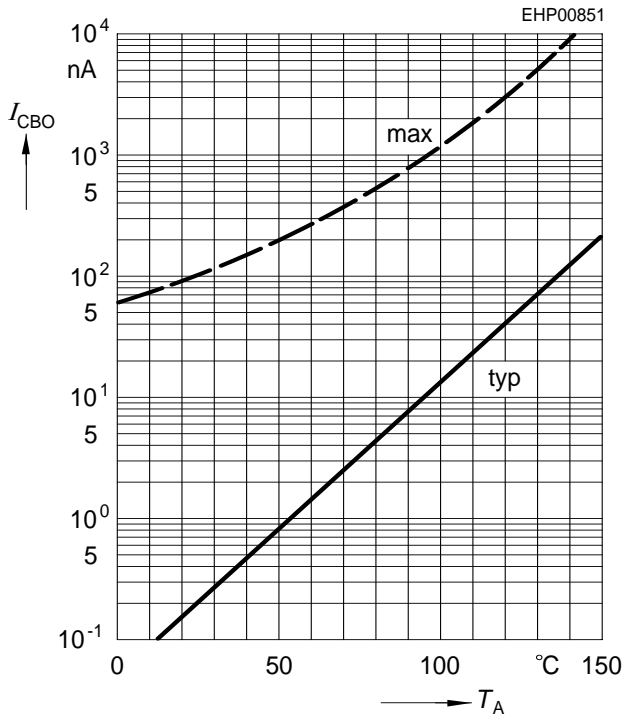
Collector current $I_C = f(V_{BE})$

$V_{CE} = 1\text{ V}$



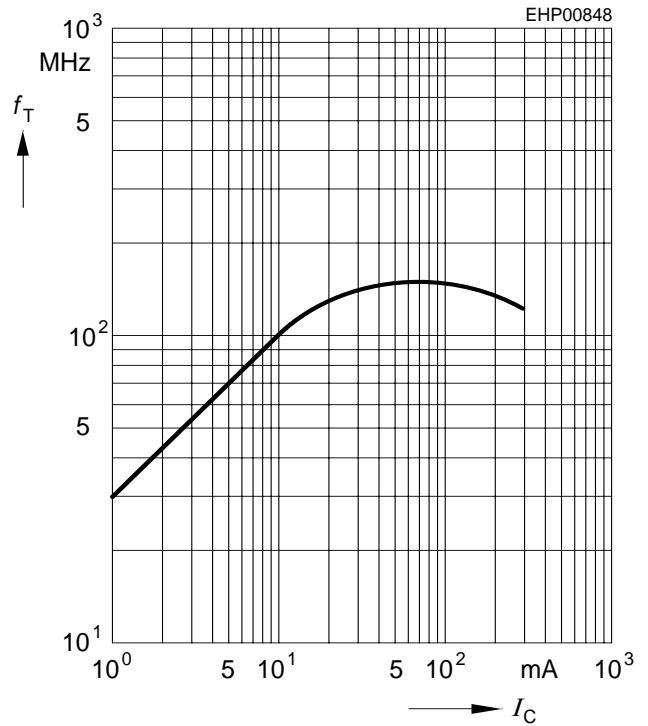
Collector cutoff current $I_{CBO} = f(T_A)$

$V_{CB} = 80\text{ V}$



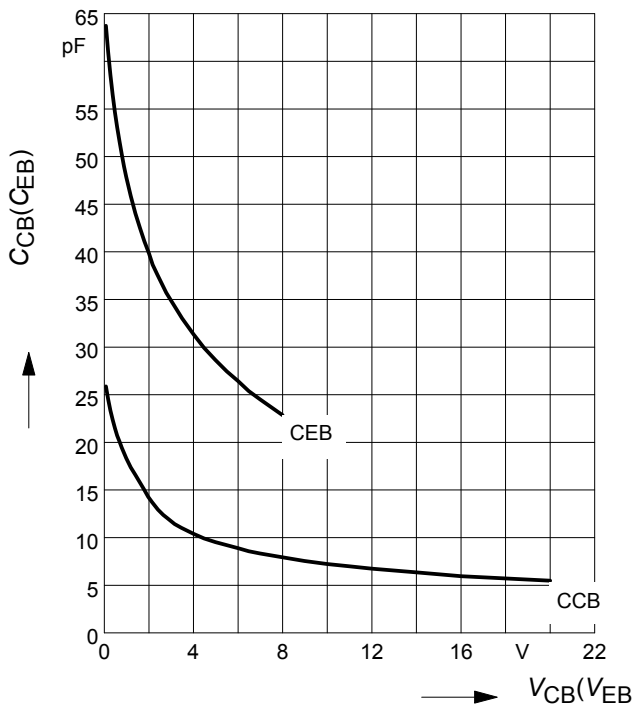
Transition frequency $f_T = f(I_C)$

$V_{CE} = \text{parameter in V, } f = 2\text{ GHz}$

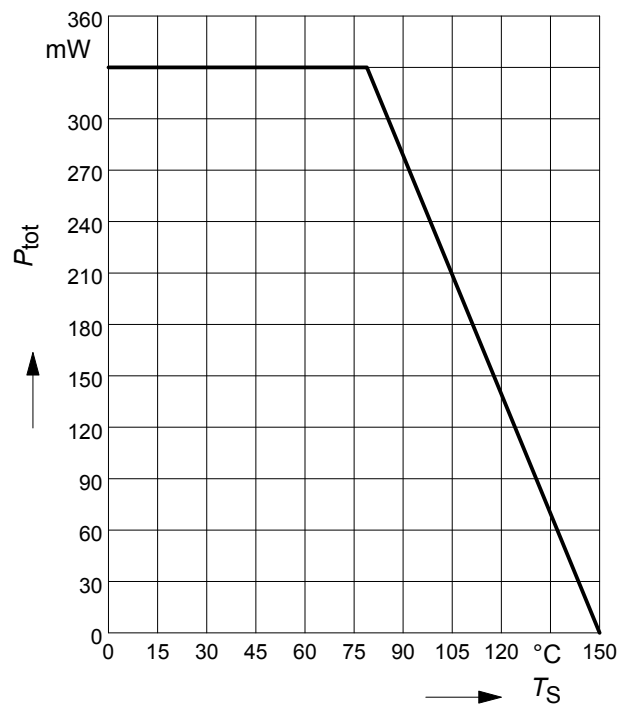


Collector-base capacitance $C_{cb} = f(V_{CB})$

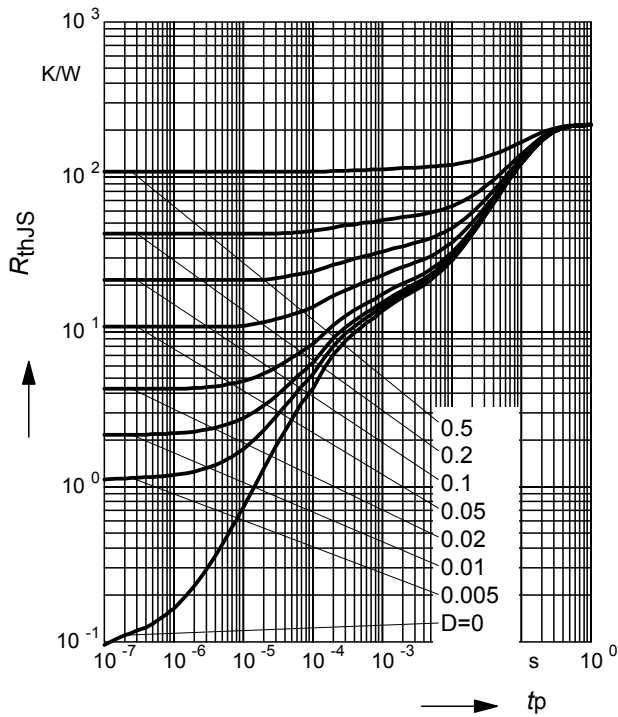
Emitter-base capacitance $C_{eb} = f(V_{EB})$



Total power dissipation $P_{tot} = f(T_S)$

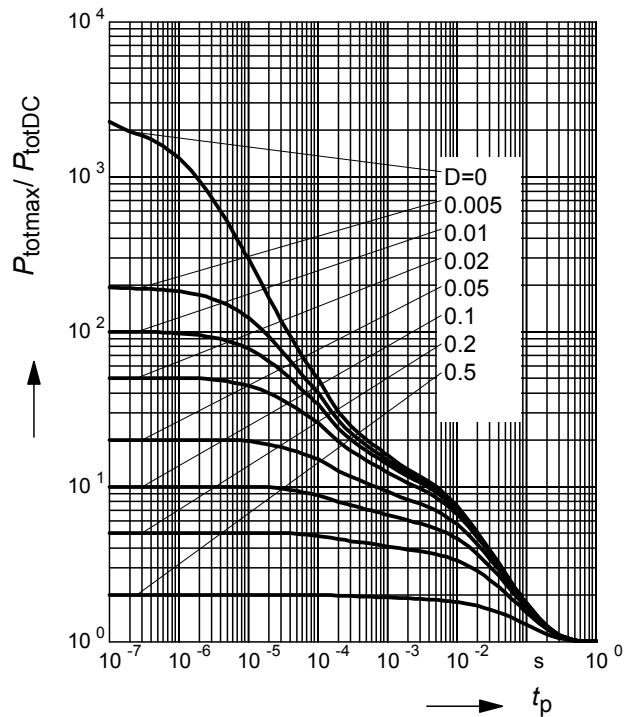


Permissible Pulse Load $R_{thJS} = f(t_p)$

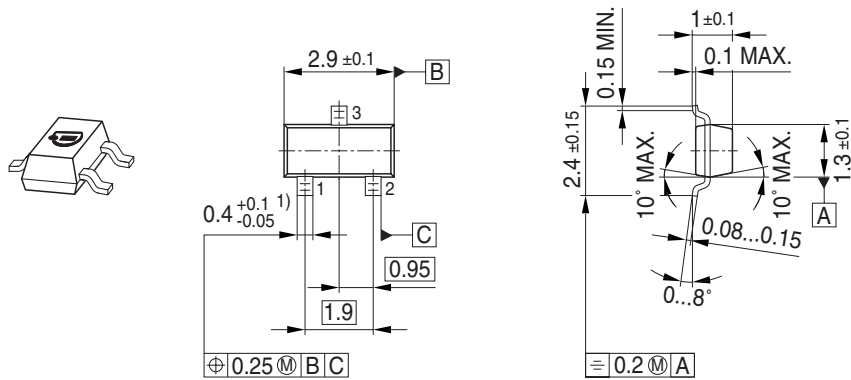


Permissible Pulse Load

$P_{totmax}/P_{totDC} = f(t_p)$

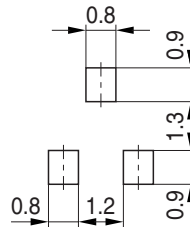


Package Outline

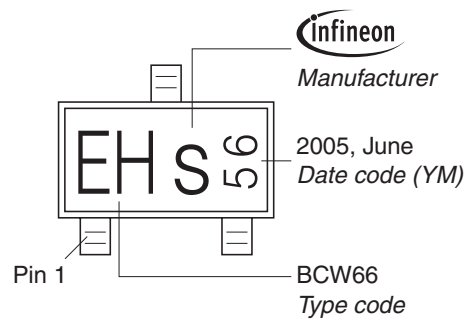


1) Lead width can be 0.6 max. in dambar area

Foot Print

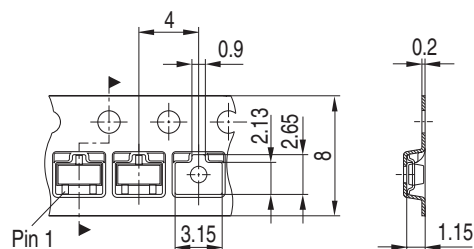


Marking Layout (Example)



Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel



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