19-3659; Rev 1; 10/06

MAX12553/MAX12554/MAX12555 Evaluation Kits

Evaluate: MAX12553/MAX12554/MAX12555

General Description

The MAX12553/MAX12554/MAX12555 evaluation kits (EV kits) are fully assembled and tested PCBs that contain all the components necessary to evaluate the performance of this family of 14-bit, analog-to-digital converters (ADCs). These ADCs accept differential or single-ended analog inputs, however, the EV kits allow for evaluation with either type of signal from one single-ended analog-signal source. The digital outputs produced by the ADCs are captured easily with a user-provided high-speed logic analyzer or data-acquisition system. The EV kits operate from a 1.8V and a 3.3V power supply and include circuitry that generates a low-jitter clock signal from an AC signal provided by the user.

Features

- **95Msps Sampling Rate with the MAX12555**
- **80Msps Sampling Rate with the MAX12554**
- **65Msps Sampling Rate with the MAX12553**
- **Low-Voltage and Low-Power Operation**
- **Fully Differential or Single-Ended Signal-Input Configuration**
- **Differential or Single-Ended Clock Configuration**
- **On-Board Clock-Shaping Circuit with Adjustable Duty Cycle**
- **Fully Assembled and Tested**

Part Selection Table

PART NUMBER	SPEED (Msps)	APPLICATION
MAX12555ETL+	95	IF/Baseband Sampling
MAX12554ETL+	80	IF/Baseband Sampling
MAX12553ETL+	65	IF/Baseband Sampling

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX12555EVKIT+	0°C to +70°C	40 Thin QFN-EP*
MAX12554EVKIT+	0°C to +70°C	40 Thin QFN-EP*
MAX12553EVKIT+	0°C to +70°C	40 Thin QFN-EP*

+ Denotes a lead-free and RoHS-compliant EV kit.
**EP = Exposed paddle.*

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2, C7, C33	4	22µF ±20%, 10V tantalum capacitors (B-case) AVX TAJB226M010
C3, C4, C6, C8–C12, C17, C21, C27, C34, C43, C45	14	1.0µF ±10%, 6.3V X5R ceramic capacitors (0402) TDK C1005X5R0J105K KEMET C0402C105K9PAC
C5, C14, C16, C18, C19, C20, C38, C44, C49, C50	0	Not installed, capacitors (0402)
C13, C15, C22–C26, C42	8	0.1µF ±20%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104M KEMET C0402C104K8PAC
C28	1	10µF ±20%, 6.3V X5R ceramic capacitor (0805) TDK C2012X5R0J106M KEMET C0805C106K9PAC
C29, C40, C41, C48, C51, C52	0	Not installed, capacitors (0603)
C30, C31, C32, C35, C36, C37	6	2.2µF ±20%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J225M Panasonic ECJ1VB0J225K
C39	1	4.7µF ±10%, 6.3V X5R ceramic capacitor (0603) TDK C1608X5R0J475K Panasonic ECJ1VB0J475K
C46, C47	2	15pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H150J
CLOCK4	0	Not installed, SMA vertical connector (SMA)
CLOCK, AINP, AINN	3	SMA vertical PC mount connectors (SMA)

Component List continued on next page.

MAX12553/MAX12554/MAX12555 Evaluation Kits

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
D1	1	Dual Schottky diode (SOT23) Central Semiconductor CMPD6263S, lead free (Top Mark: D96) Vishay BAS70-04 (Top Mark: 74) Diodes Inc. BAS70-04-7-F (Top Mark: K74 or K7D)
D2	0	Not installed, diode (SOT23)
J1	1	Dual-row, 2 x 20, 40-pin header
JU1, JU9, JU10	0	Not installed, 2-pin headers
JU2–JU8	7	3-pin headers
L1–L4	4	EMI filters Murata NFM41PC204F1H3B
R1, R8, R11, R15–R28, R31	0	Not installed, resistors (0603)
R2, R12, R13, R14	0	Not installed, resistors (0402)
R3, R4	2	75Ω ±0.5% resistors (0603)
R5, R6	2	1.0kΩ ±5% resistors (0402)
R7, R9	2	100Ω ±1% resistors (0603)
R10	1	10kΩ potentiometer, 12-turn, 1/4in
R29, R30	2	110Ω ±0.5% resistors (0603)
RA1–RA4	4	220Ω ±5% resistor arrays Panasonic EXB-2HV-221J
T1, T2	2	1:1 RF transformers Mini-Circuits ADT1-1WT
T3	1	4:1 RF transformer Mini-Circuits ADT4-6WT
T4	0	Not installed, transformer
TP1–TP4	4	Miniature PC test points (red) Keystone Electronics 5000
TP5, TP6	2	Miniature PC test points (black) Keystone Electronics 5001
U1	1	See the *EV Kit-Specific Component List*
U2	1	Low-voltage, 16-bit register (48-pin TSSOP) Texas Instruments SN74AVC16374DGGR
U3	0	Not installed (SC70-5)
U4	1	TinyLogic UHS buffer (SC70-5) Fairchild NC7SZ125P5
U5	0	Not installed (8-pin SO)
U6	1	TinyLogic dual UHS inverter (SC70-6) Fairchild NC7WZ04P6
—	7	Shunts (JU2–JU8)
—	1	MAX12553/MAX12554/ MAX12555EVKIT+ PCB

EV Kit-Specific Component List

EV KIT PART NUMBER	REFERENCE DESIGNATOR	DESCRIPTION
MAX12555EVKIT+	U1	MAX12555ETL+ (40-pin, 6mm x 6mm x 0.8mm Thin QFN with EP)
MAX12554EVKIT+		MAX12554ETL+ (40-pin, 6mm x 6mm x 0.8mm Thin QFN with EP)
MAX12553EVKIT+		MAX12553ETL+ (40-pin, 6mm x 6mm x 0.8mm Thin QFN with EP)

Component Suppliers

SUPPLIER	PHONE	WEBSITE
AVX Corp.	843-946-0238	www.avxcorp.com
Central Semiconductor	631-435-1110	www.centralsemi.com
Fairchild Semiconductor	888-522-5372	www.fairchildsemi.com
Murata Mfg. Co., Ltd.	770-436-1300	www.murata.com
Panasonic Corp.	714-373-7366	www.panasonic.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: *Indicate that you are using the MAX12553, MAX12554, or MAX12555 when contacting these component suppliers.*

Quick Start

Recommended Equipment

- DC power supplies:
  - Digital (VLDUT) 1.8V, 100mA
  - Logic (VL) 1.8V, 100mA
  - Analog (VDUT) 3.3V, 250mA
- Signal generator with low phase noise and low jitter for clock input (e.g., HP/Agilent 8644B)
- Signal generator for analog-signal input (e.g., HP/Agilent 8644B)
- Logic analyzer or data-acquisition system (e.g., HP/Agilent 16500C)
- Analog bandpass filters (e.g., K&L Microwave) for input and clock signals
- Digital voltmeter

Procedure

Each EV kit is a fully assembled and tested surface-mount PCB. Follow the steps below to verify board operation. **Caution: Do not turn on power supplies or enable signal generators until all connections are completed.**

1) Verify that shunts are installed across pins 2-3 of jumpers JU2 (ADC enabled) and JU3 (two's-complement digital-output format).
2) Verify that shunts are installed across pins 1-2 of jumpers JU4 (internal duty-cycle equalizer enabled) and JU5 (differential clock configuration).
3) Verify that shunts are installed across pins 2-3 of jumper JU6 and across pins 1-2 of jumpers JU7 and JU8.
4) Connect the clock generator output to the clock bandpass filter input.
5) Connect the output of the clock bandpass filter to the CLOCK SMA connector.
6) Connect the output of the analog-signal generator to the input of the signal bandpass filter. Keep the cable connection between the signal generators, filters, and EV kit board as short as possible for optimum dynamic performance.
7) Connect the output of the signal bandpass filter to the AINP SMA connector. **Note: It is recommended that a 3dB or 6dB attenuation pad be used to reduce reflections and distortion from the bandpass filter.**
8) Connect the logic analyzer to the square pin header (J1). See the *Digital Output* section for bit locations and J1 header designations. The system clock is available on pin 3 of J1.
9) Connect a 3.3V, 250mA power supply to VDUT. Connect the ground terminal of this supply to the corresponding GND pad.
10) Connect a 1.8V, 100mA power supply to VL. Connect the ground terminal of this supply to the GND pad.
11) Connect a 1.8V, 100mA power supply to VLDUT. Connect the ground terminal of this supply to the GND pad.
12) Turn on the 3.3V power supply.
13) Turn on the 1.8V power supplies.
14) Enable the signal generators.
15) Set the clock-signal generator to the desired clock frequency. See the *Part Selection Table* for appropriate frequency settings for each EV kit. The amplitude of the generator should be sufficient to produce a 16dBm signal at the SMA input of the EV kits.
16) Set the analog input-signal generators for an output amplitude of less than or equal to $2V_{P-P}$ and to the desired test frequency.
17) Verify that the two signal generators are synchronized to each other. Adjust the output power level of the signal generators to overcome cable, bandpass filter, and attenuation pad losses at the input.
18) Enable the logic analyzer.
19) Collect data using the logic analyzer.

Detailed Description

Each EV kit is a fully assembled and tested PCB that contains all the components necessary to evaluate the performance of the MAX12553, MAX12554, or MAX12555 IC. Data generated by the EV kits are captured on a single 14-bit parallel bus. The EV kits accept differential or single-ended analog inputs and single-ended clock signals. With the proper board configuration, the ADC is evaluated with both types of signals by supplying only one single-ended analog signal to the EV kit.

The EV kits are designed as four-layer PCBs to optimize the performance of this family of ADCs. For simple operation, the EV kits require 3.3V and 1.8V power supplies, applied to analog and digital power planes, respectively. However, the digital plane operates down to 1.7V without compromising the ADC's performance. The logic analyzer's threshold must be adjusted accordingly.

Access to the digital outputs is provided through connector J1. The 40-pin connector easily interfaces with a user-provided logic analyzer or data-acquisition system. The DAV buffered output clock signal is available at pin 3 of J1 (CLKO) and is used to synchronize the output data to the logic analyzer.

Power Supplies

The EV kits require separate analog and digital power supplies for best performance. Separate 3.3V power supplies are used to power the analog circuit blocks of the converter (VDUT) and the clock-shaping circuit (VCLK). To evaluate single-ended clock-signal operation, 3.3V must be supplied to VCLK. Separate 1.8V power supplies are used to power the digital circuit block of the converter (VLDUT) and the buffer/driver, U2 (VL). The digital circuit blocks of the EV kits operate with voltage supplies as low as 1.7V and as high as 3.6V.

Clock Input

The MAX12553, MAX12554, and MAX12555 accept differential or single-ended clock input signals. However, the EV kits only accept a single-ended clock signal. The EV kits include circuitry that converts a single-ended signal to a differential clock signal through a transformer or a user-installed differential clock driver IC (U5). The EV kits also include clock-shaping circuitry for a single-ended clock-signal configuration. Jumper JU5 must be configured for differential or single-ended clock-signal operation. See Table 1 for jumper settings.

Table 1. Clock Input Settings (JU5)

SHUNT POSITION	CLKTYP PIN	CLOCK INPUT CONFIGURATION
1-2*	Connected to VLDUT	Differential
2-3	Connected to GND	Single-Ended

**Default position.*

Transformer-Coupled Differential Clock

A single-ended signal connected to the CLOCK SMA connector is converted to a differential signal by transformer T3. In this mode, diode D1 limits the clock-signal amplitude. Using this diode in the signal path allows the clock signal to be increased significantly without violating the absolute maximum ratings of the converter inputs, as the diode clips the input signal. Overdriving the clock input to the board (CLOCK SMA) results in an increased slew rate, which, in turn, compensates for the negative effects that clock jitter imposes on parameters such as signal-to-noise ratio (SNR) and signal-to-noise plus distortion (SINAD). See Table 2 for jumper settings.

Table 2. Clock Drive Settings

JUMPER	SHUNT POSITION	CLOCK MODE
JU4	2-3	Single-Ended Clock Mode—See the *Clock-Shaping Circuit with Variable Duty Cycle* section.
JU6	1-2	
JU7	2-3	
JU8	2-3	
JU4	1-2*	Differential Clock Mode—A single-ended signal is converted to a differential signal that drives the ADC clock inputs.
JU6	2-3*	
JU7	1-2*	
JU8	1-2*	

**Default position.*

Install a shunt across pins 1-2 of jumper JU5 for differential clock operation. **Note: While in transformer-coupled differential clock mode, power to VCLK should not be applied unless R10 is turned to one extreme to avoid unnecessary triggering of U6. Unnecessary triggering could potentially disturb the ground plane with unwanted spur energy.**

Clock-Shaping Circuit with Variable Duty Cycle

An on-board variable duty-cycle, clock-shaping circuit generates a single-ended clock signal from an AC-coupled sine wave applied to the CLOCK SMA connector. Measure the clock signal at pin 2 of jumper JU7 and adjust potentiometer R10 to obtain the desired duty cycle. See Table 2 for shunt positions. A 3.3V voltage source must be connected across VCLK and GND to power the clock-circuit comparators.

Input Signal

The MAX12553, MAX12554, and MAX12555 accept differential or single-ended analog input signals. However, the EV kits require only a single-ended analog input signal. Because the amplitude of the received signal at the ADC depends on the actual cable and bandpass filter loss, account for these losses when configuring the signal-input generator. In differential mode, on-board transformers T1 and T2 take the single-ended analog input connected to the AINP SMA connector and generate a differential analog signal at the ADC's input pins. For direct single-ended or differential input-signal operation, the EV kit board circuit modifications are listed in the *Direct AC-Coupled Differential Input* and *Direct AC-Coupled Single-Ended Input* sections.

Direct AC-Coupled Differential Input

To evaluate the MAX12553/MAX12554/MAX12555 EV kits with differential input signals directly connected to the ADC input pins, modify the EV kits as follows:

1) Remove transformers T1 and T2.
2) Remove the short across resistor R15.
3) Remove R3 and R4.
4) Install 0Ω resistors across R20 and R24.
5) Install 0.1µF ceramic capacitors across C51 and C52.
6) Modify resistors R29 and R30 to match the source impedance (e.g., 25Ω resistors for a 50Ω differential source impedance).
7) Connect the positive input-signal source to the AINP SMA connector.
8) Connect the negative input-signal source to the AINN SMA connector.

Direct AC-Coupled Single-Ended Input

To evaluate the MAX12553/MAX12554/MAX12555 EV kits with a single-ended input signal directly connected to the ADC input terminal, modify the EV kits as follows:

1) Remove transformers T1 and T2.
2) Remove resistor R3.
3) Install 0Ω resistors across R20, R29, and R13.
4) Install a 0.1µF ceramic capacitor across C51.
5) Install a 1µF capacitor across C47.
6) Modify resistor R30 to match the source impedance (e.g., a 50Ω resistor for a 50Ω source impedance).
7) Connect the positive input-signal source to the AINP SMA connector.

Converter Power-Down

The MAX12553, MAX12554, and MAX12555 each feature an active-high global device power-down pin. Jumper JU2 controls this feature. Other ICs on the EV kits continue to draw quiescent current from the power supplies. See Table 3 for power-down jumper settings.

Table 3. Power-Down Settings (JU2)

SHUNT POSITION	PD PIN	EV KIT OPERATION
1-2	Connected to VLDUT	Powered Down
2-3*	Connected to GND	Normal Operation

**Default position.*

Reference Voltage

The MAX12553, MAX12554, and MAX12555 require an input-reference voltage at the converter's REFIN pin to set the full-scale analog-signal voltage input. The ADC offers a stable on-chip reference voltage of 2.048V that is accessed at the REFIN pad. The EV kits were designed to use the on-chip reference voltage by shorting REFIN to REFOUT through resistor R12.

The user externally adjusts the reference level, hence the full-scale range, by cutting open the PC trace shorting resistor R12 and installing the appropriate resistors at locations R2 and R12 (located on the board's component side). Calculate the resistor values using the following equation:

$$R12 = R2\left(\frac{V_{REFOUT}}{V_{REFIN}} - 1\right)$$

where:

R2 = 10kΩ ±1%

V_{REFOUT} = 2.048V

V_{REFIN} = desired REFIN voltage in the 0.7V to 2.2V range

Alternatively, resistors R12 and R2 can be left unpopulated and the ADC's full-scale range set by applying a stable, low-noise, external voltage reference directly at the REFIN pad.

Shorting the REFIN pad to ground through resistor R2 disables the internal reference voltage. In this mode, test points TP1 (REFP), TP2 (REFN), and TP3 (COM) must be driven with stable reference voltages. Refer to the *Analog Inputs and Reference Configurations* section in the MAX12553, MAX12554, and MAX12555 IC data sheets for further details. **Note: To drive test point TP3 with an external reference voltage, add a 0Ω resistor across R27.**

Output Coding

Set the digital output coding to either two's-complement or Gray-code format by configuring jumper JU3. See Table 4 for shunt positions.

Table 4. Output Code Settings (JU3)

SHUNT POSITION	$G/\overline{T}$ PIN	DIGITAL OUTPUT FORMAT
1-2	Connected to VLDUT	Gray Code
2-3*	Connected to GND	Two's Complement

**Default position.*

Digital Output

The MAX12553, MAX12554, and MAX12555 feature a 14-bit, parallel, CMOS-compatible output bus. The outputs of the ADC are applied to an output buffer (U2) capable of driving large capacitive loads that may be present at the logic analyzer connection. The digital outputs are valid on the rising edge of the CLKO output signal. The outputs of the buffer are connected to a 40-pin header (J1) located on the right side of the EV kits, where the user connects a logic analyzer or data-acquisition system. See Table 5 for bit locations at header J1. The signals are available on the J1 pins closest to the edge of the EV kit boards.

Component Placement and Board Layout Recommendations

Refer to the *Schematic and Layout Guidelines for High-Speed Data Converters* application note, located at www.maxim-ic.com/appnotes.cfm/an_pk/3491, for a detailed discussion about component placement and PCB layout recommendations for the MAX12553/MAX12554/MAX12555.

Table 5. Output Bit Locations (J1)

CLOCK	DOR	BIT D13	BIT D12	BIT D11	BIT D10	BIT D9	BIT D8	BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
J1-3 CLKO ↑	J1-7	J1-11	J1-13	J1-15	J1-17	J1-19	J1-21	J1-23	J1-25	J1-27	J1-29	J1-31	J1-33	J1-35	J1-37

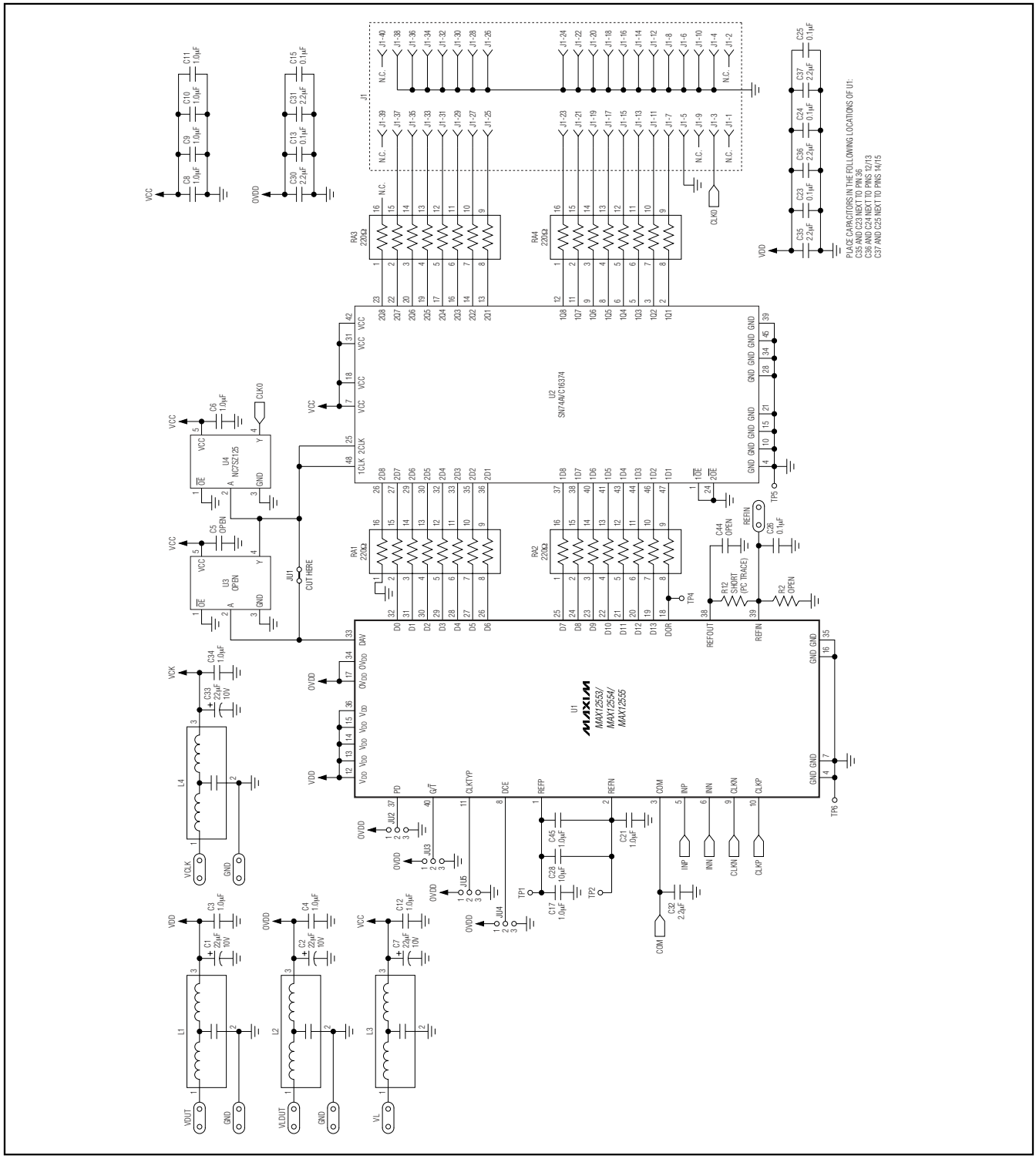

Figure 1a. MAX12553/MAX12554/MAX12555 EV Kits Schematic (Sheet 1 of 2)

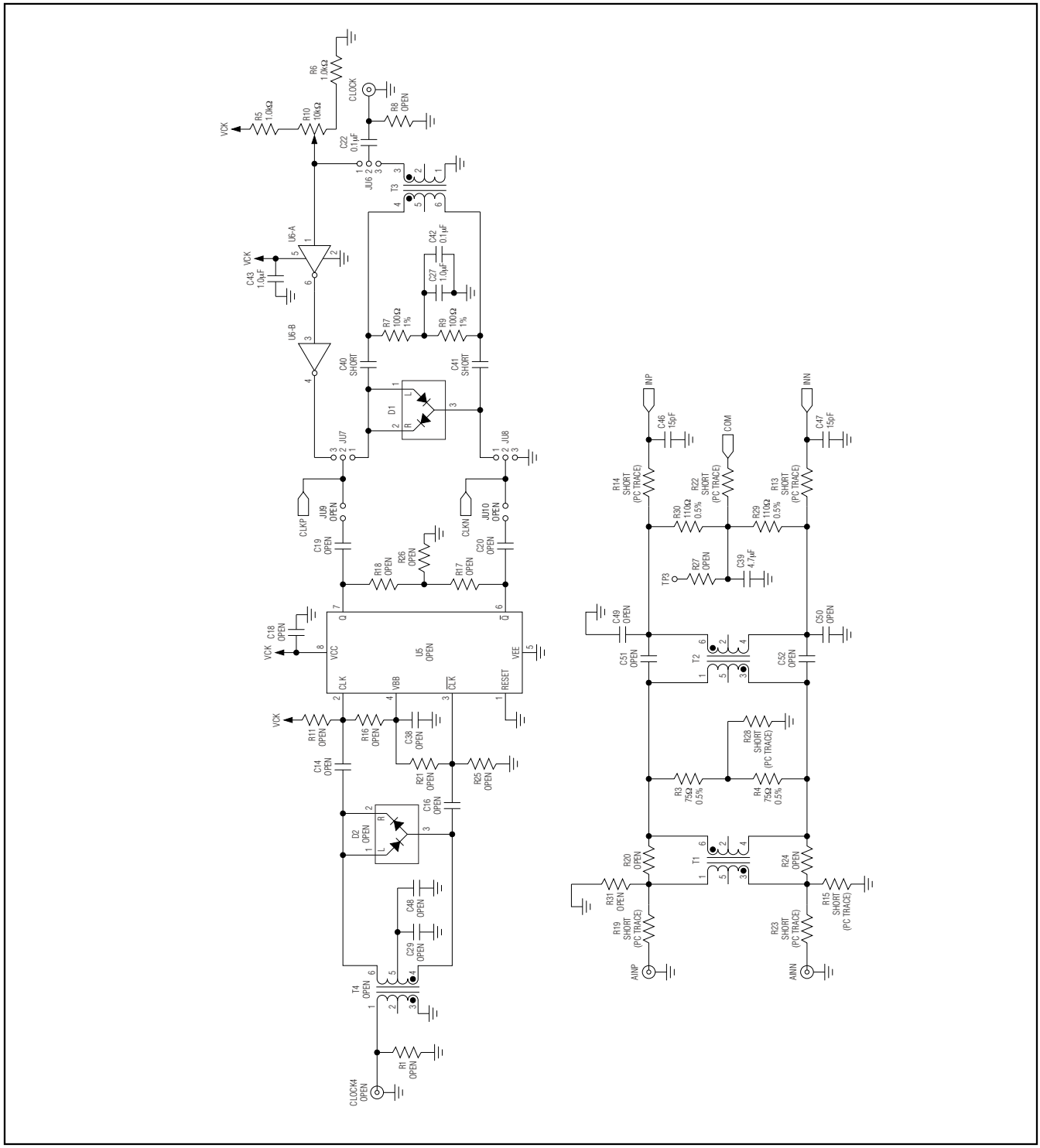

Figure 1b. MAX12553/MAX12554/MAX12555 EV Kits Schematic (Sheet 2 of 2)

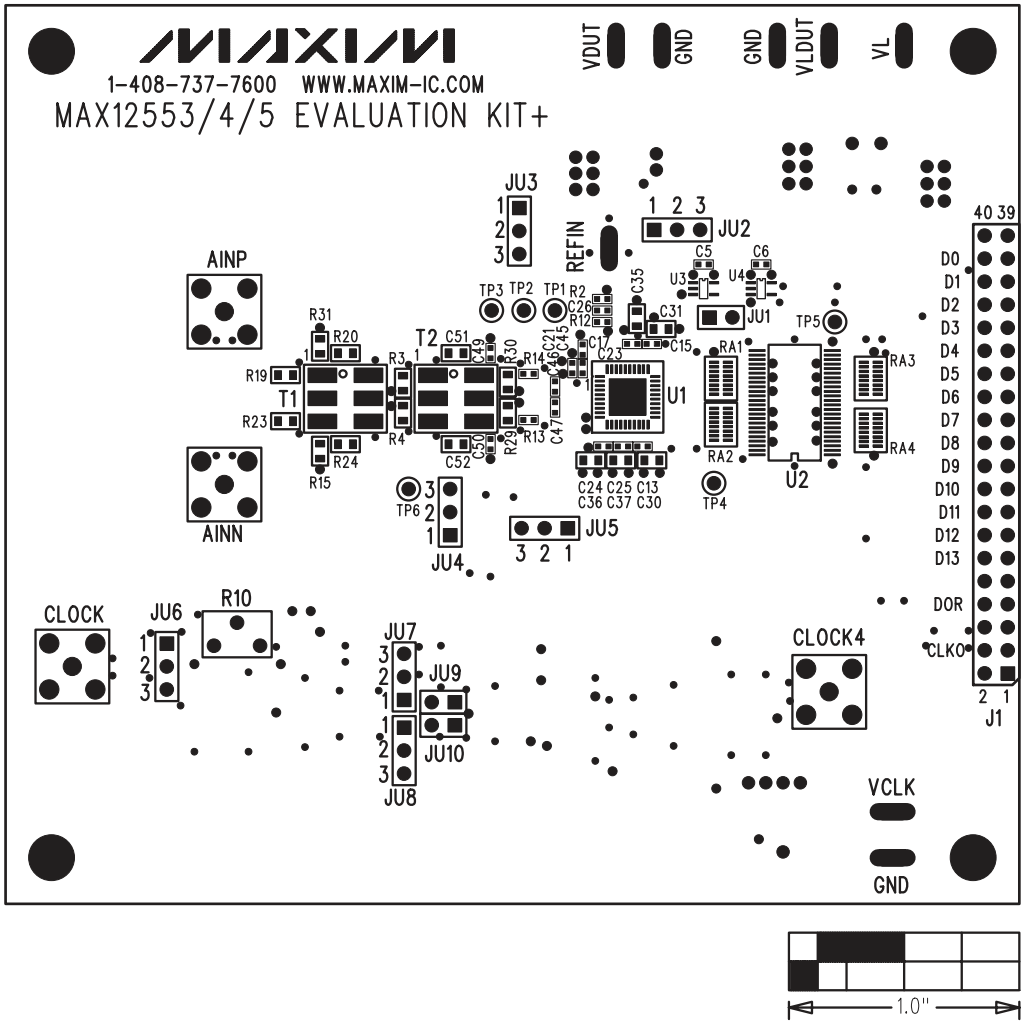

Figure 2. MAX12553/MAX12554/MAX12555 EV Kits Component Placement Guide—Component Side

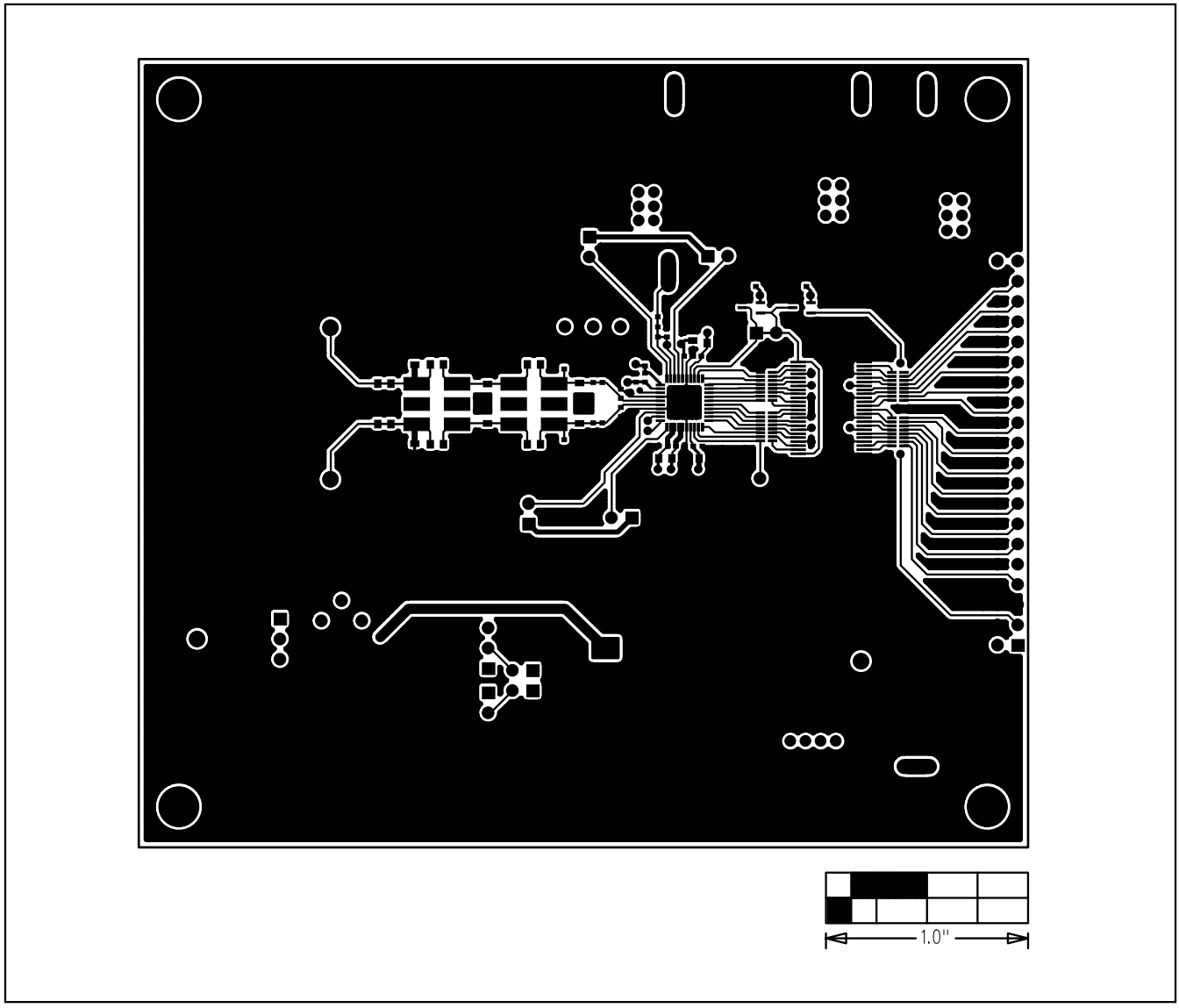

Figure 3. MAX12553/MAX12554/MAX12555 EV Kits PCB Layout—Component Side

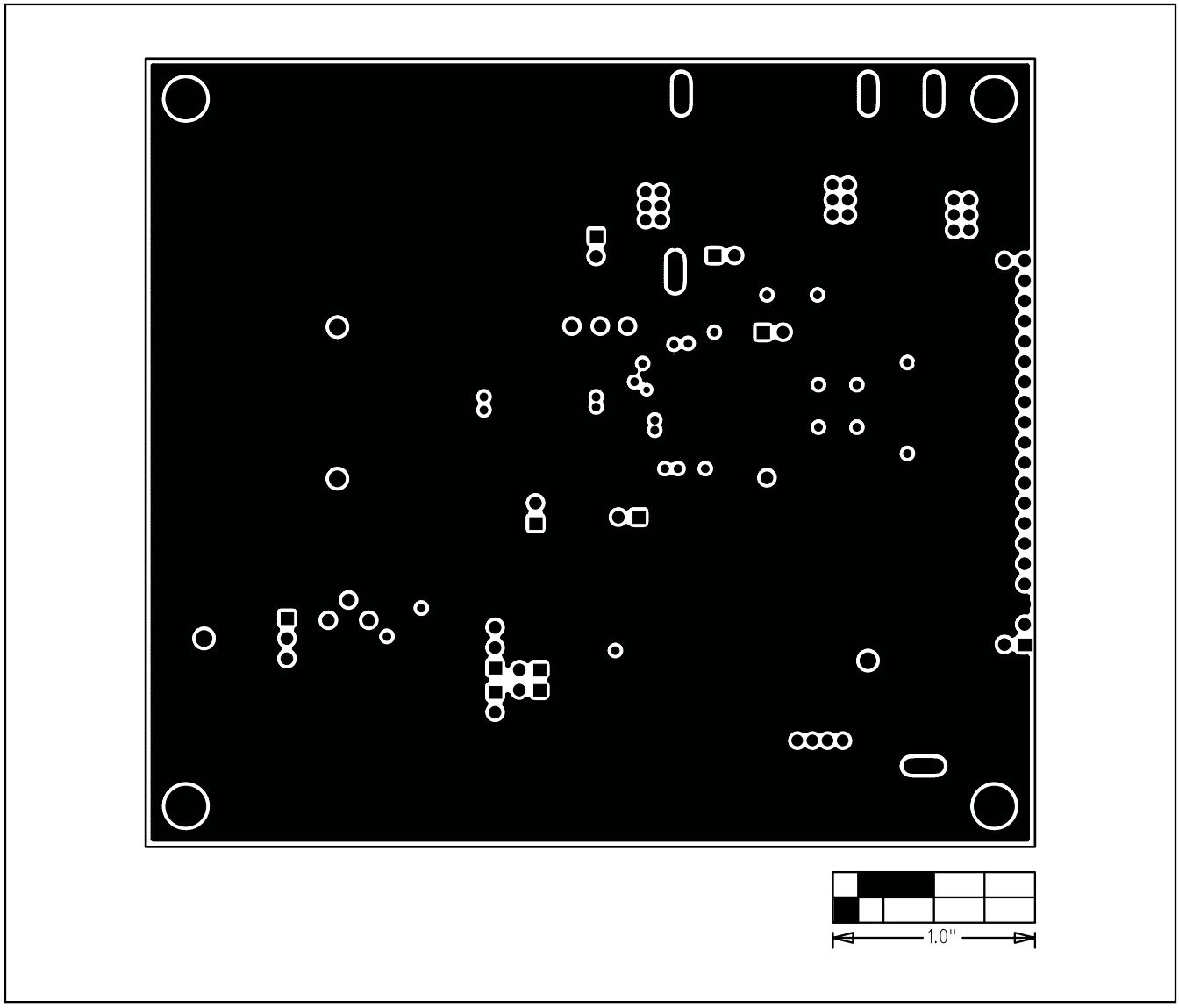

Figure 4. MAX12553/MAX12554/MAX12555 EV Kits PCB Layout—Ground Planes

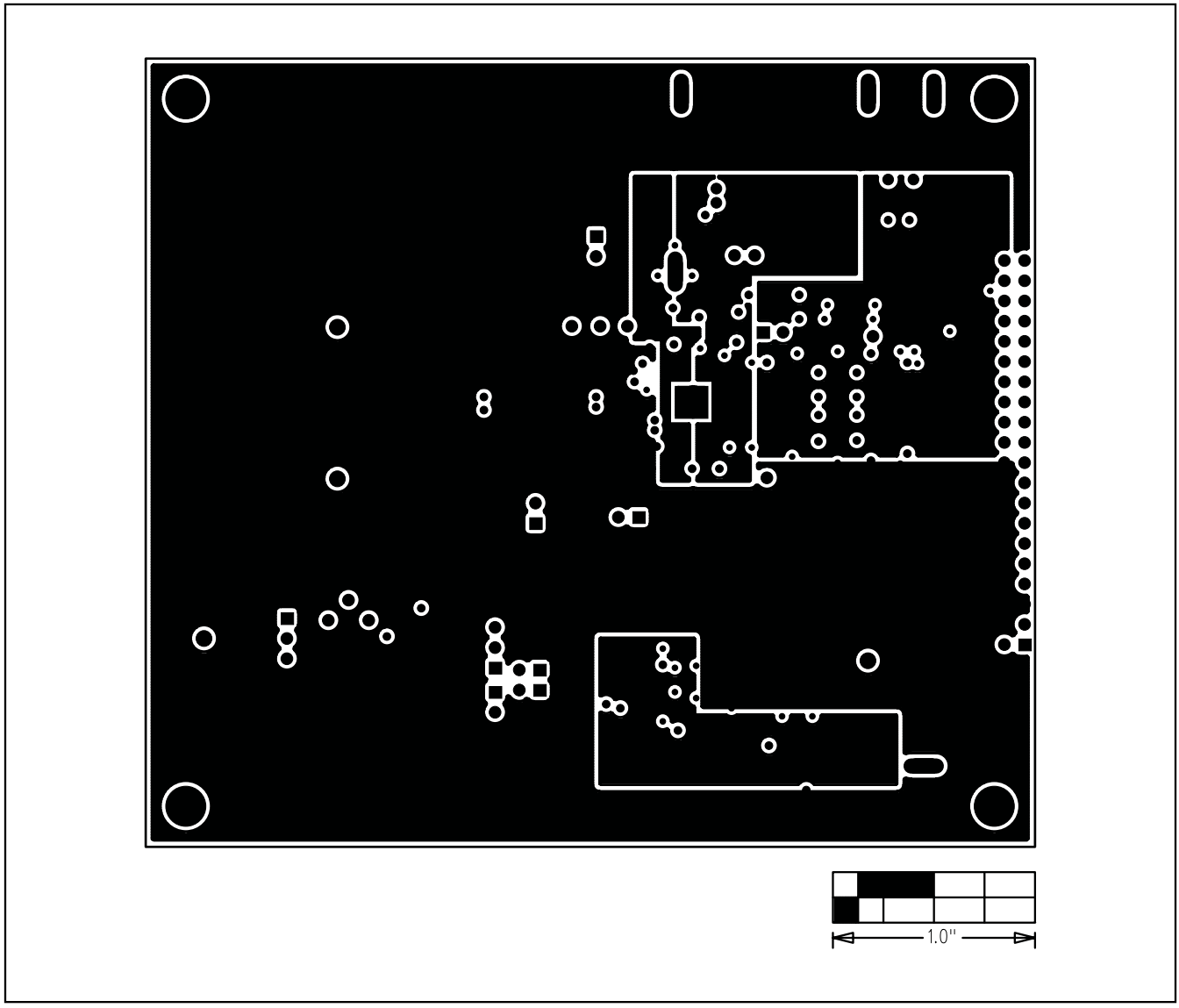

Figure 5. MAX12553/MAX12554/MAX12555 EV Kits PCB Layout—Power Planes

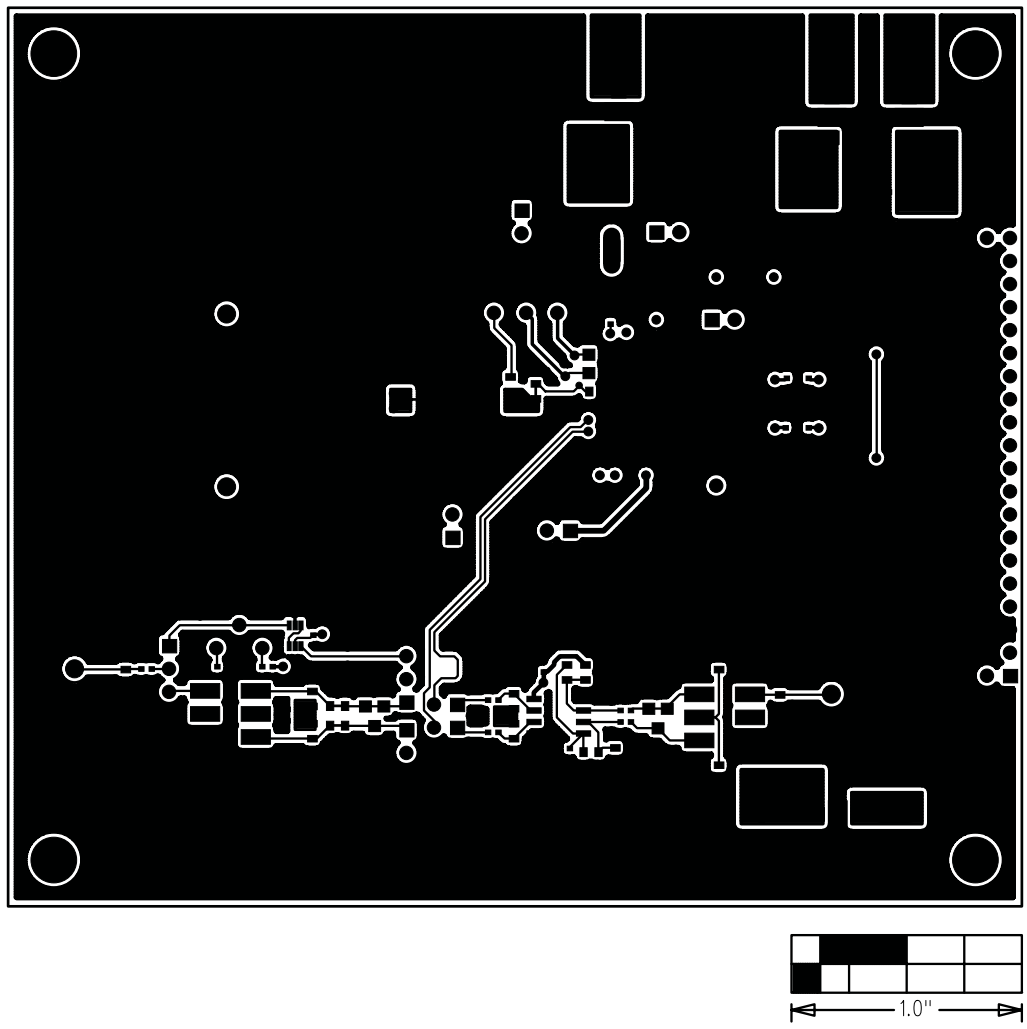

Figure 6. MAX12553/MAX12554/MAX12555 EV Kits PCB Layout—Solder Side

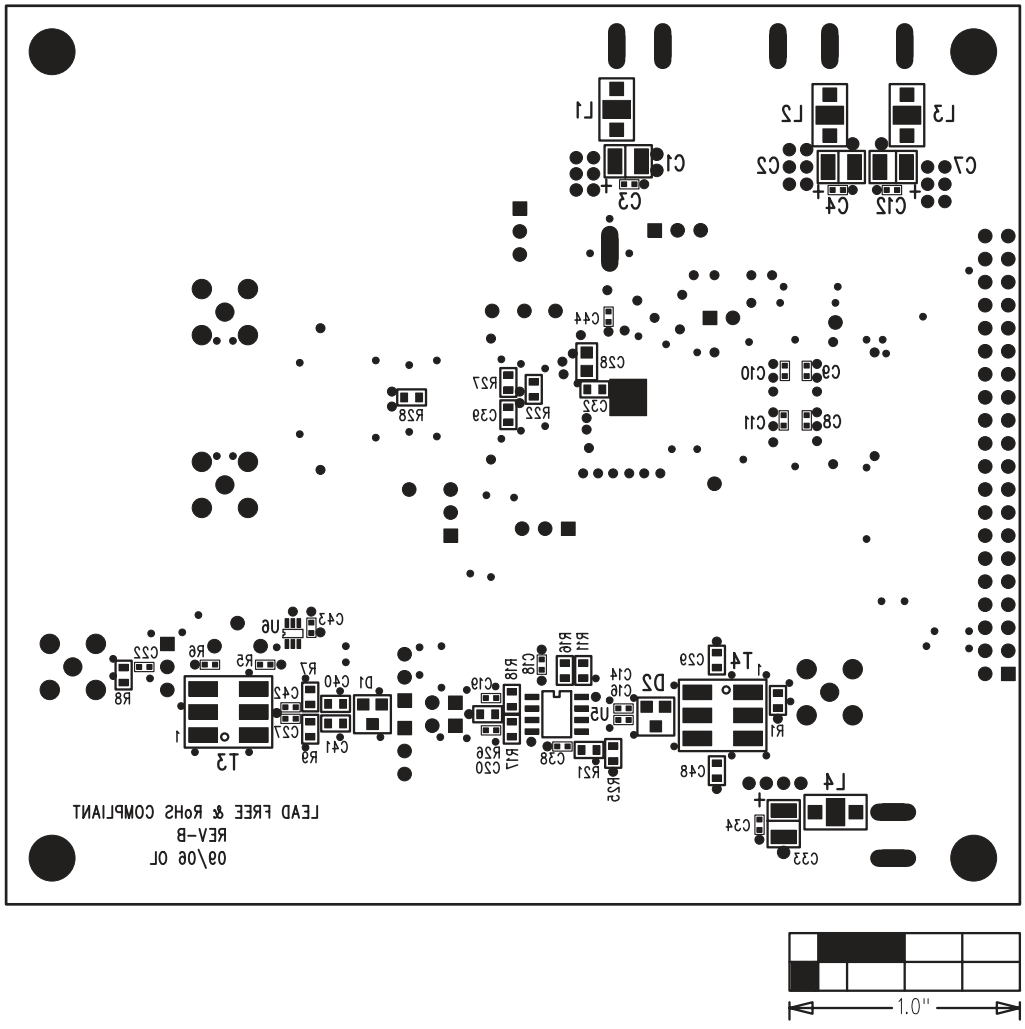

Figure 7. MAX12553/MAX12554/MAX12555 EV Kits Component Placement Guide—Solder Side

Revision History

Pages changed at Rev 1: Title change—all pages, 1–14