

# Product Standards

Part No.	<b>AN44075A</b>
Package Code No.	HSOP034-P-0300A

Semiconductor Company  
Matsushita Electric Industrial Co., Ltd.

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	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	2

### Contents

■ Overview .....		3
■ Features .....		3
■ Applications .....		3
■ Package .....		3
■ Type .....		3
■ Application Circuit Example .....		4
■ Block Diagram.....		5
■ Pin Descriptions .....		6
■ Absolute Maximum Ratings .....		7
■ Operating Supply Voltage Range .....		7
■ Allowed Voltage and Current Ranges .....		8
■ Electrical Characteristics .....		9
■ Electrical Characteristics (Reference values for design) .....		11
■ Test Circuit Diagram .....		12
■ Electrical Characteristics Test Procedures .....		14
■ Technical Data .....		20
• Circuit diagrams of the input/output part and pin function descriptions .....		20
• Control mode (truth table) .....		26
■ Usage Notes .....		27

2007-11-12		
Established	Revised	

	Product Standards	AN44075A	
		Total Pages	Page
		30	3

# AN44075A

## Driver IC for DC Motor

### ■ Overview

AN44075A is a one channel H-bridge driver IC. 1-ch. DC motor can be controlled by a single driver IC.

### ■ Features

- Built-in thermal protection and low voltage detection circuit
- Built-in over current protection (when external resistance is added to Pin 7 and Pin 8.)
- Built-in 5 V power supply

### ■ Applications

- IC for DC motor drives

### ■ Package

- 34 pin Plastic Small Outline Package with Back Heat Sink (SOP Type)

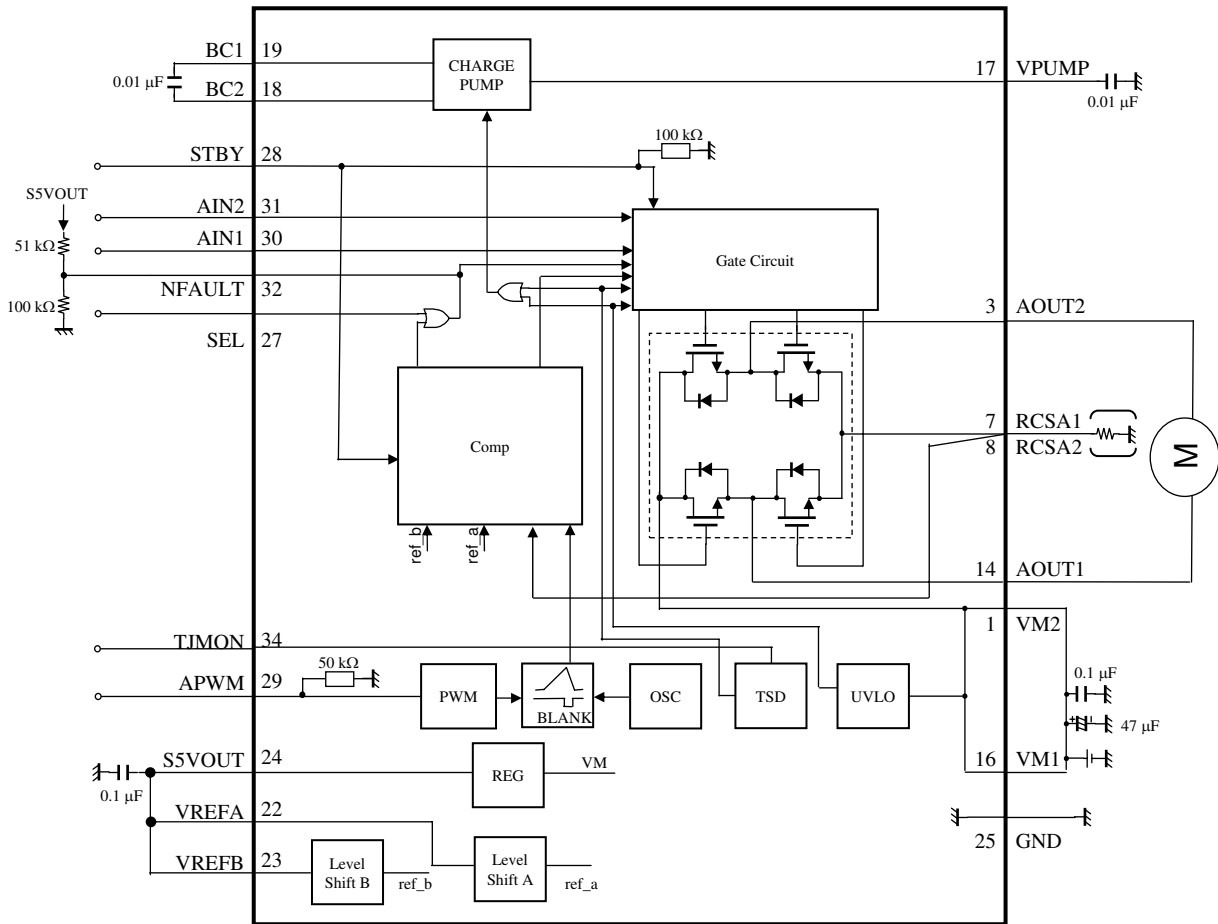
### ■ Type

- Bi-CDMOS IC

2007-11-12		
Established	Revised	

	Product Standards	AN44075A	
		Total Pages	Page
		30	4

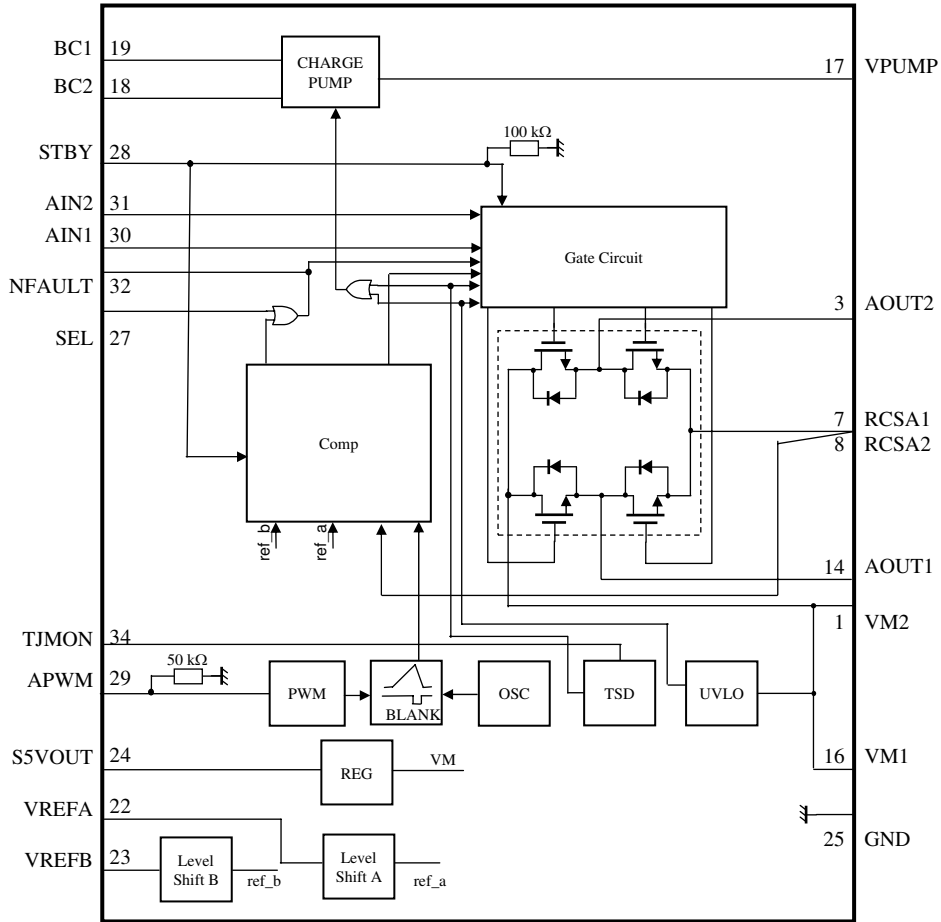
■ Application Circuit Example



Note) • This application circuit is shown as an example but does not guarantee the design for mass production set.

2007-11-12		
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■ Block Diagram



Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	6

### ■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	VM2	Power supply	Motor power supply 2
2	N.C.	—	not used
3	AOUT2	Output	Motor drive output 2
4	N.C.	—	not used
5	N.C.	—	not used
6	N.C.	—	not used
7	RCSA1	Input / Output	Current detection 1
8	RCSA2	Input / Output	Current detection 2
9	GND	Ground	Die pad ground
10	N.C.	—	not used
11	N.C.	—	not used
12	N.C.	—	not used
13	N.C.	—	not used
14	AOUT1	Output	Motor drive output 1
15	N.C.	—	not used
16	VM1	Power supply	Motor power supply 1
17	VPUMP	Output	Charge Pump circuit output
18	BC2	Output	Charge Pump capacitor connection 2
19	BC1	Output	Charge Pump capacitor connection 1
20	N.C.	—	not used
21	N.C.	—	not used
22	VREFA	Input	Peak current setting input
23	VREFB	Input	Load short threshold input
24	S5VOUT	Output	Internal reference voltage (5 V output)
25	GND	Ground	Signal ground
26	GND	Ground	Die pad ground
27	SEL	Input	Test mode input
28	STBY	Input	Standby input
29	APWM	Input	PWM input
30	AIN1	Input	Forward-Reverse input
31	AIN2	Input	Brake mode input
32	NFAULT	Output	Abnormal detection output
33	N.C.	—	not used
34	TJMON	Output	VBE monitor

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	7

### ■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which are not destructed, and are not the values to which operation is guaranteed.

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage1 (Pin 1, Pin 16)	$V_M$	37	V	*1
2	Power dissipation	$P_D$	0.466	W	*2
3	Operating ambient temperature	$T_{opr}$	-20 to +70	°C	*3
4	Storage temperature	$T_{stg}$	-55 to +150	°C	*3
5	Output pin voltage (Pin 3, Pin 14)	$V_{OUT}$	37	V	*4
6	Motor drive current (Pin 3, Pin 14)	$I_{OUT}$	±3.0	A	*4, *5
7	Flywheel diode current (Pin 3, Pin 14)	$I_f$	3.0	A	*4, *5

Notes) \*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

\*2 : The power dissipation shown is the value at  $T_a = 70^\circ\text{C}$  for the independent (unmounted) IC package without a heat sink.

When using this IC, refer to the  $P_D$ - $T_a$  diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

\*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for  $T_a = 25^\circ\text{C}$ .

\*4 : Do not apply current or voltage from outside to any pin not listed above.

In the circuit current, (+) means the current flowing into IC and (-) means the current flowing out of IC.

\*5 : It is the rating value when connecting the heat sink on the rear face of the package to the ground pattern on the glass epoxy 4-layered PCB. (the ground area in the second and third layer : more than 1 500 mm<sup>2</sup>)

### ■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
Operating supply voltage range	$V_M$	10.0 to 35.0	V	*

Note) \* : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	8

### ■ Allowed Voltage and Current Ranges

Notes) • Rating Voltage is voltage of pin on GND

- Do not apply current or voltage from outside to any pin not listed below.

Pin No.	Pin name	Rating	Unit	Note
7	RCSA1	+2.5	V	—
8	RCSA2	+2.5	V	—
17	VPUMP	$(V_M - 2)$ to 43	V	—
18	BC2	$(V_M - 1)$ to 43	V	—
19	BC1	$V_M + 0.3$	V	—
22	VREFA	-0.3 to 6	V	—
23	VREFB	-0.3 to 6	V	—
24	S5VOUT	-7 to 0	mA	*1
27	SEL	-0.3 to 6	V	—
28	STBY	-0.3 to 6	V	—
29	APWM	-0.3 to 6	V	—
30	AIN1	-0.3 to 6	V	—
31	AIN2	-0.3 to 6	V	—
32	NFAULT	-0.3 to 6	V	—
32	NFAULT	4	mA	—

Note) \*1 : It is the rating when using with the rang of  $V_M = 16\text{ V}$  to  $35\text{ V}$ . When  $V_M = 10\text{ V}$  to  $15\text{ V}$ , the rating is  $-4\text{ mA}$ .

2007-11-12		
Established	Revised	



<h1>Product Standards</h1>		AN44075A	
		Total Pages	Page
		30	9

## ■ Electrical Characteristics at $V_M = 24\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Note
					Min	Typ	Max		
<b>Output drivers</b>									
1	High-level output saturation voltage	$V_{OH}$	1	$I_{SA1} = I_{SA2} = -1\text{ A}$	$V_M$ -0.47	$V_M$ -0.36	—	V	—
2	Low-level output saturation voltage	$V_{OL}$	1	$I_{SA1} = I_{SA2} = 1\text{ A}$	—	0.50	0.65	V	—
3	Flywheel diode forward voltage	$V_{DI}$	2	$I_{DI} = \pm 1\text{ A}$	0.5	1.0	1.5	V	—
4	Output leakage current	$I_{LEAK}$	1	$V_M = 37\text{ V}, V_{SRCS} = 0\text{ V}$	—	10	20	$\mu\text{A}$	—
<b>Power supply</b>									
5	Supply current 1 (Sleep)	$I_{M1}$	1	$V_{STBY} = 0\text{ V}$	—	65	105	$\mu\text{A}$	—
6	Supply current 2 (with circuit turned on)	$I_{M2}$	1	$V_{STBY} = 5\text{ V}$	—	7.3	12	mA	—
7	Reference voltage	$V_{SSVOUT}$	1	$I_{SSVOUT} = -2.5\text{ mA}$	4.5	5.0	5.5	V	—
8	Output impedance	$Z_{SSVOUT}$	1	$\Delta I_{SSVOUT} = -5\text{ mA}$	—	18	27	$\Omega$	—
<b>IN input</b>									
9	High-level IN input voltage	$V_{INH}$	1	—	2.1	—	5	V	—
10	Low-level IN input voltage	$V_{INL}$	1	—	0	—	0.6	V	—
11	High-level IN input current	$I_{INH}$	1	$V_{AIN1} = V_{AIN2} = 5\text{ V}$	-10	—	10	$\mu\text{A}$	—
12	Low-level IN input current	$I_{INL}$	1	$V_{AIN1} = V_{AIN2} = 0\text{ V}$	-10	—	10	$\mu\text{A}$	—
<b>Standby input</b>									
13	High-level STBY input voltage	$V_{STBYH}$	1	—	2.1	—	5	V	—
14	Low-level STBY input voltage	$V_{STBYL}$	1	—	0	—	0.6	V	—
15	High-level STBY input current	$I_{STBYH}$	1	$V_{STBY} = 5\text{ V}$	30	—	80	$\mu\text{A}$	—
16	Low-level STBY input current	$I_{STBYL}$	1	$V_{STBY} = 0\text{ V}$	-10	—	10	$\mu\text{A}$	—
<b>PWM input</b>									
17	High-level PWM input voltage	$V_{PWMH}$	1	—	2.1	—	5	V	—
18	Low-level PWM input voltage	$V_{PWML}$	1	—	0	—	0.6	V	—
19	High-level PWM input current	$I_{PWMH}$	1	$V_{APWM} = 5\text{ V}$	60	—	150	$\mu\text{A}$	—
20	Low-level PWM input current	$I_{PWML}$	1	$V_{APWM} = 0\text{ V}$	-10	—	10	$\mu\text{A}$	—
21	PWM Input Max frequency	$f_{PWM}$	1	—	—	—	200	kHz	—
22	Input Min pulse width	$t_w$	1	—	2	—	—	$\mu\text{s}$	—

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	10

■ Electrical Characteristics (continued) at  $V_M = 24\text{ V}$

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Peak current detection / Over current protection									
23	Input bias current	$I_{REF}$	1	$V_{REFA} = V_{REFB} = 5\text{ V}$	83	100	125	$\mu\text{A}$	—
24	PWM frequency	$f_{PWM}$	1	$V_{REFA} = 0\text{ V}, V_{REFB} = 5\text{ V}$	17	26	35	kHz	—
25	Pulse blanking time	$T_B$	1	$V_{REFA} = 0\text{ V}, V_{REFB} = 5\text{ V}$	1.5	2.5	4.5	$\mu\text{s}$	—
26	Comp threshold 1	$V_{TH1}$	1	$V_{REFA} = V_{REFB} = 5\text{ V}$	480	500	520	mV	—
27	Comp threshold 2	$V_{TH2}$	1	$V_{REFA} = 5.5\text{ V}, V_{REFB} = 2.5\text{ V}$	475	500	525	mV	—
28	NFAULT output voltage	$V_{NFLT}$	1	$I_{NFLT} = 1\text{ mA}$	—	—	0.4	V	—

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	11

■ Electrical Characteristics (Reference values for design) at  $V_M = 24\text{ V}$

Notes)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

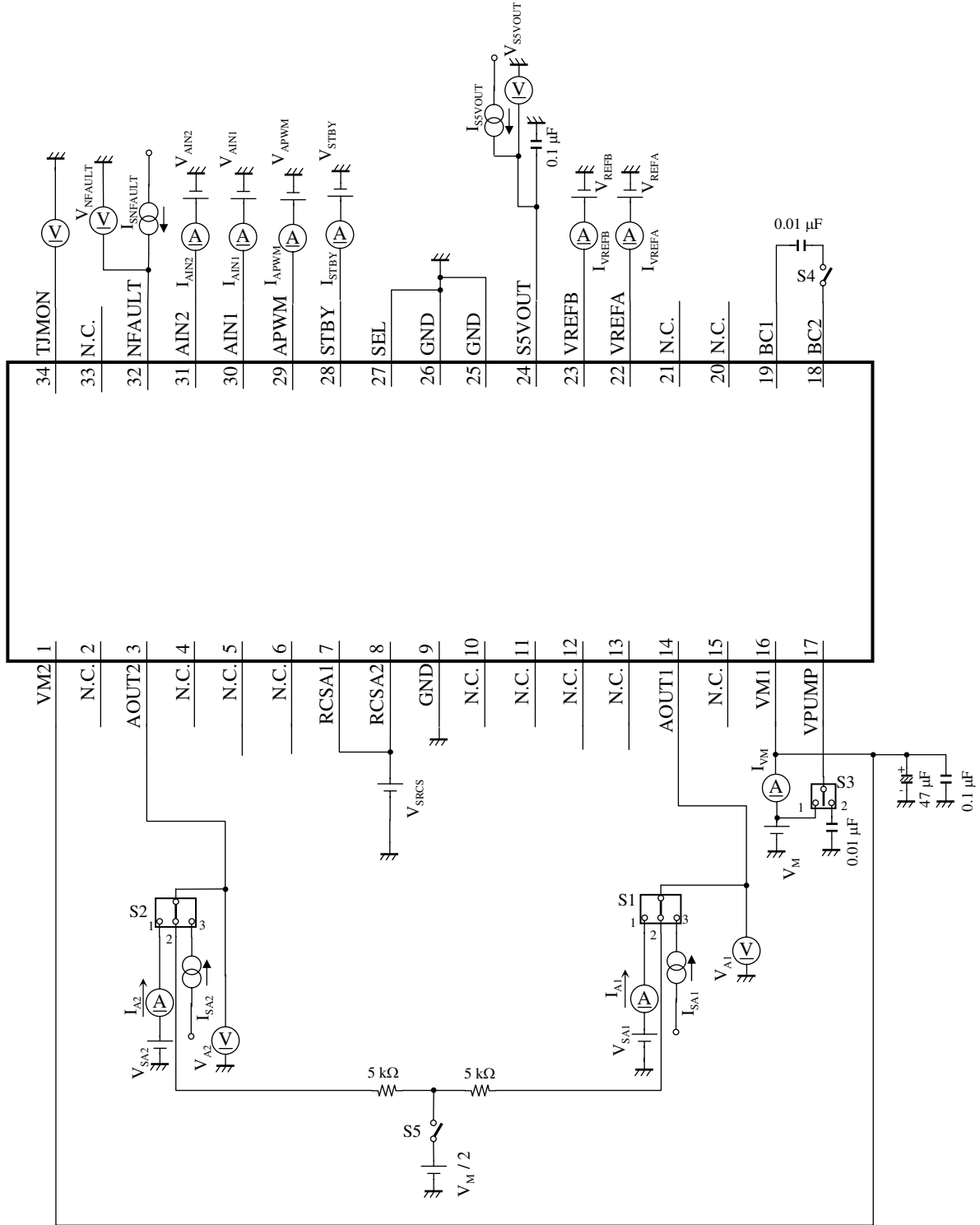
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Note
					Min	Typ	Max		
<b>Output drivers</b>									
29	Output slew rate 1	$VT_r$	—	Rising edge	—	270	—	V/ $\mu\text{s}$	—
30	Output slew rate 2	$VT_f$	—	Falling edge	—	330	—	V/ $\mu\text{s}$	—
31	Dead time	$T_D$	—	—	—	0.45	—	$\mu\text{s}$	—
<b>Thermal protection</b>									
32	Thermal protection operating temperature	$TSD_{on}$	—	—	—	150	—	$^\circ\text{C}$	—
33	Thermal protection hysteresis width	$\Delta TSD$	—	—	—	40	—	$^\circ\text{C}$	—
<b>Low voltage protection</b>									
34	Protection operating voltage	UVLO1	—	—	—	8.0	—	V	—
35	Protection release voltage	UVLO2	—	—	—	8.6	—	V	—

2007-11-12		
Established	Revised	

■ Test Circuit Diagram

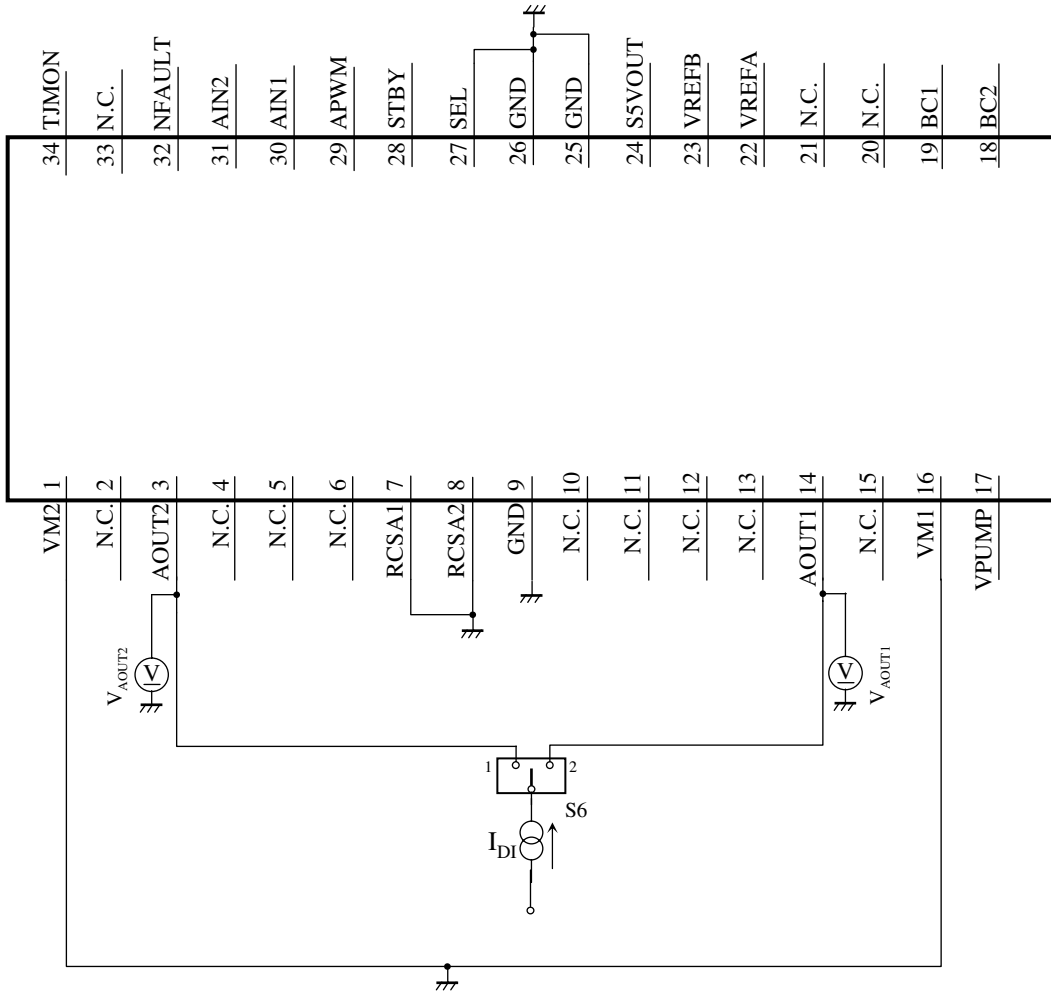
1. Test Circuit Diagram1



2007-11-12		
Established	Revised	

■ Test Circuit Diagram (continued)

2. Test Circuit Diagram2



C No.	Measuring Pin	Relay Conditions	Voltage Conditions
		S6	$I_{D1}$
3	3	1	1 A
			-1 A
	14	2	1 A
			-1 A

2007-11-12		
Established	Revised	

		<h1>Product Standards</h1>											<h2>AN44075A</h2>	
													Total Pages	Page
		30	14											

### ■ Electrical Characteristics Test Procedures

#### 1. Test Circuit 1

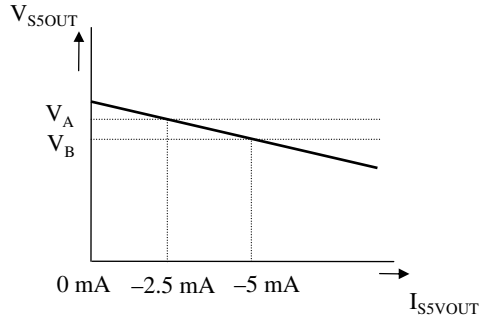
C No.	Measuring Pin	Relay Conditions				Voltage Conditions													
		S1 S2	S3	S4	S5	V <sub>STBY</sub>	V <sub>APWM</sub>	V <sub>AIN1</sub>	V <sub>AIN2</sub>	V <sub>REFA</sub>	V <sub>REFB</sub>	V <sub>SRCs</sub>	V <sub>SA1</sub> V <sub>SA2</sub>	V <sub>M</sub>	I <sub>SA1</sub>	I <sub>SA2</sub>	I <sub>FAULT</sub>	I <sub>SSVOUT</sub>	
1 2	3, 14	3	2	on	off	5 V	5 V	5 V	5 V	5 V	5 V	0 V	Hi-Z	24 V	-1.0 A	1.0 A	Hi-Z	Hi-Z	
		3	2	on	off	5 V	5 V	0 V	5 V	5 V	5 V	0 V	Hi-Z	24 V	1.0 A	-1.0 A	Hi-Z	Hi-Z	
4	3, 14	1	1	off	off	5 V	0 V	5 V	5 V	5 V	5 V	0 V	37 V	37 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
		1	1	off	off	5 V	0 V	5 V	0 V	5 V	5 V	0 V	0 V	37 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
5	1, 16	3	2	on	off	0 V	5 V	5 V	0 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
6	1, 16	3	2	on	off	5 V	5 V	5 V	0 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
7	24	3	2	on	off	5 V	5 V	5 V	0 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	-2.5 mA	
8	24	3	2	on	off	5 V	5 V	5 V	0 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	-5 mA	
9 17	3, 14	2	2	on	off	5 V	2.1 V	2.1 V	2.1 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
10 17	3, 14	2	2	on	off	5 V	2.1 V	0.6 V	2.1 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
9 18	3, 14	2	2	on	off	5 V	0.6 V	0.6 V	2.1 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
10 18	3, 14	2	2	on	off	5 V	0.6 V	0.6 V	0.6 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
11 15 19	28, 29, 30, 31	3	2	on	off	5 V	5 V	5 V	5 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
12	29, 30, 31	3	2	on	off	5 V	0 V	0 V	0 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
13	3, 14	2	2	on	off	2.1 V	5 V	5 V	5 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
14	3, 14	2	2	on	off	0.6 V	5 V	5 V	5 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
16	28	3	2	on	off	0 V	0 V	0 V	0 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
21	3	2	2	on	off	5 V	Pulse	5 V	5 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
22	3	2	2	on	off	5 V	Pulse	5 V	5 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
23	22, 23	3	2	on	off	5 V	5 V	5 V	5 V	5 V	5 V	0 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
24	3	2	2	on	on	5 V	5 V	5 V	5 V	0 V	5 V	1 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
25	3	2	2	on	on	5 V	5 V	5 V	5 V	0 V	5 V	1 V	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
26	3	2	2	on	off	5 V	5 V	5 V	5 V	5 V	5 V	Sweep	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
27	14	2	2	on	off	5 V	5 V	5 V	5 V	5.5 V	2.5 V	Sweep	Hi-Z	24 V	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
28	32	2	2	on	off	5 V	5 V	5 V	5 V	5 V	0 V	1 V	Hi-Z	24 V	Hi-Z	Hi-Z	1 mA	Hi-Z	

2007-11-12		
Established	Revised	

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

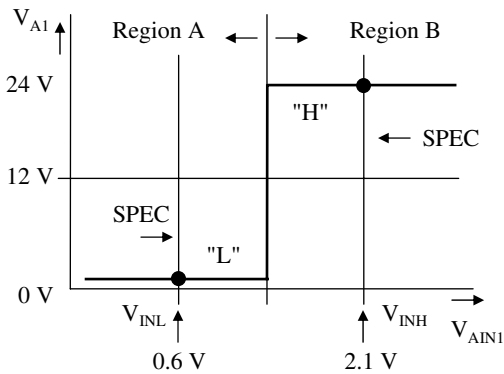
8) Output impedance  $Z_{SSVOUT}$



$$Z_{SSVOUT} = \frac{V_A - V_B}{2.5 \text{ mA}}$$

9) High-level IN input voltage  $V_{INH}$

10) Low-level IN input voltage  $V_{INL}$



Check the conditions by measuring the AOUT1 voltage, AOUT2 voltage with the input voltage set to high level and low level respectively.

Region A : The Power transistor on the flow-in side turned on.  
Another Power transistor on the flow-out side turned off.

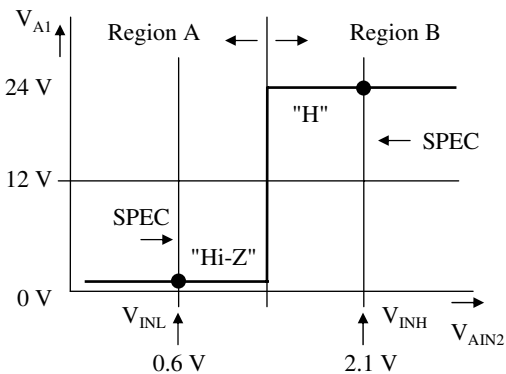
Region B : The Power transistor on the flow-in side turned off.  
Another Power transistor on the flow-out side turned on.

Measuring Pin	Voltage Conditions		Status
	$V_{AIN1}$	$V_{AIN2}$	
$V_{AOUT1}$	2.1 V	2.1 V	"H" output
	0.6 V	2.1 V	"L" output
$V_{AOUT2}$	2.1 V	2.1 V	"L" output
	0.6 V	2.1 V	"H" output

Check the conditions by measuring the AOUT1 voltage, AOUT2 voltage with the input voltage set to high level and low level respectively.

Region A : The Power transistor on the flow-in side turned off.  
Another Power transistor on the flow-out side turned off.

Region B : The Power transistor on the flow-in side turned off.  
Another Power transistor on the flow-out side turned on.



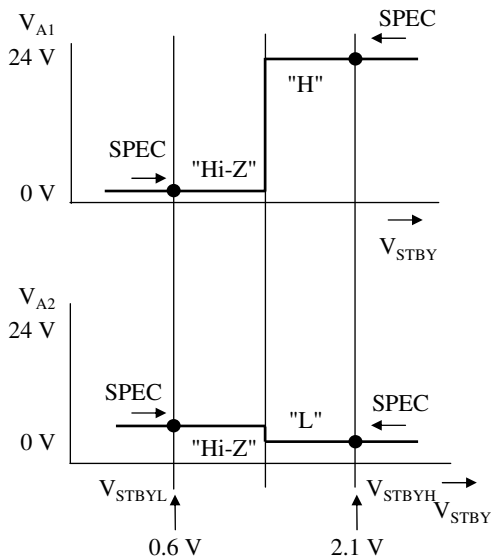
Measuring Pin	Voltage Conditions		Status
	$V_{AIN1}$	$V_{AIN2}$	
$V_{AOUT1}$	0.6 V	2.1 V	"H" output
	0.6 V	0.6 V	"Hi-Z" output
$V_{AOUT2}$	0.6 V	2.1 V	"H" output
	0.6 V	0.6 V	"Hi-Z" output

2007-11-12		
Established	Revised	

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

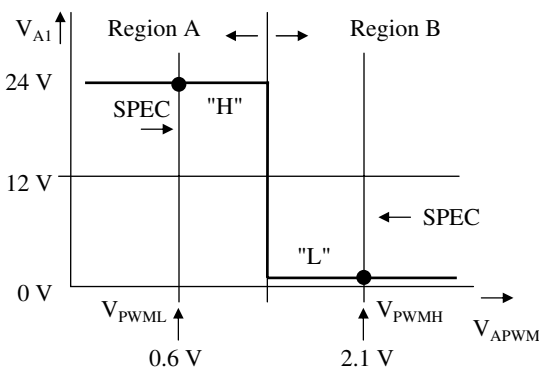
- 13) High-level STBY input voltage  $V_{STBYH}$
- 14) Low-level STBY input voltage  $V_{STBYL}$



Check the conditions by measuring the AOUT1 voltage, AOUT2 voltage with the input voltage set to high level and low level respectively.

Measuring Pin	Voltage Conditions	Status
	$V_{STBY}$	
$V_{AOUT1}$	0.6 V	"Hi-Z" output
$V_{AOUT2}$	0.6 V	"Hi-Z" output
$V_{AOUT1}$	2.1 V	"H" output
$V_{AOUT2}$	2.1 V	"L" output

- 17) High-level PWM input voltage  $V_{PWML}$
- 18) Low-level PWM input voltage  $V_{PWHM}$



Check the conditions by measuring the AOUT1 voltage with the input voltage set to high level and low level respectively.

Measuring Pin	Voltage Conditions	Status
	$V_{APWM}$	
$V_{AOUT1}$	0.6 V	"H" output
	2.1 V	"L" output

Region A : The Power transistor on the flow-in side turned off.  
Another Power transistor on the flow-out side turned on.

Region B : The Power transistor on the flow-in side turned on.  
Another Power transistor on the flow-out side turned off.

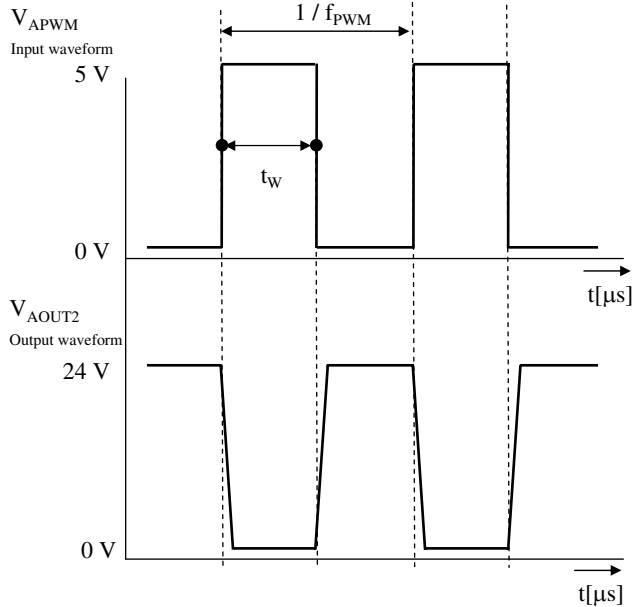
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■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

- 21) PWM Input Max frequency  $f_{PWM}$
- 22) Input Min pulse width  $t_w$



$V_{APWM} = \text{Pulse}$

Check the conditions by measuring the AOUT2 voltage waveform.

PWM Input Pulse

	Pulse Conditions	Input waveform
	$V_{APWM}$	
Frequency	200 kHz	Square-wave pulse
Duty	40%	
Amplitude	5 V[p-p]	
Offset	2.5 V	

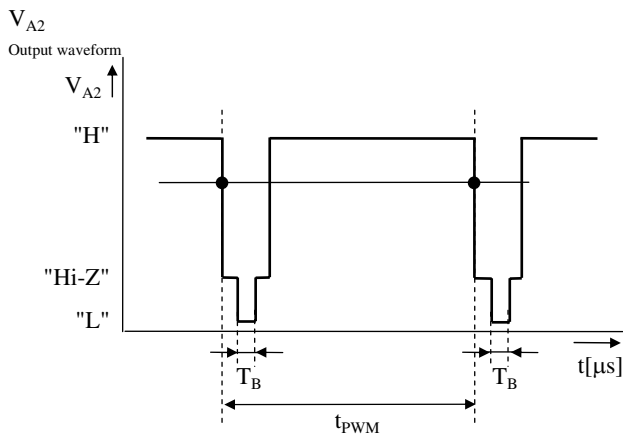
PWM Input Max Frequency  $f_{PWM}$

Check the conditions by measuring the cycle time of output voltage pulses.

Input Min pulse width  $t_w$

Check the conditions by measuring the Duty of output voltage pulses.

- 24) PWM frequency 1  $f_{PWM}$
- 25) Pulse blanking time  $T_B$



The value is obtained from  $V_{A2}$  voltage at  $V_{REFA} = 0\text{ V}$ ,  $V_{REFB} = 5\text{ V}$ ,  $A1N1 = 5\text{ V}$ .

The  $V_{A2}$  output waveform is shown below.

PWM Frequency  $f_{PWM}$

Measure the cycle time of output voltage pulses and obtain the value from the following formula.

$$f_{PWM} = \frac{1}{t_{PWM}}$$

Pulse blanking time  $T_B$

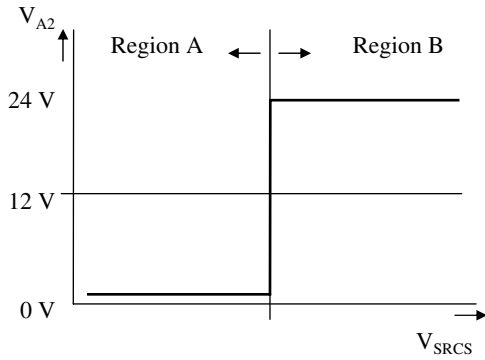
Measure the time of  $V_{A2}$  output voltage low level.

2007-11-12		
Established	Revised	

■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

26) Comp threshold 1  $V_{TH1}$



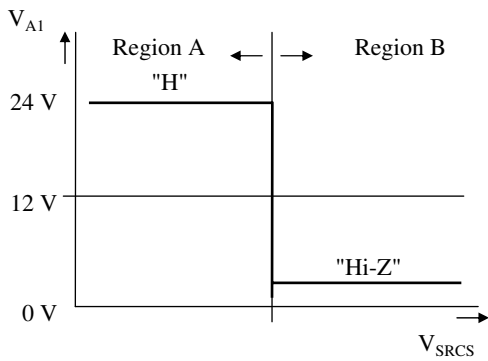
Make RCS voltage sweep and measure threshold voltage of output pins.

Region A : Always output "L"  
 Region B : Min. duty, output "L"



27) Comp threshold 2

$V_{TH2}$



Make RCS voltage sweep and measure threshold voltage of output pins.

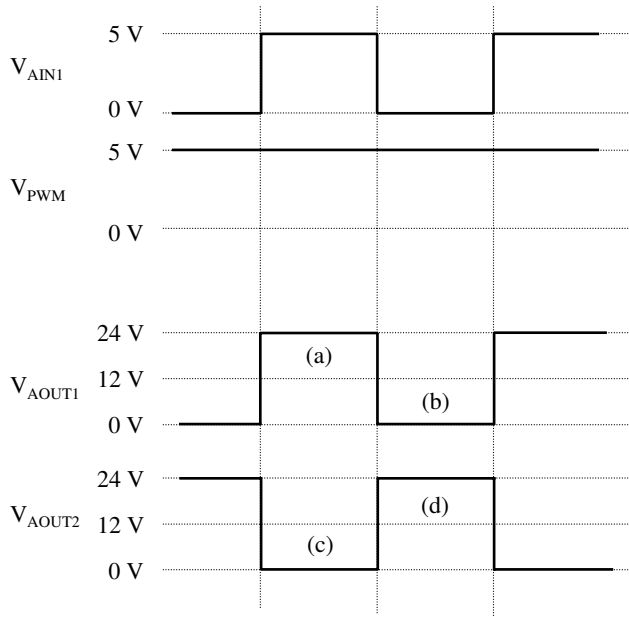
Region A : Always output "H"  
 Region B : Output "Hi-Z"

2007-11-12		
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■ Electrical Characteristics Test Procedures (continued)

1. Test Circuit 1 (continued)

- 1) High-level output saturation voltage  $V_{OH}$
- 2) Low-level output saturation voltage  $V_{OL}$



C No.	Measuring Pin	Current Conditions	Status
		$I_{SA1}, I_{SA2}$	
1	AOUT1 / AOUT2	-1.0 A	Measure each voltage of the AOUT1 and AOUT2 at (a) , (d) above
2	AOUT1 / AOUT2	1.0 A	Measure each voltage of the AOUT1 and AOUT2 at (c) , (b) above

2. Test Circuit 2

- 3) Flywheel diode forward voltage  $V_{DI}$

C No.	Measuring Pin	Relay Conditions
		S6
3	AOUT1 / AOUT2	Measure the diode voltage at each level on contacts1, 2 of S6.

2007-11-12		
Established	Revised	

		<h1>Product Standards</h1>		<h2>AN44075A</h2>	
				Total Pages	Page
				30	20

■ Technical Data

- Circuit diagrams of the input/output part and pin function descriptions

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
3 7 8 14	—		—	Pin 7 : Current detection 1 8 : Current detection 2 3 : Motor drive output 2 14 : Motor drive output 1
17 18	—		—	Pin 18 : Charge Pump capacitor 2 17 : Charge Pump circuit output

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	21

■ Technical Data (continued)

- Circuit diagrams of the input/output part and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
19	—		—	Pin 19 : Charge Pump capacitor 1
22	—		50 kΩ	Pin 22 : Peak current setting input

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	22

■ Technical Data (continued)

- Circuit diagrams of the input/output part and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
23	—		50 kΩ	Pin 23 : Load short threshold input
24	—		—	Pin 24 : Internal reference voltage (5 V output)

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	23

■ Technical Data (continued)

- Circuit diagrams of the input/output part and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
28	—		100 kΩ	Pin 28 : Standby input
27 29	—		54 kΩ	Pin 27 : Test mode input 29 : PWM input

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	24

■ Technical Data (continued)

- Circuit diagrams of the input/output part and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
30 31	—		—	Pin 30 : Forward / Reverse input 31 : Brake mode input
32	—		—	Pin 32 : Abnormal detection output

2007-11-12		
Established	Revised	



	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	25

■ Technical Data (continued)

- Circuit diagrams of the input/output part and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
34	—		—	Pin 34 : VBE monitor
Sym bols	—	<ul style="list-style-type: none"> <li> S5VOUT (Pin 24)</li> <li> VM (Pin 1, Pin 16)</li> <li> Diode</li> <li> Zener diode</li> <li> Ground</li> </ul>	—	—

2007-11-12		
Established	Revised	

	Product Standards	AN44075A	
		Total Pages	Page
		30	26

- Technical Data (continued)
  - Control mode (truth table)

INPUT				OUTPUT		
STBY	AIN1	AIN2	APWM	AOUT1	AOUT2	Mode
"H"	—	"H"	"L"	"H"	"H"	Short Brake
	"L"	—	"H"	"L"	"H"	Forward
	"H"	—	"H"	"H"	"L"	Reverse
	—	"L"	"L"	OFF	OFF	Stop
"L"	—	—	—	OFF	OFF	Standby

INPUT	OUTPUT
SEL	Mode
"H"	Short Detect off
"L"	Short Detect on

2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	27

### ■ Usage Notes

#### • Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [DC motor with brass].  
Consult our sales staff in advance for information on the following applications:
  - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
  - Any applications other than the standard applications intended.
    - (1) Space appliance (such as artificial satellite, and rocket)
    - (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
    - (3) Medical equipment for life support
    - (4) Submarine transponder
    - (5) Control equipment for power plant
    - (6) Disaster prevention and security device
    - (7) Weapon
    - (8) Others : Applications of which reliability equivalent to (1) to (7) is required
2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin- $V_M$  short (Power supply fault), output pin-GND short (Ground fault), output-to-output-pin short (load short) or the leakage between pins.  
Pay special attention to the following pins so that are not short-circuited with the  $V_M$  pin, ground pin, other output pins or RCS pin.
  - (1) AOUT1 (Pin 14), AOUT2 (Pin 3)
  - (2) BC1 (Pin 19), BC2 (Pin 18), VPUMP (Pin 17)
  - (3) VM1 (Pin 16), VM2 (Pin 1), S5VOUT (Pin 24)
  - (4) RCSA1 (Pin 7), RCSA2 (Pin 8)
 And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
6. When using the LSI for new models, verify the safety including the long-term reliability for each product.
7. When the application system is designed by using this LSI, be sure to confirm notes in this book.  
Be sure to read the notes to descriptions and the usage notes in the book.
8. Please connect the metallic plate (fin) on the back side of the IC with the GND potential (the pattern for cooling).
9. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.  
Especially the thermal protection circuit might be damaged before it could operate if the area of safety operation of the device or the absolute maximum rating is instantaneously exceeded due to the output pin to  $V_M$  short (Power supply fault), or output pin to GND short (Ground fault) .
10. Unless specified in the product specifications, make sure the negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil, optical pick-up or transformer is being driven.
11. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.
12. Check the risk that is caused by the failure of external components.

2007-11-12		
Established	Revised	

<h1 style="margin: 0;">Product Standards</h1>		<h2 style="margin: 0;">AN44075A</h2>	
		Total Pages	Page
		30	28

■ Usage Notes (continued)

13. Perform thermal design work with consideration of a sufficient margin to keep the power dissipation based on supply voltage, load, and ambient temperature conditions.

(The IC is recommended that junctions are designed below 70% to 80% of Absolute Maximum Rating.)

14. Set the values of the capacitor between the VPUMP and GND pins so that the voltage on the VPUMP (Pin 17) will not transiently exceed 43 V in the transition from motor standby to motor start.

15. This IC employs a PWM drive method that switches the high-current output of the output transistor. Therefore, the IC is apt to generate noise that may cause the IC to malfunction or have fatal damage. To prevent these problems, the power supply must be stable enough. Therefore, the capacitance between the S5VOUT and GND pins must be a minimum of 0.1 μF and the one between the VM and GND pins must be a minimum of 47 μF and as close as possible to the IC so that PWM noise will not cause the IC to malfunction or have fatal damage.

16. A high current flows into the IC. Therefore, the common impedance of the PCB pattern cannot be ignored. Take the following points into consideration and design the PCB pattern of the motor.

A high current flows into the line between the VM1 (Pin 16) and VM2 (Pin 1) pins. Therefore, noise is generated with ease at the time of switching due to the inductance (L) of the line, which may result in the malfunctioning or destruction of the IC (see the circuit diagram 1). As shown in the circuit diagram 2, the escape way of the noise is secured by connecting a capacitor to the connector close to the VM pin of the IC. This makes it possible to suppress the direct VM pin voltage of the IC. Make the settings as shown in the circuit diagram 2 as much as possible.

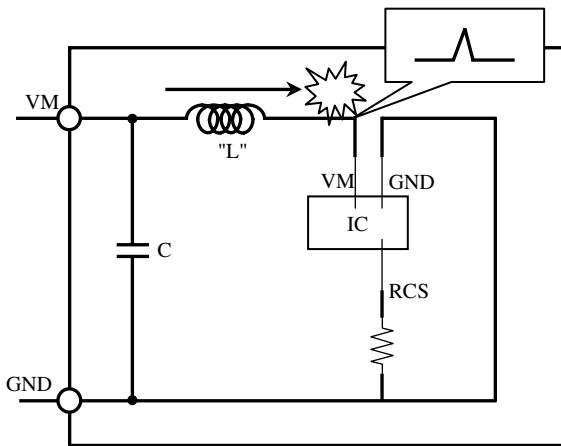


Diagram 1. Unrecommended pattern

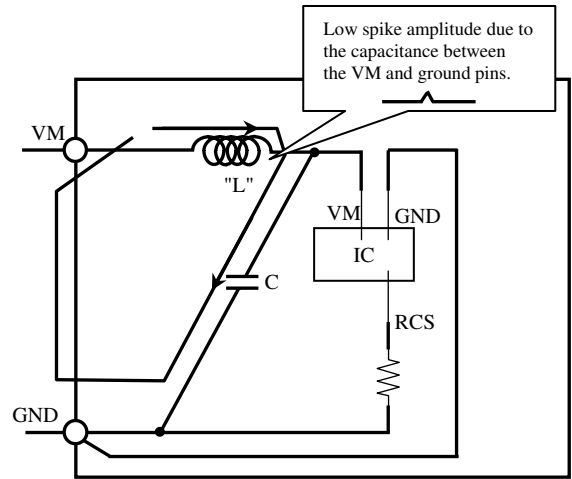
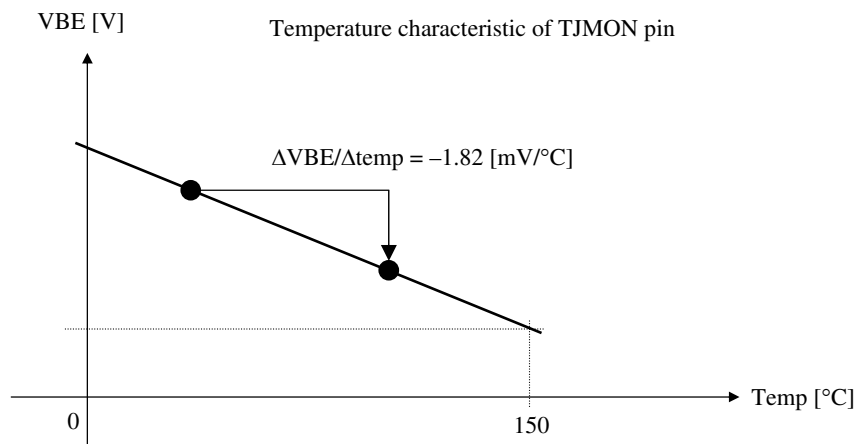


Diagram 2. Recommended pattern

17. In the case of measuring the chip temperature of the IC, measure the voltage of TJMON (Pin 34) and presume chip temperature from following data. Use the following data as reference data. Before applying the IC to a product, conduct a sufficient reliability test of the IC along with the evaluation of the product with the IC incorporated.



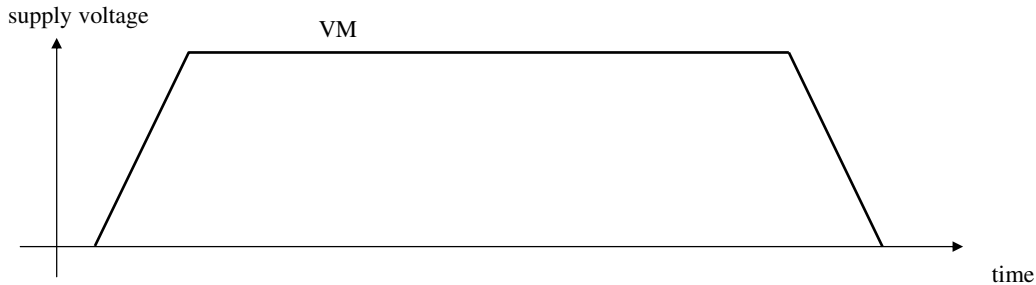
2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	29

■ Usage Notes (continued)

18. Power Supply Sequence

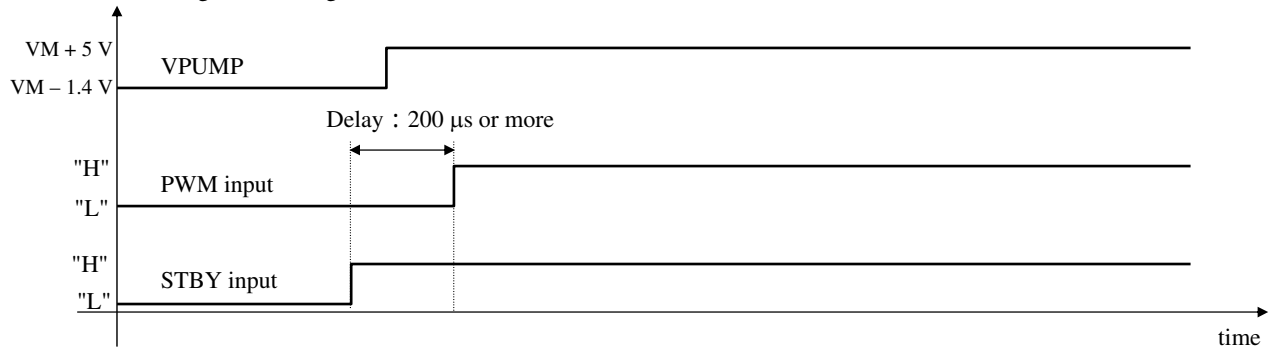
Rise/Fall slew rate are designed,  $V_M$  : below  $0.1V/\mu s$ .



19. Charge pump circuit

The charge pump circuit has stopped when the Low signal is input to STBY (Pin 28).

The start time is necessary until the charge pump circuit begins operating. Please take the wait time of  $200 \mu s$  or more until the motor starts rotating after making IC active.



20. PWM operation

When Free Run Mode and Forward/Reverse Mode is repeated in PWM operation, the backflow current flows from GND toward  $V_M$  in Free Run Mode. Please add external capacity so as not to exceed the absolute maximum rating of  $V_M$ .

Also, when Free Run Mode and Forward/Reverse Mode is repeated in PWM operation, the duty of the output is extremely different from the duty of the input.

21. Thermal protection circuit

The operation point and hysteresis of the thermal protection circuit of the IC have about  $\pm 10^\circ C$  of variation.

Also, the protection circuit is incorporated for the purpose of securing safety if the IC malfunctions. Therefore design a protection circuit so that a protection circuit will not operate under a normal operating condition.

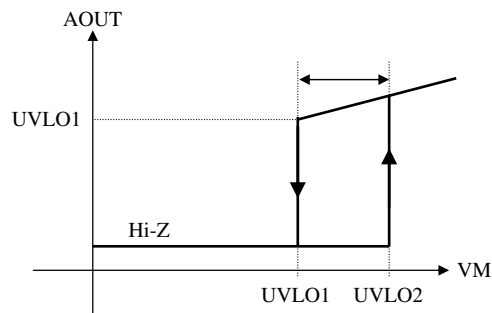
22. Low voltage detection circuit

The threshold of low voltage detection circuit of the IC is below,

Detection voltage (UVLO1) : Min = 7.1 V

Release voltage (UVLO2) : Max = 9.5 V

In case of less than the detection voltage, the power transistor of the motor output pins ( AOUT1, AOUT2) on the flow-in side and another power transistor on the flow-out side turn off.



2007-11-12		
Established	Revised	

	<h1>Product Standards</h1>	<h2>AN44075A</h2>	
		Total Pages	Page
		30	30

■ Usage Notes (continued)

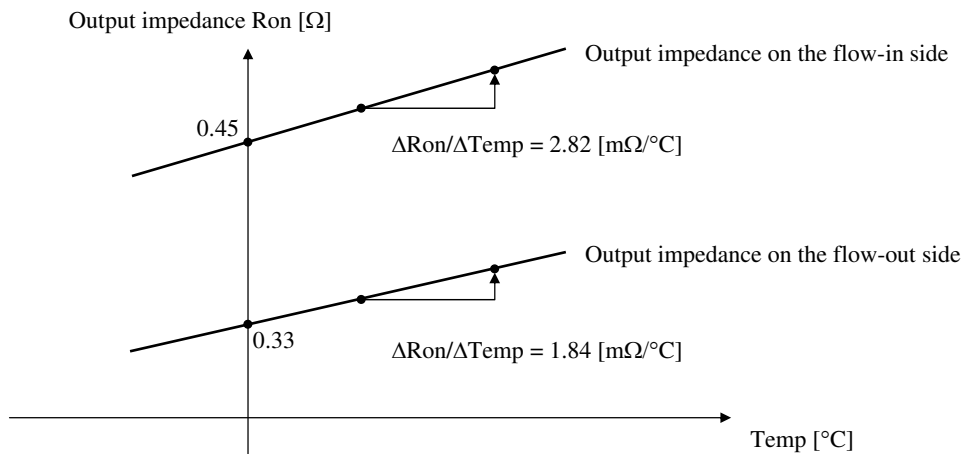
23. Operation within Supply Voltage Range

About Parameters from No.9 to No.28 in Electrical Characteristics, It is possible to gain characteristics described in Electrical Characteristics if operating within Supply Voltage Range (10 V to 35 V).

24. Temperature dependence of output impedance of motor drive output pins

Output impedance of motor drive output pins (Pin 3, 14) have temperature dependence below.

The characteristics below are reference values derived from the design of the IC and are not guaranteed by inspection. Conduct a sufficient reliability test of the IC along with the evaluation of the product with the IC incorporated.



25. No connected pins

When no connected pins (Pin 2, 4, 6, 13, 15, 20, 33) are connected to the GND pin, adjacent pin short or reverse insertion may cause destruction and smoke generation. Therefore, design the PCB pattern so that the above no connected pins are opened on the PCB pattern. There is no problem that no connected pins (Pin5, 10, 11, 12, 21) except for the above-mentioned pins are connected to the GND pin.

26. AOUT1 and AOUT2 pins after operation of the protection circuit of the IC

This IC has built-in thermal protection circuit, low voltage detection circuit and over current detection circuit.

AOUT1 and AOUT2 pins operate as below after each protection circuit operates,

**Thermal protection circuit :** In operating, the power transistor of AOUT1 and AOUT2 pins on the flow-in side and another power transistor on the flow-out side turn off. If the temperature of the IC lowers above thermal protection hysteresis width, AOUT1 and AOUT2 pins recover in normal operation automatically.

**Low voltage detection circuit :** In operating, the power transistor of AOUT1 and AOUT2 pins on the flow-in side and another power transistor on the flow-out side turn off. If VM pin voltage exceeds protection release voltage, AOUT1 and AOUT2 pins recover in normal operation automatically.

**Over current detection circuit :** In operating, the power transistor of AOUT1 and AOUT2 pins on the flow-in side and another power transistor on the flow-out side turn off, and keep this status latched. If over current detection circuit operates, reset the circuit by inputting low voltage to STBY pin or setting VM pin voltage to less than protection operating voltage.

27. Peak current detection and over current detection

Peak current detection values and over current detection values are obtained by following formula.

$$I_{\text{peak1}} = 0.1 \times V_{\text{REFA}} / R_{\text{CS}}[\text{A}]$$

$$I_{\text{peak2}} = 0.2 \times V_{\text{REFB}} / R_{\text{CS}}[\text{A}]$$

$I_{\text{peak1}}$  : Peak current detection value

$I_{\text{peak2}}$  : Over current detection value

$V_{\text{REFA}}$  : VREFA pin applied voltage

$V_{\text{REFB}}$  : VREFB pin applied voltage

$R_{\text{CS}}$  : RCSA1 / resistive connection between RCSA2 and GND pins

2007-11-12		
Established	Revised	

# PACKAGE STANDARDS

Package Code

HSOP034-P-0300A

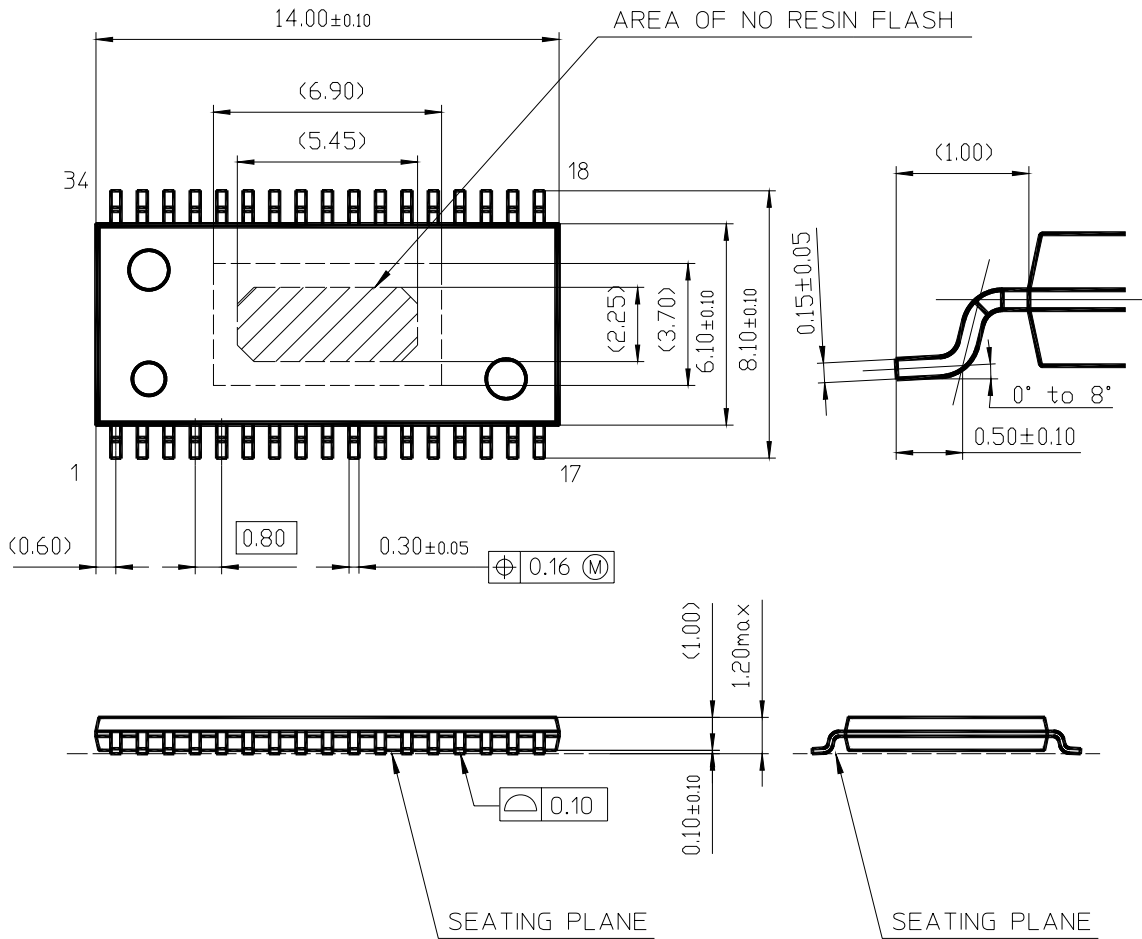
Semiconductor Company  
Matsushita Electric Industrial Co., Ltd.

Established by	Applied by	Checked by	Prepared by
K.Komichi	H.Yoshida	M.Okajima	M.Itoh

	<b>PACKAGE STANDARDS</b>	
	<b>HSOP034-P-0300A</b>	
	Total Pages	Page
	6	2

**1. Outline Drawing**

Unit:mm

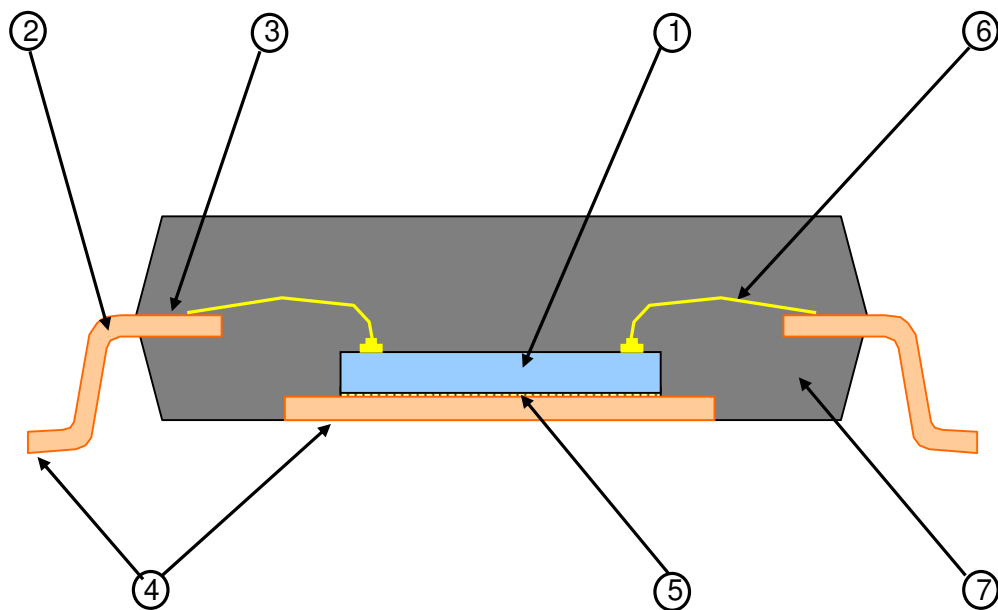


Body Material	: Epoxy Resin
Lead Material	: Cu Alloy
Lead Finish Method	: Pd Plating



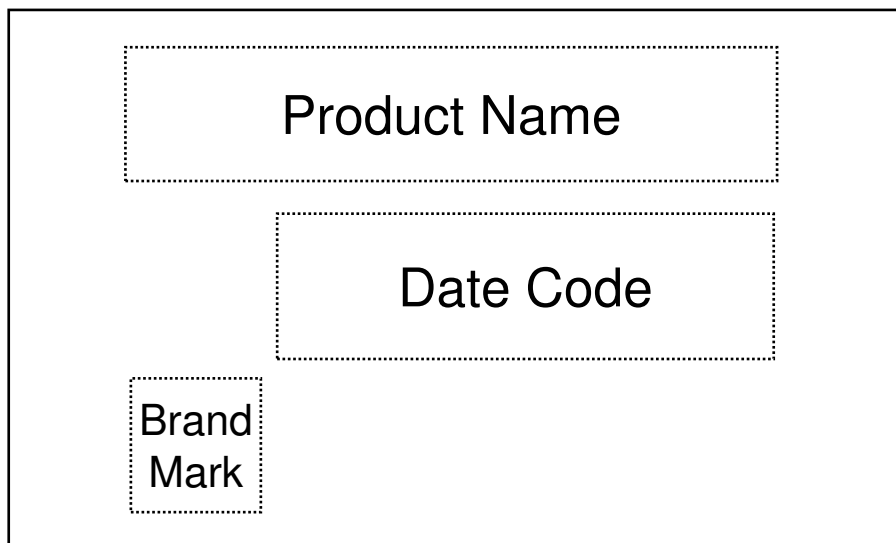
2. Package Structure (Technical Report : Reference Value)

Chip Material		Si	①
Leadframe material		Cu alloy	②
Inner lead surface		Pd plating	③
Outer lead surface		Pd plating	④
Chip mount	Method	Resin adhesive method	⑤
	Material	Adhesive material	
Wirebond	Method	Thermo-compression bonding	⑥
	Material	Au	
Molding	Method	Transfer molding	⑦
	Material	Epoxy resin	
Mass		250 mg	



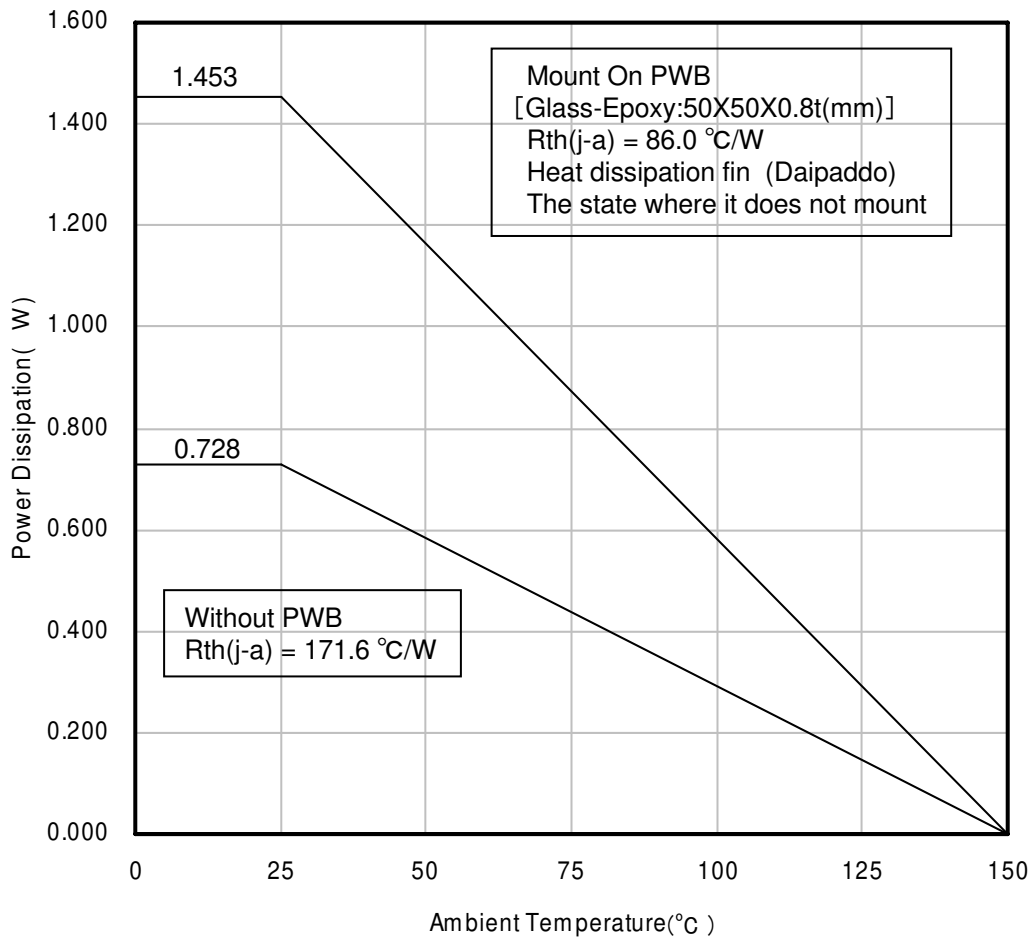
	<b>PACKAGE STANDARDS</b> HSOP034-P-0300A		
		Total Pages	Page
		6	4

3. Mark Drawing



	<b>PACKAGE STANDARDS</b> <b>HSOP034-P-0300A</b>		
		Total Pages	Page
		6	5

4. Power Dissipation (Technical Report)



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**5. Power Dissipation (Supplementary Explanation)**

**[Experiment environment]**

Power Dissipation (Technical Report) is a result in the experiment environment of SEMI standard conformity. (Ambient air temperature (Ta) is 25 degrees C)

**[Supplementary information of PWB to be used for measurement]**

The supplement of PWB information for Power Dissipation data (Technical Report) are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

**[Notes about Power Dissipation (Thermal Resistance) ]**

Power Dissipation values (Thermal Resistance) depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value (Technical Report) is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

**[Definition of each temperature and thermal resistance]**

Ta : Ambient air temperature

※ The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc : It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj : Semiconductor element surface temperature (Junction temperature.)

Rth(j-c) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a) : The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

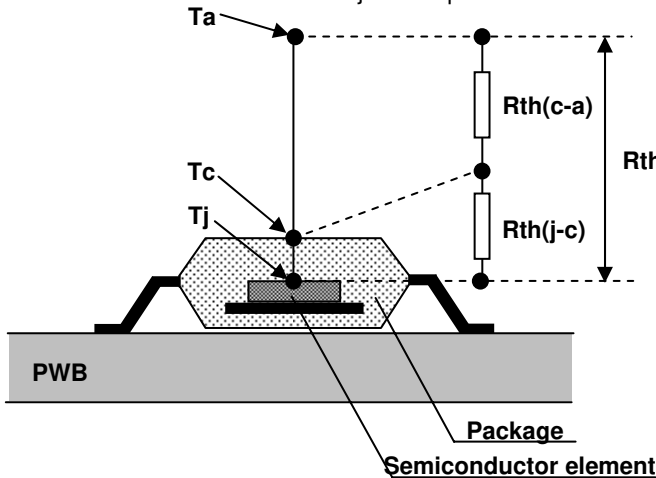


Fig1. Definition image

**[Definition formula]**

$$T_j = \{R_{th}(j-c) + R_{th}(c-a)\} \times P + T_a$$

$$= R_{th}(j-a) \times P + T_a$$

$$R_{th}(j-c) = \frac{T_j - T_c}{P} \quad (^\circ\text{C/W})$$

$$R_{th}(c-a) = \frac{T_c - T_a}{P} \quad (^\circ\text{C/W})$$

$$R_{th}(j-a) = \frac{T_j - T_a}{P} \quad (^\circ\text{C/W})$$

$$= R_{th}(j-c) + R_{th}(c-a)$$

P:power(W)