

# KA7630/KA7631

## Fixed Multi-Output Regulator

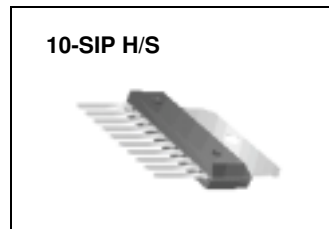
### Features

- Output Currents up to 0.5A (Output1 & 2)
- Output Current up to 1A with External Transistor (Output3)
- Fixed Precision Output 1 Voltage 5.1V  $\pm 2\%$
- Fixed Precision Output 2 Voltage 8V  $\pm 2\%$  (KA7630)
- Fixed Precision Output 2 Voltage 9V  $\pm 2\%$  (KA7631)
- Control Signal Generator for Output 3 Voltage (12V  $\pm 2\%$ )
- Reset Facility for Output Voltage1
- Output 2,3 with Disable by TTL Input
- Current Limit Protection at Each Output
- Thermal Shut Down

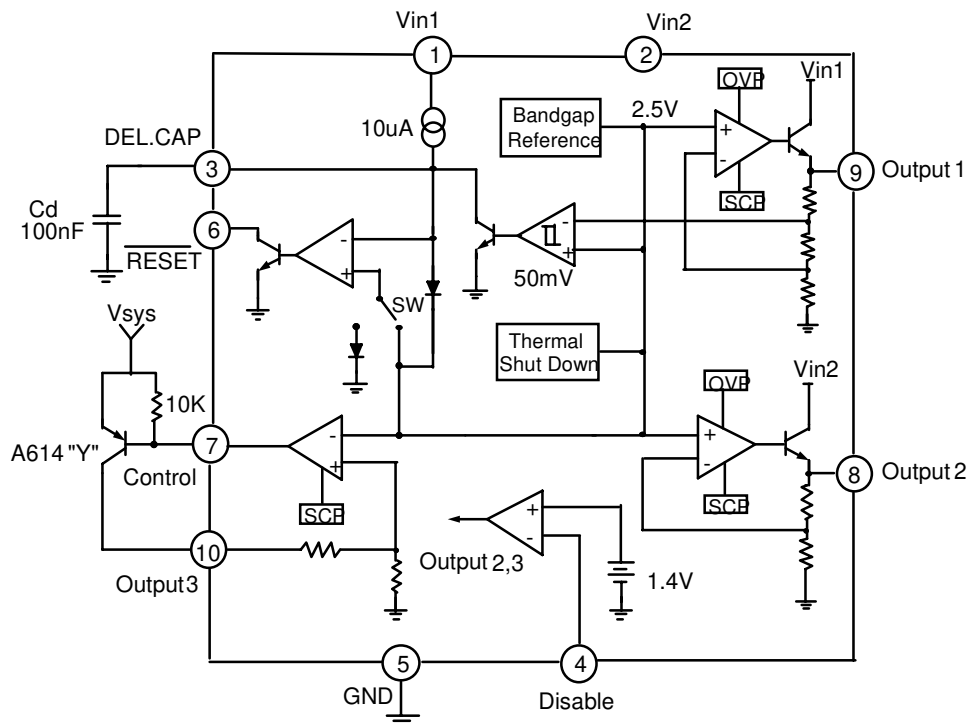
### Description

The KA7630/KA7631 is a multi-output positive voltage regulator designed to provide fixed precision output voltages of 5.1V, 8V (7630) / 9V(7631) at current up to 0.5A and 12V at current up to 1A with external PNP transistor.

An internal reset circuit generates a reset pulse when the output 1 decreases below the regulated value. Output2 & 3 can be disabled by TTL input. Protection features include over voltage protection, short circuit protection and thermal shutdown.



### Internal Block Diagram



## Absolute Maximum Ratings

| Parameter             | Symbol | Value    | Unit | Remark      |
|-----------------------|--------|----------|------|-------------|
| DC Input Voltage      | Vin    | 20       | V    | -           |
| Disable Input Voltage | Vc     | 20       | V    | -           |
| Output Current        | Io     | 0.5      | A    | -           |
| Power Dissipation     | Pd     | 1.5      | W    | No Heatsink |
| Junction Temperature  | Tj     | +150     | °C   | -           |
| Operating Temperature | Topr   | 0 ~ +125 | °C   | -           |

## Electrical Characteristics(KA7630)

(Refer to test circuit Vin1=7.5V ,Vin2=10.5V ,Tj = +25°C, unless otherwise specified)

| Parameter                             | Symbol  | Conditions   | Min.        | Typ.       | Max.        | Unit   |
|---------------------------------------|---------|--|-------------|------------|-------------|--------|
| Output Voltage 1                      | Vo1     | Io1 = 10mA<br>7.5V < Vin1 < 14V<br>5mA < Io1 < 500mA     | 5<br>4.9    | 5.1<br>5.1 | 5.2<br>5.3  | V      |
| Output Voltage 2                      | Vo2     | Io2 = 10mA<br>10.5V < Vin2 < 18V<br>5mA < Io2 < 500mA    | 7.84<br>7.7 | 8<br>8     | 8.16<br>8.3 | V      |
| Dropout Output Voltage 1,2            | Vd1,2   | Io1,2 = 500mA  | -           | -          | 2.5         | V      |
| Line Regulation 1,2                   | ΔVo 1,2 | 7.5V < Vin1 < 14V<br>10.5V < Vin2 < 18V<br>Io1,2 = 200mA | -           | -          | 50<br>80    | mV     |
| Load Regulation 1,2                   | ΔVo 1,2 | 5mA < Io1 < 500mA<br>5mA < Io2 < 500mA                   | -           | -          | 100<br>160  | mV     |
| Output Voltage 3                      | Vo3     | Vsys=13V, Io3=100mA                                      | 11.7        | 12         | 12.3        | V      |
| Line Regulation 3                     | ΔVo3    | 13V < Vin2 < 18V, Io3 = 100mA                            | -           | -          | 120         | mV     |
| Load Regulation 3                     | ΔVo3    | 5mA < Io3 < 1A   | -           | -          | 250         | mV     |
| Reset Pulse Delay                     | Trd     | Cd = 100nF, Note1  | -           | 25         | -           | ms     |
| Saturation Voltage in Reset Condition | VrL     | I6 = 5mA   | -           | -          | 0.4         | V      |
| Leakage Current at Pin 6              | IrH     | V6 = 10V   | -           | -          | 10          | μA     |
| Output Voltage Thermal Drift          | STt     | 0°C < Tj < +125°C , Note2                                | -           | 100        |             | ppm/°C |
| Short Circuit Output Current          | Isc1,2  | Vin1 = 7.5V , Vin2 = 10.5V                               | -           | -          | 1.6         | A      |
| Disable Voltage High                  | VdisH   | Output 2 Active  | 0.8         | -          | 2.0         | V      |
| Disable Voltage Low                   | VdisL   | Output 2 Disabled  | 0.8         | -          | 2.0         | V      |
| Disable Bias Current                  | Idis    | 0V < Vdis < 7V   | -100        | -          | 2           | μA     |
| Junction Temperature for TSD          | Ttsd    | Note 2   | -           | 145        | -           | °C     |
| Quiescent Current                     | Iq      | Io1 = 10mA, Output2 Disabled                             | -           | -          | 2           | mA     |
| Reset Threshold Voltage               | Vr      | K = Vo1  | K-0.4       | K-0.25     | K -0.1      | V      |
| Reset Threshold Hysteresis            | Vrth    | Note1  | 20          | 50         | 100         | mA     |

### Notes:

- To check the reset circuit ,the reset output is low to discharge the delay capacitor(=Cd), it's less than Vo1-0.25V. And the reset output is high when the delay capacitor voltage linearly increased by the internal current source(10μA) if it's more than Vo1- 0.2V. The equation of delay time is same as below. Trd = (Cd × 2.5) / 10μA
- These parameters, although guaranteed, are not 100% tested in production.

**Electrical Characteristics(KA7631)** (Continued)(Refer to test circuit  $V_{in1}=7.5V$  ,  $V_{in2}=11.5V$  ,  $T_j = +25^{\circ}C$ , unless otherwise specified)

| Parameter                             | Symbol           | Conditions   | Min.         | Typ.       | Max.         | Unit    |
|---------------------------------------|------------------|--|--------------|------------|--------------|---------|
| Output Voltage 1                      | Vo1              | Io1 = 10mA<br>7.5V < Vin1 < 14V<br>5mA < Io1 < 500mA     | 5<br>4.9     | 5.1<br>5.1 | 5.2<br>5.3   | V       |
| Output Voltage 2                      | Vo2              | Io2 = 10mA<br>11.5V < Vin2 < 18V<br>5mA < Io2 < 500mA    | 8.82<br>8.65 | 9<br>9     | 9.18<br>9.35 | V       |
| Dropout Output Voltage 1,2            | Vd1,2            | Io1,2 = 500mA  | -            | -          | 2.5          | V       |
| Line Regulation 1,2                   | $\Delta V_o$ 1,2 | 7.5V < Vin1 < 14V<br>11.5V < Vin2 < 18V<br>Io1,2 = 200mA | -            | -          | 50<br>80     | mV      |
| Load Regulation 1,2                   | $\Delta V_o$ 1,2 | 5mA < Io1 < 500mA<br>5mA < Io2 < 500mA                   | -            | -          | 100<br>160   | mV      |
| Output Voltage 3                      | Vo3              | Vsys = 13V, Io3 = 100mA                                  | 11.7         | 12         | 12.3         | V       |
| Line Regulation 3                     | $\Delta V_o3$    | 13V < Vin2 < 18V, Io3 = 100mA                            | -            | -          | 120          | mV      |
| Load Regulation 3                     | $\Delta V_o3$    | 5mA < Io3 < 1A   | -            | -          | 250          | mV      |
| Reset Pulse Delay                     | Trd              | Cd = 100nF, Note1  | -            | 25         | -            | ms      |
| Saturation Voltage in Reset Condition | VrL              | I6 = 5mA   | -            | -          | 0.4          | V       |
| Leakage Current at Pin 6              | IrH              | V6 = 10V   | -            | -          | 10           | $\mu A$ |
| Output Voltage Thermal Drift          | STt              | 0°C < Tj < +125°C , Note2                                | -            | 100        | -            | ppm/°C  |
| Short Circuit Output Current          | Isc1,2           | Vin1 = 7.5V , Vin2 = 11.5V                               | -            | -          | 1.6          | A       |
| Disable Voltage High                  | VdisH            | Output 2 Active  | 0.8          | -          | 2.0          | V       |
| Disable Voltage Low                   | VdisL            | Output 2 Disabled  | 0.8          | -          | 2.0          | V       |
| Disable Bias Current                  | Idis             | 0V < Vdis < 7V   | -100         | -          | 2            | $\mu A$ |
| Junction Temperature for TSD          | Ttsd             | Note2  | -            | 145        | -            | °C      |
| Quiescent Current                     | Iq               | Io1=10mA, Output2 Disabled                               | -            | -          | 2            | mA      |
| Reset Threshold Voltage               | Vr               | K = Vo1  | K-0.4        | K-0.25     | K -0.1       | V       |
| Reset Threshold Hysteresis            | Vrth             | Note1  | 20           | 50         | 100          | mA      |

**Notes:**

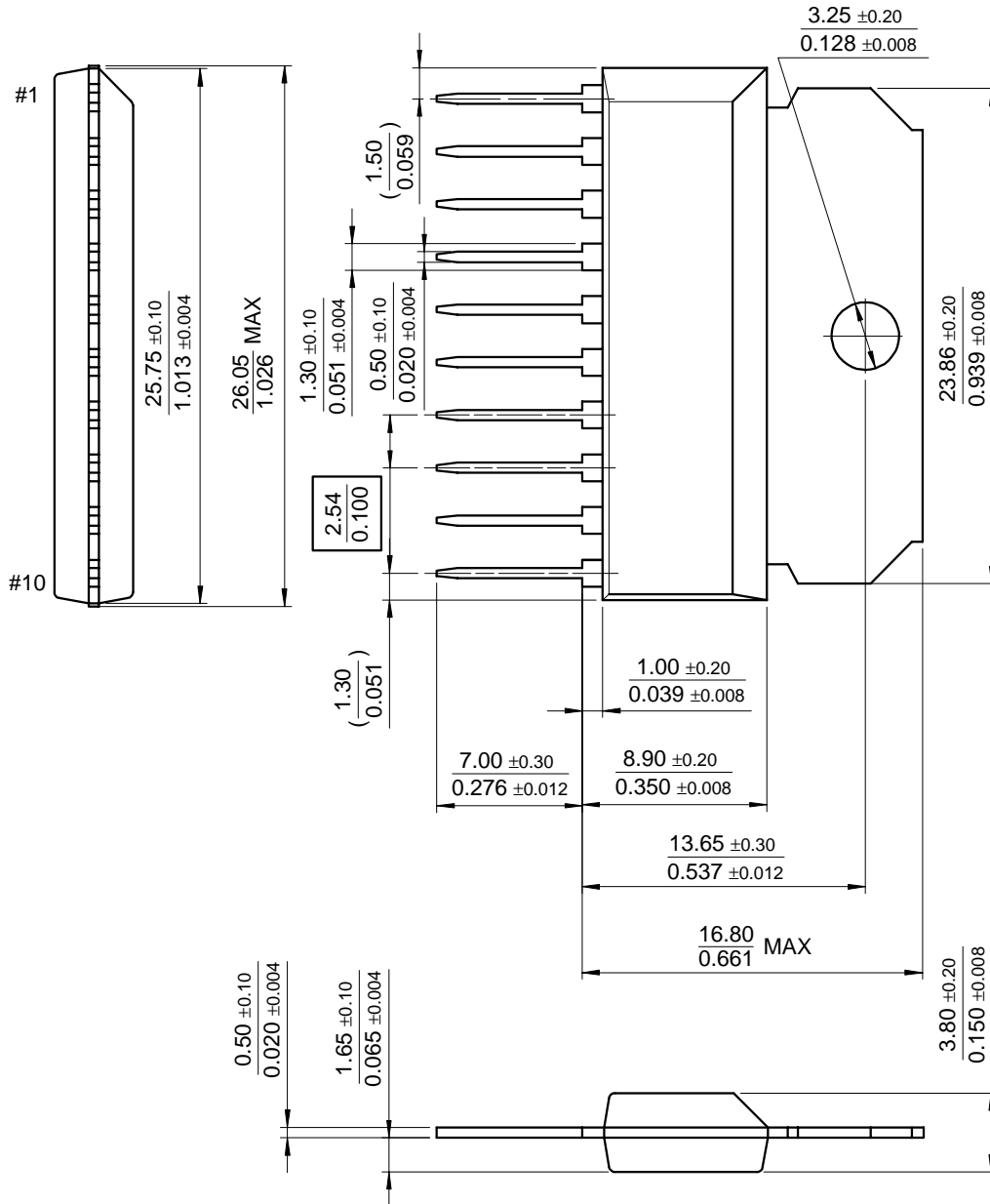
- To check the reset circuit ,the reset output is low to discharge the delay capacitor(=Cd). if it's less than Vo1-0.25V. And the reset output is high when the delay capacitor voltage linearly increased by the internal current source(10 $\mu A$ ) if it's more than Vo1- 0.2V. The equation of delay time is same as below.  $Trd = (Cd \times 2.5) / 10\mu A$
- These parameters, although guaranteed, are not 100% tested in production.

# Mechanical Dimensions

Package

Dimensions in millimeters

## 10-SIP-H/S



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## Ordering Information

| Product Number | Package    | Operating Temperature |
|----------------|------------|-----------------------|
| KA7630         | 10-SIP-H/S | 0°C to +125°C         |
| KA7631         |            |                       |

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