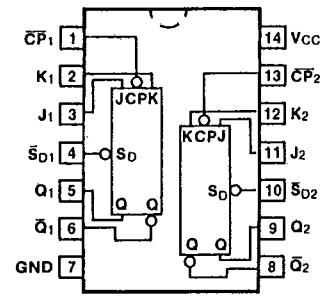


T-46-07-07 113

54S/74S113 54LS/74LS113

DUAL JK EDGE-TRIGGERED FLIP-FLOP

CONNECTION DIAGRAM PINOUT A



DESCRIPTION — The '113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

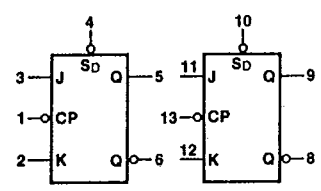
TRUTH TABLE

| INPUTS | | OUTPUT |
|---------|-------------|-------------|
| @ t_n | @ t_{n+1} | |
| J | K | Q |
| L | L | Q_n |
| L | H | L |
| H | L | H |
| H | H | \bar{Q}_n |

Asynchronous Input:
LOW input to \bar{S}_D sets Q to HIGH level
Set is independent of clock

t_n = Bit time before clock pulse.
 t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

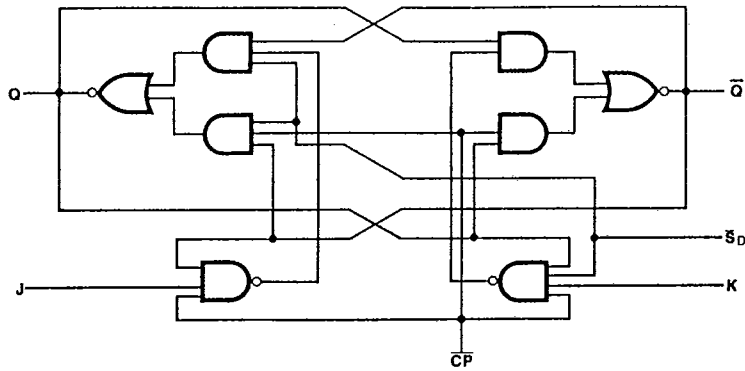
| PKGS | PIN OUT | COMMERCIAL GRADE | MILITARY GRADE | PKG TYPE |
|-----------------|---------|--|--|----------|
| | | VCC = +5.0 V ±5%, TA = 0°C to +70°C | VCC = +5.0 V ±10%, TA = -55°C to +125°C | |
| Plastic DIP (P) | A | 74S113PC, 74LS113PC | | 9A |
| Ceramic DIP (D) | A | 74S113DC, 74LS113DC | 54S113DM, 54LS113DM | 6A |
| Flatpak (F) | A | 74S113FC, 74LS113FC | 54S113FM, 54LS113FM | 3I |

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74S (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|--|--|------------------------|-------------------------|
| J ₁ , J ₂ , K ₁ , K ₂ | Data Inputs | 1.25/1.0 | 0.5/0.25 |
| CP ₁ , CP ₂ | Clock Pulse Inputs (Active Falling Edge) | 2.5/2.5 | 2.0/0.5 |
| SD ₁ , SD ₂ | Direct Set Inputs (Active LOW) | 2.5/4.375 | 1.5/0.5 |
| Q ₁ , Q ₂ , Q ₁ -bar, Q ₂ -bar | Outputs | 25/12.5 | 10/5.0 (2.5) |

4

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| SYMBOL | PARAMETER | 54/74S | | 54/74LS | | UNITS | CONDITIONS |
|-----------------|----------------------|--------|-----|---------|-----|-------|--|
| | | Min | Max | Min | Max | | |
| I _{CC} | Power Supply Current | 50 | | 8.0 | | mA | V _{CC} = Max, V _{CP} = 0 V |

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 54/74S | | 54/74LS | | UNITS | CONDITIONS |
|--------------------------------------|---|--|-----|------------------------|-----|-------|-----------------|
| | | C _L = 15 pF R _L = 280 Ω | | C _L = 15 pF | | | |
| | | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 80 | | 30 | | MHz | Figs. 3-1, 3-9 |
| t _{PLH} t _{PHL} | Propagation Delay CP _n to Q _n or Q _n -bar | 7.0 | | 16 | | ns | Figs. 3-1, 3-9 |
| | | 7.0 | | 24 | | | |
| t _{PLH} t _{PHL} | Propagation Delay S _{Dn} to Q _n or Q _n -bar | 7.0 | | 16 | | ns | Figs. 3-1, 3-10 |
| | | 7.0 | | 24 | | | |

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

| SYMBOL | PARAMETER | 54/74S | | 54/74LS | | UNITS | CONDITIONS |
|--|---|--------|-----|---------|-----|-------|------------|
| | | Min | Max | Min | Max | | |
| t _s (H) t _s (L) | Setup Time J _n or K _n to CP _n | 7.0 | | 20 | | ns | Fig. 3-7 |
| | | 7.0 | | 15 | | | |
| t _h (H) t _h (L) | Hold Time J _n or K _n to CP _n | 0 | | 0 | | ns | |
| | | 0 | | 0 | | | |
| t _w (H) t _w (L) | CP _n Pulse Width | 6.0 | | 20 | | ns | Fig. 3-9 |
| | | 6.5 | | 15 | | | |
| t _w (L) | S _{Dn} Pulse Width LOW | 8.0 | | 15 | | ns | Fig. 3-10 |