

# PCF8575C Remote 16-Bit I<sup>2</sup>C AND SMBus Low-Power I/O Expander with Interrupt Output

## 1 Features

- I<sup>2</sup>C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Low Standby-Current Consumption of 10  $\mu$ A Maximum
- Compatible With Most Microcontrollers
- 400-kHz Fast I<sup>2</sup>C Bus
- Address by Three Hardware Address Pins for Use of up to Eight Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

## 2 Applications

- Telecom Shelters: Filter Units
- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics
- Industrial Automation
- Products with GPIO-Limited Processors

## 3 Description

This 16-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 4.5-V to 5.5-V  $V_{CC}$  operation.

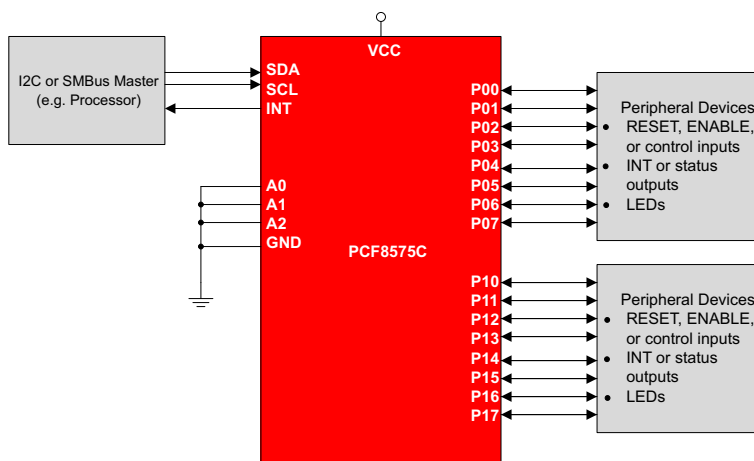
The PCF8575C provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface serial clock (SCL) and serial data (SDA).

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00, P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are in 3-state mode. The strong pullup to  $V_{CC}$  allows fast-rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs. After power on, as all the I/Os are set to 3-state, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode. If a high is applied externally to an I/O that has been written earlier to low, a large current ( $I_{OL}$ ) flows to GND.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE (PIN)	BODY SIZE
PCF8575C	SSOP (24)	8.20 mm × 5.30 mm
	QSOP (24)	8.65 mm × 3.90
	TVSOP (24)	5.00 mm × 4.50 mm
	SOIC (24)	15.40 mm × 7.50 mm
	TSSOP (24)	7.80 mm × 4.40 mm
	QFN (24)	4.0 mm × 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.2 Functional Block Diagram .....	<b>12</b>
<b>2 Applications</b> .....	<b>1</b>	8.3 Feature Description .....	<b>13</b>
<b>3 Description</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>15</b>
<b>4 Revision History</b> .....	<b>2</b>	<b>9 Application and Implementation</b> .....	<b>17</b>
<b>5 Pin Configuration</b> .....	<b>3</b>	9.1 Application Information .....	<b>17</b>
<b>6 Specifications</b> .....	<b>4</b>	9.2 Typical Application .....	<b>17</b>
6.1 Absolute Maximum Ratings .....	<b>4</b>	<b>10 Power Supply Recommendations</b> .....	<b>20</b>
6.2 ESD Ratings .....	<b>4</b>	10.1 Power-On Reset Requirements .....	<b>20</b>
6.3 Recommended Operating Conditions .....	<b>4</b>	<b>11 Layout</b> .....	<b>22</b>
6.4 Thermal Information .....	<b>4</b>	11.1 Layout Guidelines .....	<b>22</b>
6.5 Electrical Characteristics .....	<b>5</b>	11.2 Layout Example .....	<b>23</b>
6.6 I <sup>2</sup> C Interface Timing Requirements .....	<b>5</b>	<b>12 Device and Documentation Support</b> .....	<b>24</b>
6.7 Switching Characteristics .....	<b>6</b>	12.1 Trademarks .....	<b>24</b>
6.8 Typical Characteristics .....	<b>6</b>	12.2 Electrostatic Discharge Caution .....	<b>24</b>
<b>7 Parameter Measurement Information</b> .....	<b>8</b>	12.3 Glossary .....	<b>24</b>
<b>8 Detailed Description</b> .....	<b>11</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>24</b>
8.1 Overview .....	<b>11</b>		

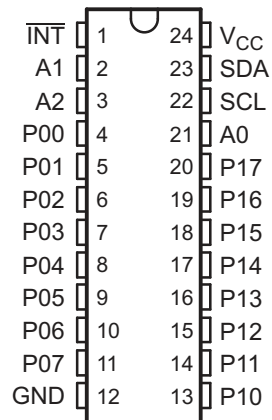
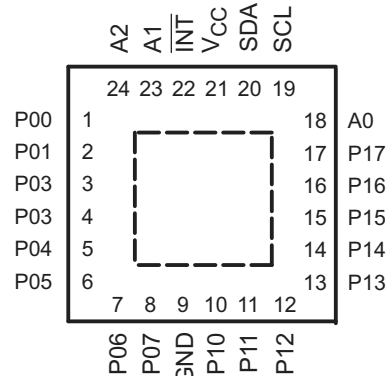
## 4 Revision History

### Changes from Revision E (October 2007) to Revision F

**Page**

- |  |                      |
|--|----------------------|
| <ul style="list-style-type: none"> <li>Added <i>Applications</i>, <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i>, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....</li> <li>Deleted <i>Ordering Information</i> table. ....</li> </ul> | <b>1</b><br><b>1</b> |
|--|----------------------|

## 5 Pin Configuration

**DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)**

**RGE PACKAGE  
(TOP VIEW)**


### Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	NO.			
	DB, DBQ, DGV, DW, AND PW	RGE		
INT	1	22	I	Interrupt output. Connect to $V_{CC}$ through a pullup resistor.
A1	2	23	I	Address input 1. Connect directly to $V_{CC}$ or ground. Pullup resistors are not needed.
A2	3	24	I	Address input 2. Connect directly to $V_{CC}$ or ground. Pullup resistors are not needed.
P00	4	1	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P01	5	2	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P02	6	3	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P03	7	4	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P04	8	5	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P05	9	6	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P06	10	7	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P07	11	8	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
GND	12	9	—	Ground
P10	13	10	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P11	14	11	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P12	15	12	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P13	16	13	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P14	17	14	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P15	18	15	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P16	19	16	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
P17	20	17	I/O	P-port input/output. Open-drain design structure. Connect to $V_{CC}$ through a pullup resistor.
A0	21	18	I	Address input 0. Connect directly to $V_{CC}$ or ground. Pullup resistors are not needed.
SCL	22	19	I	Serial clock line. Connect to $V_{CC}$ through a pullup resistor
SDA	23	20	I/O	Serial data line. Connect to $V_{CC}$ through a pullup resistor.
$V_{CC}$	24	21	—	Supply voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-20 mA
I <sub>OK</sub>	Input/output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±400 µA
I <sub>OL</sub>	Continuous output low current	V <sub>O</sub> = 0 to V <sub>CC</sub>		50 mA
I <sub>OH</sub>	Continuous output high current	V <sub>O</sub> = 0 to V <sub>CC</sub>		-4 mA
Continuous current through V <sub>CC</sub> or GND				±100 mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	1000

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	4.5	5.5	V	
V <sub>IH</sub>	High-level input voltage	A0, A1, A2, SDA, and SCL	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V
		P07–P00 and P17–P10	0.8 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5	
V <sub>IL</sub>	Low-level input voltage	A0, A1, A2, SDA, and SCL	-0.5	0.3 × V <sub>CC</sub>	V
		P07–P00 and P17–P10	-0.5	0.6 × V <sub>CC</sub>	
I <sub>OHT</sub>	P-port transient pullup current			-10 mA	
I <sub>OL</sub>	P-port low-level output current			25 mA	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		PCF8575						UNIT
		DB	DBQ	DGV	DW	PW	RGE	
		24 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	63	61	86	46	88	53	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	4.5 V to 5.5 V	-1.2			V
V <sub>POR</sub>	Power-on reset voltage <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	V <sub>POR</sub>		1.2	1.8	V
I <sub>OHT</sub>	P-port transient pullup current	High during ACK V <sub>OH</sub> = GND	4.5 V	-0.5	-1		mA
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V	4.5 V to 5.5 V	3			mA
	P port	V <sub>OL</sub> = 0.4 V	4.5 V to 5.5 V	5	15		
		V <sub>OL</sub> = 1 V		10	25		
	$\overline{\text{INT}}$	V <sub>OL</sub> = 0.4 V	4.5 V to 5.5 V	1.6			
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	4.5 V to 5.5 V			±2	µA
	A0, A1, A2					±1	
I <sub>IHL</sub>	P port	V <sub>I</sub> ≥ V <sub>CC</sub> or V <sub>I</sub> ≤ GND	4.5 V to 5.5 V			±400	µA
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 400 kHz	5.5 V		100	200	µA
	Standby mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 0 kHz			2.5	10	
ΔI <sub>CC</sub>	Supply current increase	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	4.5 V to 5.5 V			200	µA
C <sub>i</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	4.5 V to 5.5 V		3	7	pF
C <sub>io</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	4.5 V to 5.5 V		3	7	pF
	P port				4	10	

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) The power-on reset circuit resets the I<sup>2</sup>C bus logic with V<sub>CC</sub> < V<sub>POR</sub> and sets all I/Os to logic high (with current source to V<sub>CC</sub>).

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7)

		MIN	MAX	UNIT
f <sub>scl</sub>	I <sup>2</sup> C clock frequency		400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	0.6		µs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	1.3		µs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time	20 + 0.1C <sub>b</sub> <sup>(1)</sup>	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time	20 + 0.1C <sub>b</sub> <sup>(1)</sup>	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time (10-pF to 400-pF bus)		300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start	1.3		µs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	0.6		µs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	0.6		µs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup	0.6		µs
t <sub>vd</sub>	Valid-data time	SCL low to SDA output valid		1.2
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF

(1) C<sub>b</sub> = total bus capacitance of one bus line in pF

### 6.7 Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see Figure 8 and Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{iv}$	Interrupt valid time	P port		4	$\mu$ s
$t_{ir}$	Interrupt reset delay time	SCL		4	$\mu$ s
$t_{pv}$	Output data valid	SCL		4	$\mu$ s
$t_{su}$	Input data setup time	P port	0		$\mu$ s
$t_h$	Input data hold time	P port	4		$\mu$ s

### 6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

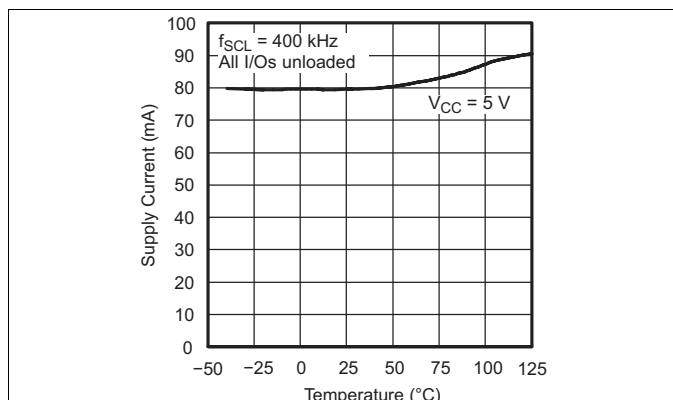


Figure 1. Supply Current vs Temperature

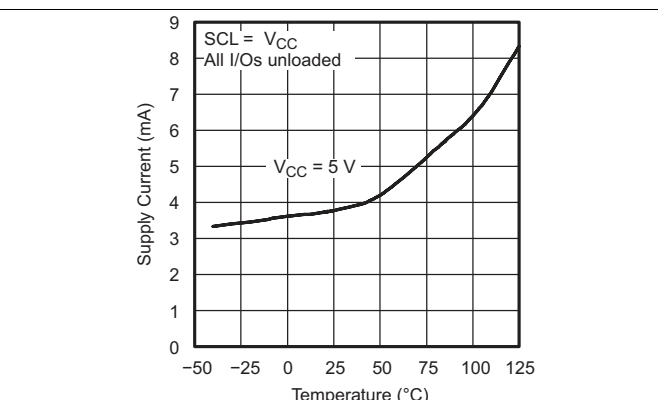


Figure 2. Standby Supply Current vs Temperature

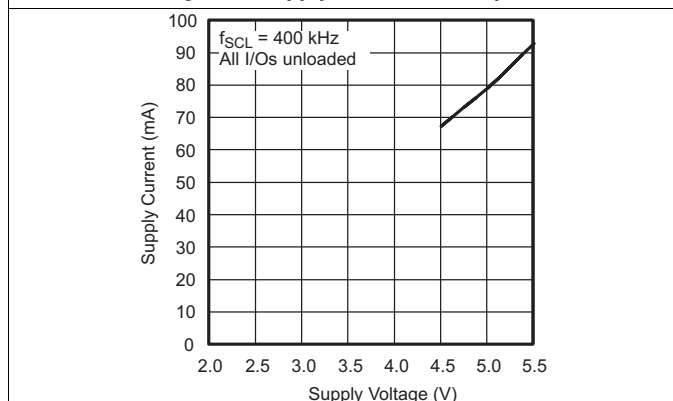


Figure 3. Supply Current vs Supply Voltage

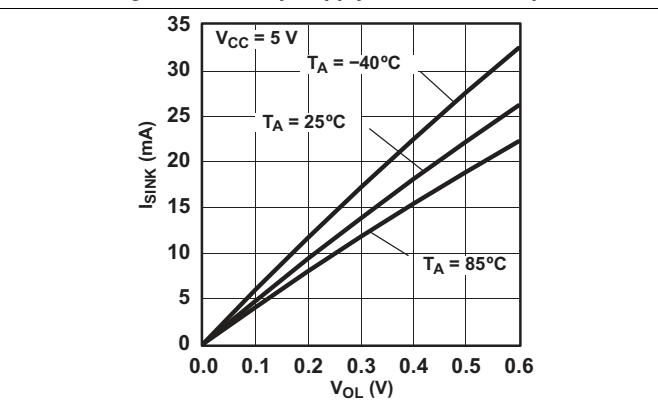
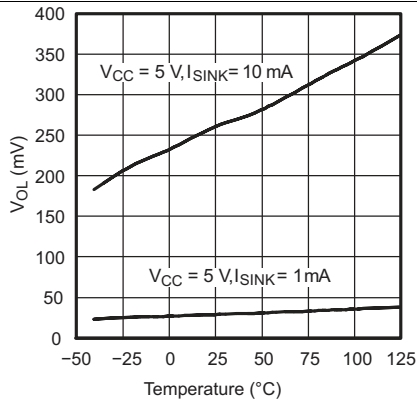


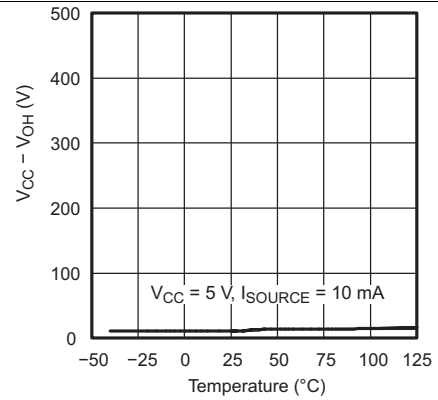
Figure 4. I/O Sink Current vs Output Low Voltage

**Typical Characteristics (continued)**

T<sub>A</sub> = 25°C (unless otherwise noted)

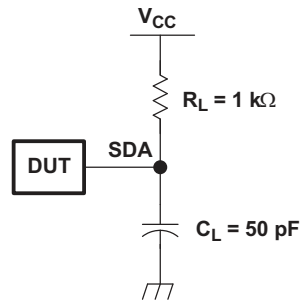


**Figure 5. I/O Output Low Voltage vs Temperature**

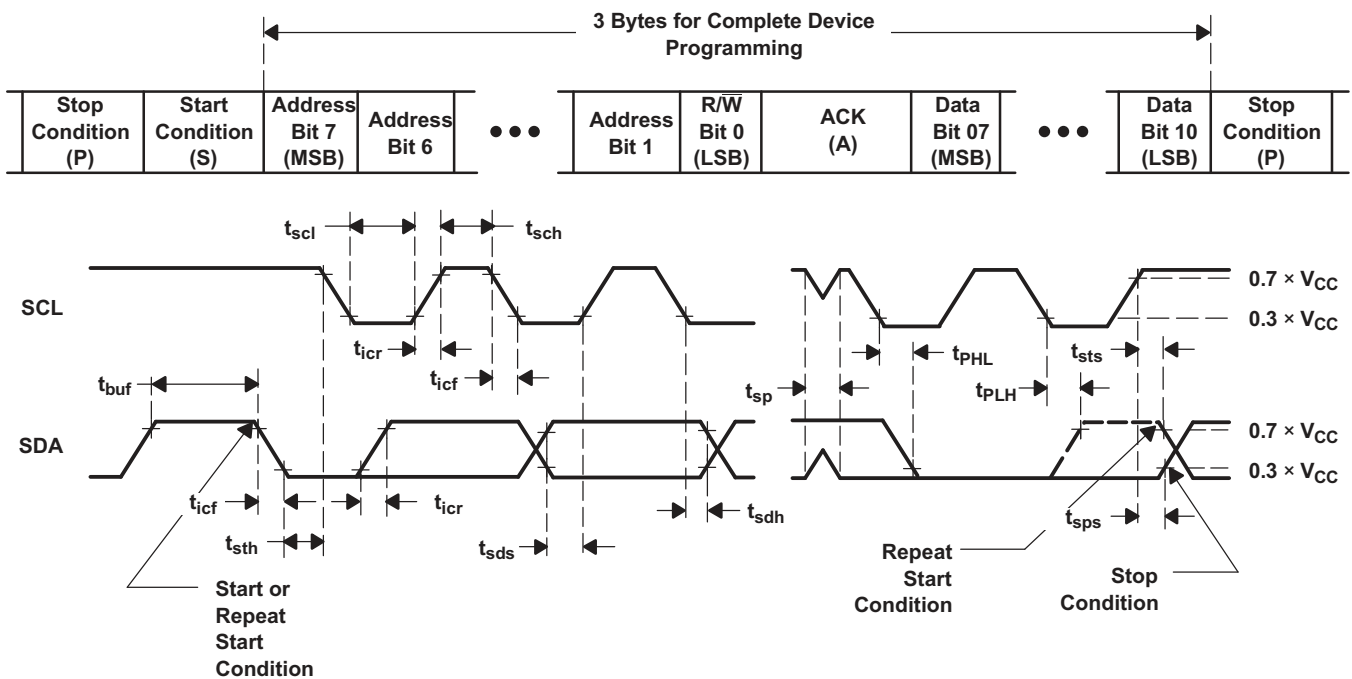


**Figure 6. I/O High Voltage vs Temperature**

## 7 Parameter Measurement Information



SDA LOAD CONFIGURATION



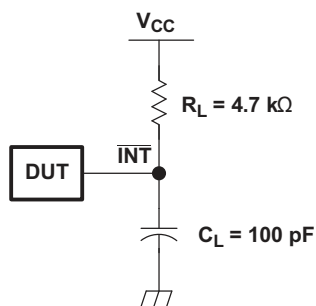
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

Figure 7. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms



Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION

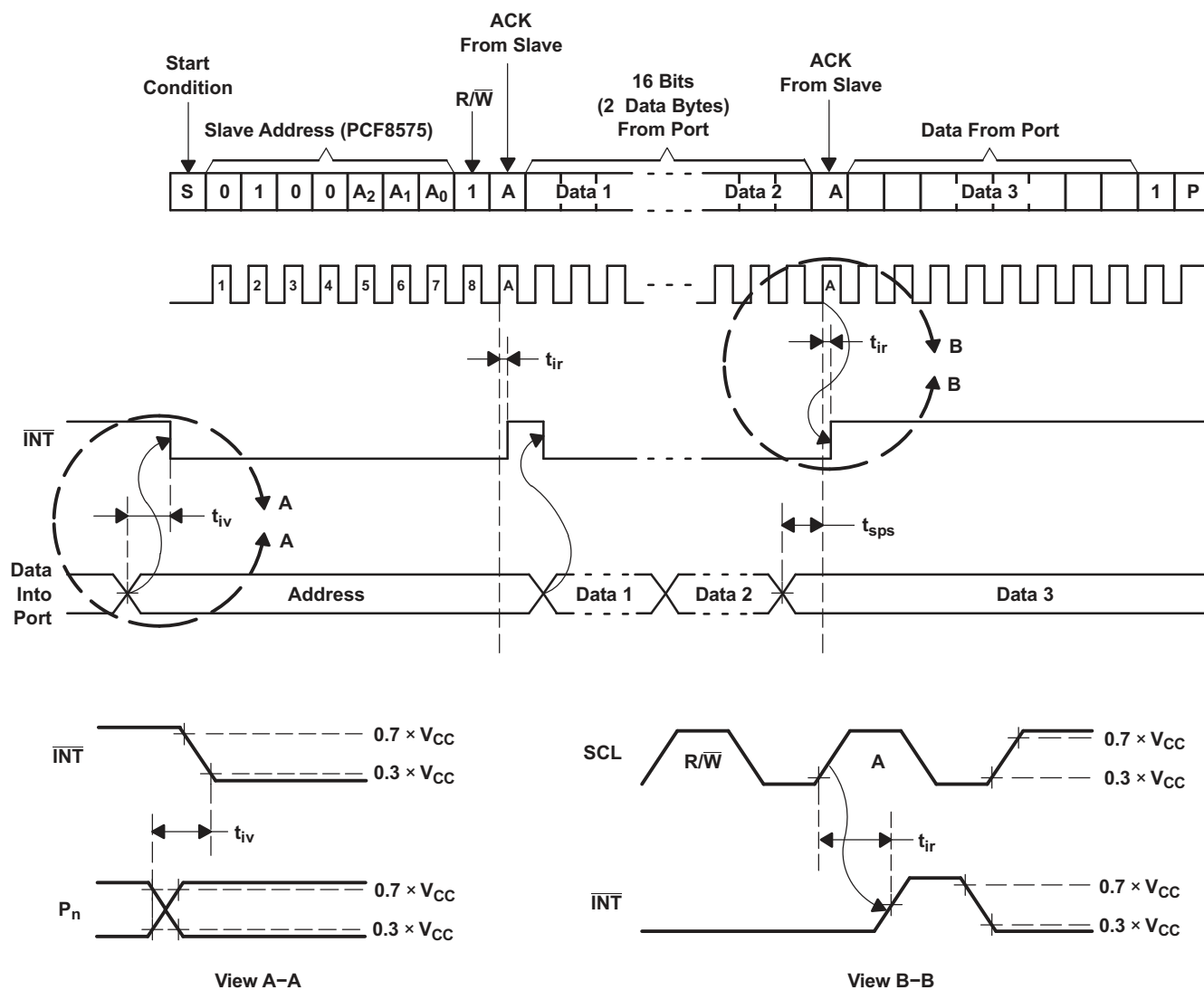
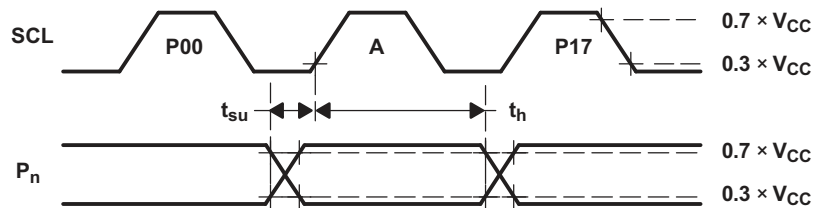
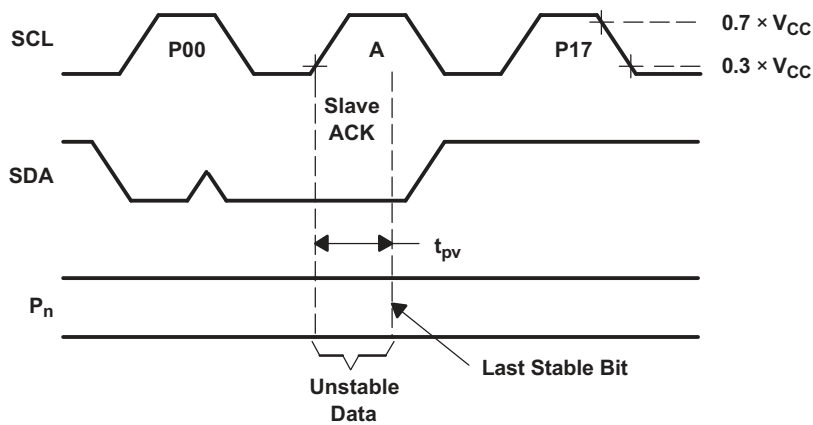
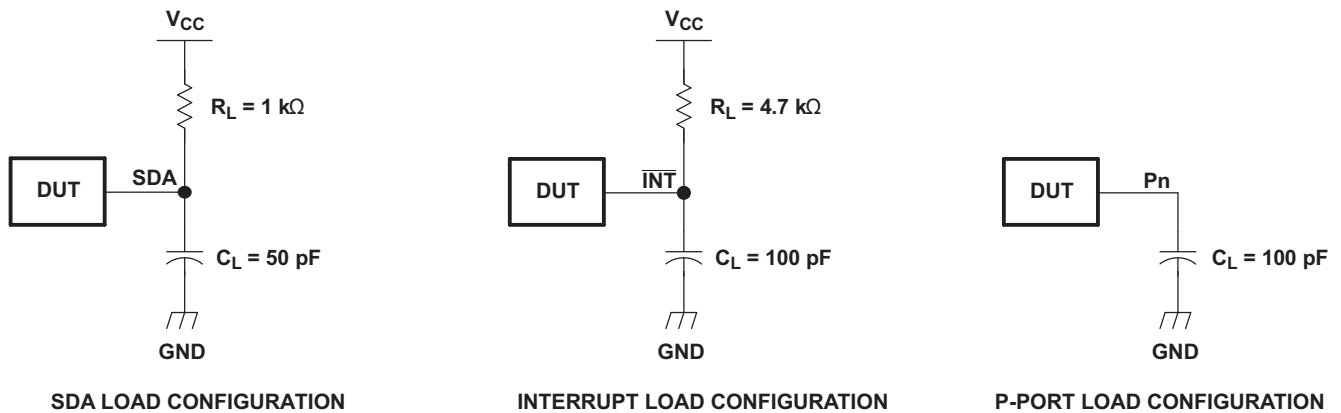


Figure 8. Interrupt Load Circuit and Voltage Waveforms

**Parameter Measurement Information (continued)**

**Figure 9. P-Port Load Circuits and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The PCF8575C provides an open-drain interrupt ( $\overline{\text{INT}}$ ) output, which can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time ( $t_{iv}$ ), the signal  $\overline{\text{INT}}$  is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting, or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal or in the write mode at the ACK bit after the falling edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short), due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{\text{INT}}$ . Reading from or writing to another device does not affect the interrupt circuit.

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports, without having to communicate via the I<sup>2</sup>C bus. Thus, the PCF8575C can remain a simple slave device.

Every data transmission to or from the PCF8575C must consist of an even number of bytes. The first data byte in every pair refers to port 0 (P07–P00), and the second data byte in every pair refers to port 1 (P17–P10). To write to the ports (output mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 0. The PCF8575C acknowledges and the master sends the first data byte for P07–P00. After the first data byte is acknowledged by the PCF8575C, the second data byte (P17–P10) is sent by the master. Once again, the PCF8575C acknowledges the receipt of the data, after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten. When the PCF8575C receives the pairs of data bytes, the first byte is referred to as P07–P00 and the second byte as P17–P10. The third byte is referred to as P07–P00, the fourth byte as P17–P10, and so on.

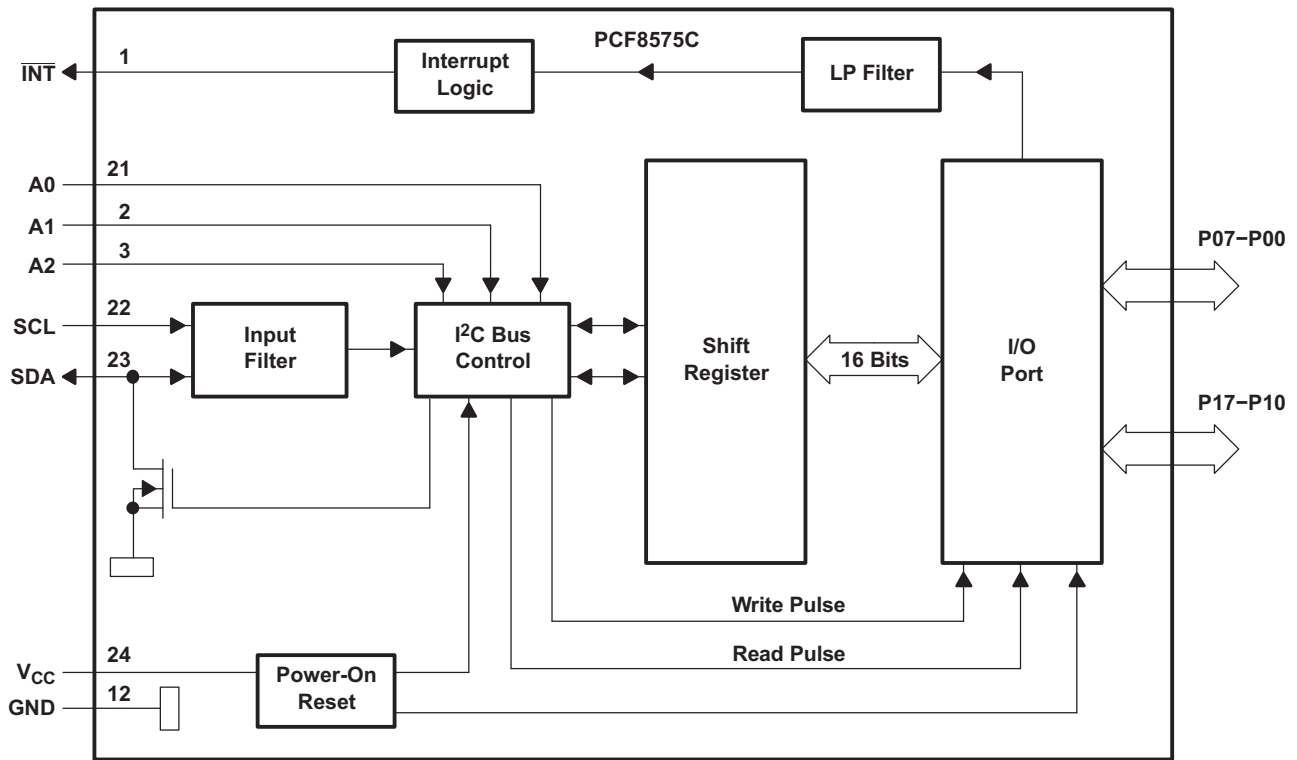
Before reading from the PCF8575C, all ports desired as input should be set to logic 1. To read from the ports (input mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 1. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the master can read, this data may be lost.

When power is applied to  $V_{CC}$ , an internal power-on reset holds the PCF8575C in a reset state until  $V_{CC}$  has reached  $V_{POR}$ . At that time, the reset condition is released, and the device I<sup>2</sup>C-bus state machine initializes the bus to its default state.

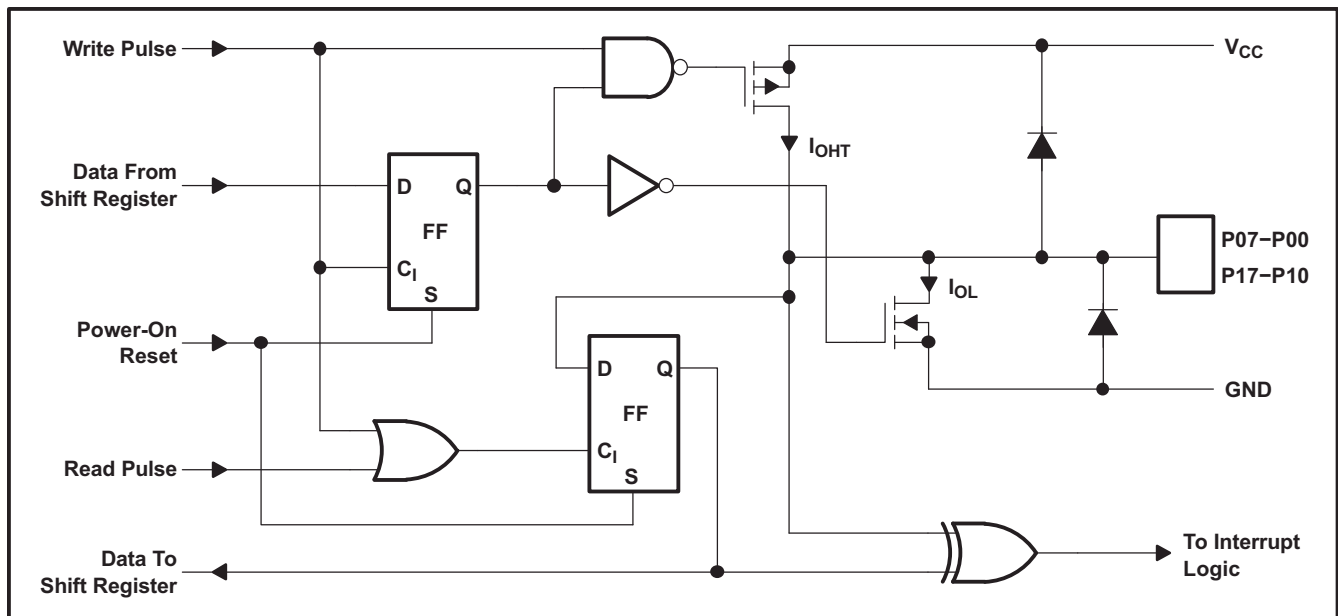
The hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C address, and allow up to eight devices to share the same I<sup>2</sup>C bus or SMBus. The fixed I<sup>2</sup>C address of the PCF8575C is the same as the PCF8575, PCF8574, PCA9535, and PCA9555, allowing up to eight of these devices, in any combination, to share the same I<sup>2</sup>C bus or SMBus.

## 8.2 Functional Block Diagram

### 8.2.1 Simplified Block Diagram of Device



### 8.2.2 Simplified Schematic Diagram of Each P-Port Input/Output



## 8.3 Feature Description

### 8.3.1 I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 10). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A2–A0) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address ACK. If the  $\overline{R/W}$  bit is high, the data from this device are the values read from the P port. If the R/W bit is low, the data are from the master, to be output to the P port. The data byte is followed by an ACK sent from this device. If other data bytes are sent from the master, following the ACK, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time ( $t_{pv}$ ) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 11).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 10).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 12). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

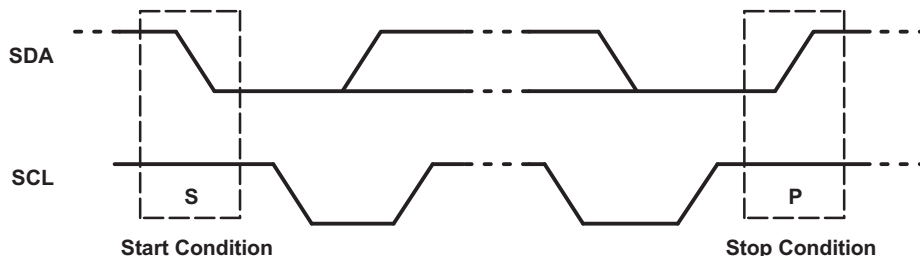
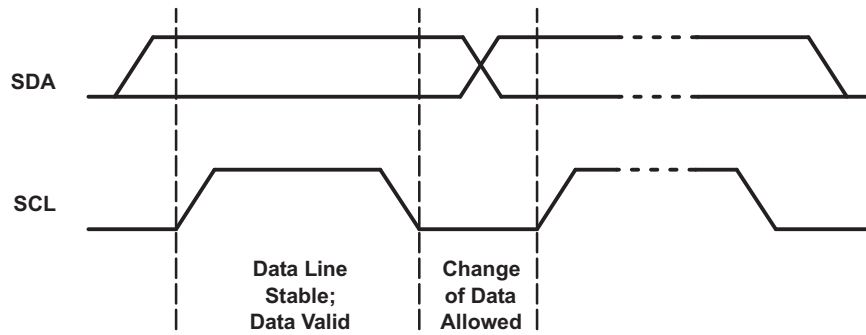
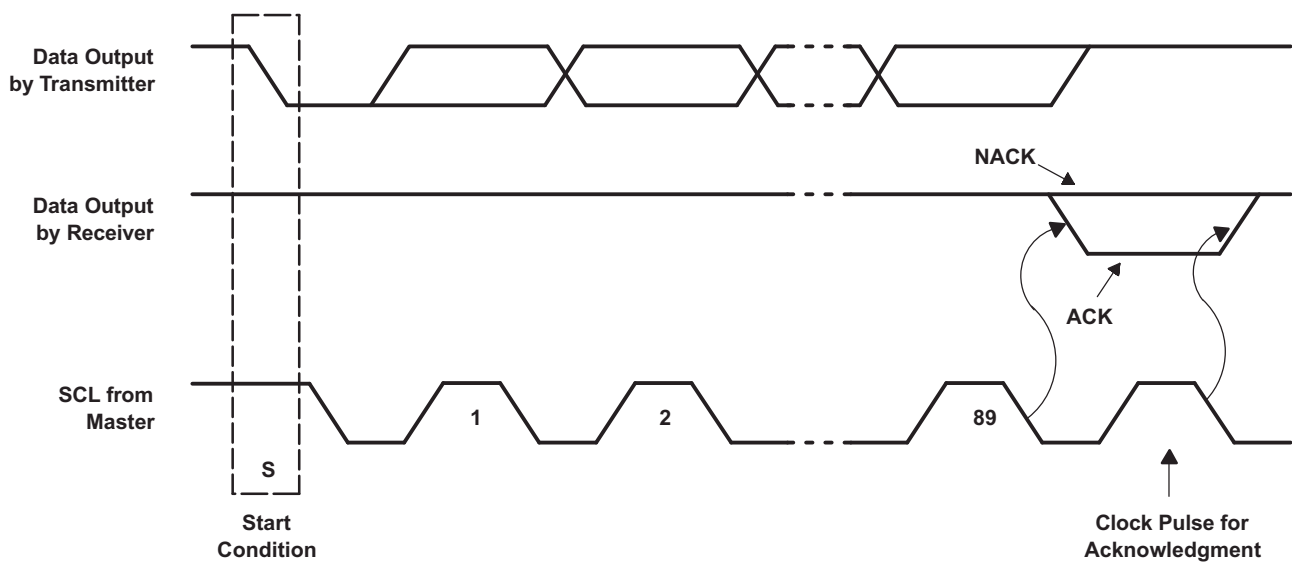


Figure 10. Definition of Start and Stop Conditions

**Feature Description (continued)**

**Figure 11. Bit Transfer**

**Figure 12. Acknowledgment on I<sup>2</sup>C Bus**
**8.3.2 Interface Definition**

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	L	H	L	L	A2	A1	A0	R/W
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

### 8.3.3 Address Reference

INPUTS			I <sup>2</sup> C BUS SLAVE 8-BIT READ ADDRESS	I <sup>2</sup> C BUS SLAVE 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	65 (decimal), 41 (hexadecimal)	64 (decimal), 40 (hexadecimal)
L	L	H	67 (decimal), 43 (hexadecimal)	66 (decimal), 42 (hexadecimal)
L	H	L	69 (decimal), 45 (hexadecimal)	68 (decimal), 44 (hexadecimal)
L	H	H	71 (decimal), 47 (hexadecimal)	70 (decimal), 46 (hexadecimal)
H	L	L	73 (decimal), 49 (hexadecimal)	72 (decimal), 48 (hexadecimal)
H	L	H	75 (decimal), 4B (hexadecimal)	74 (decimal), 4A (hexadecimal)
H	H	L	77 (decimal), 4D (hexadecimal)	76 (decimal), 4C (hexadecimal)
H	H	H	79 (decimal), 4F (hexadecimal)	78 (decimal), 4E (hexadecimal)

### 8.4 Device Functional Modes

Figure 13 and Figure 14 show the address and timing diagrams for the write and read modes, respectively.

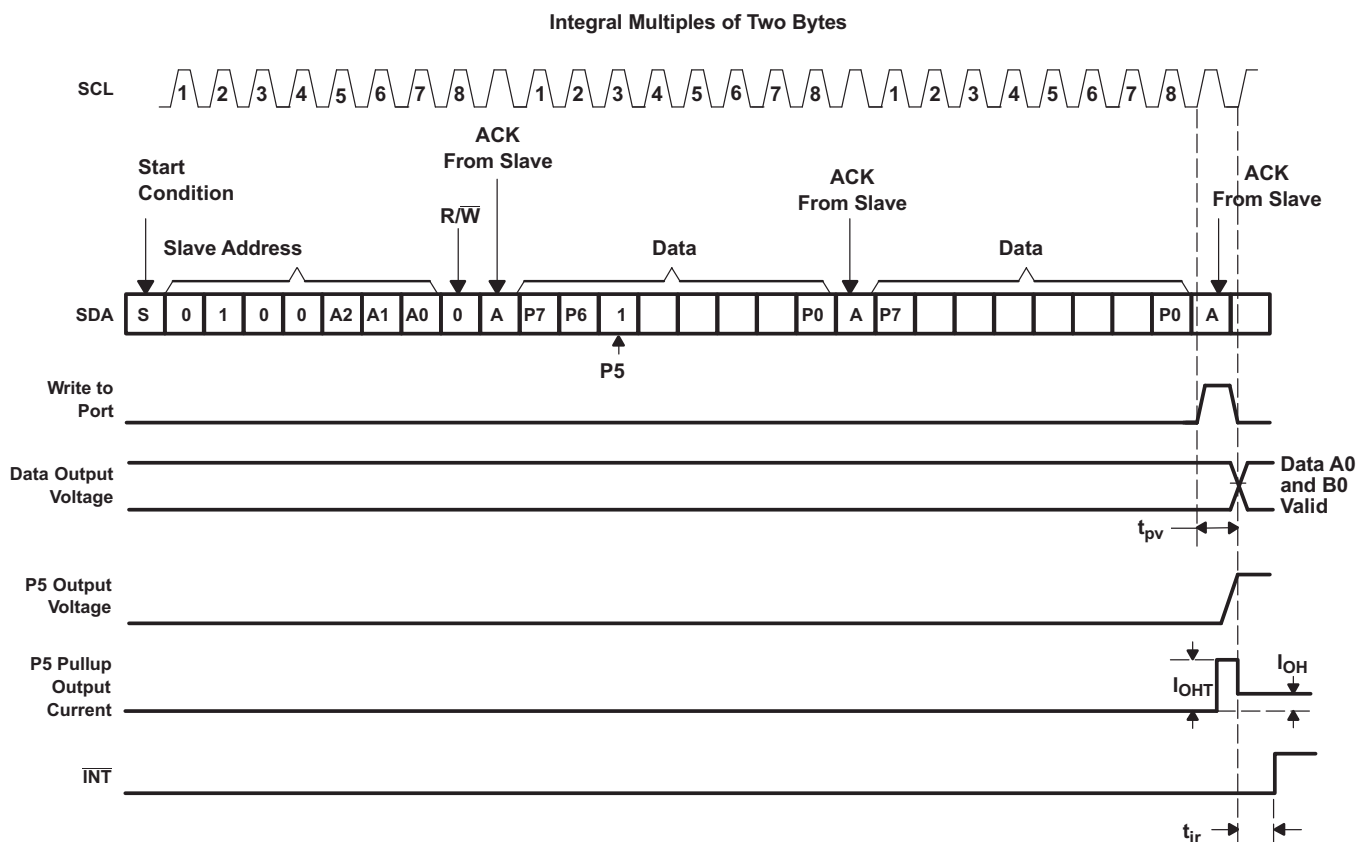
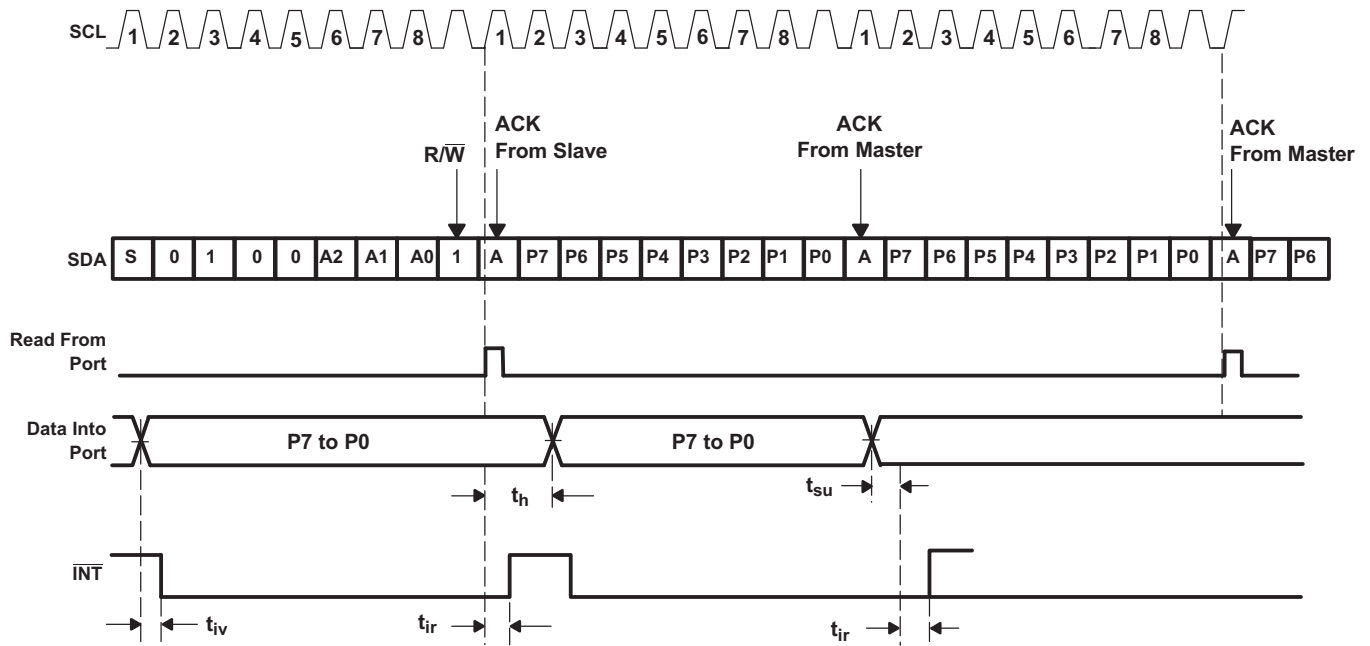


Figure 13. Write Mode (Output)

**Device Functional Modes (continued)**



**Figure 14. Read Mode (Input)**



## 9 Application and Implementation

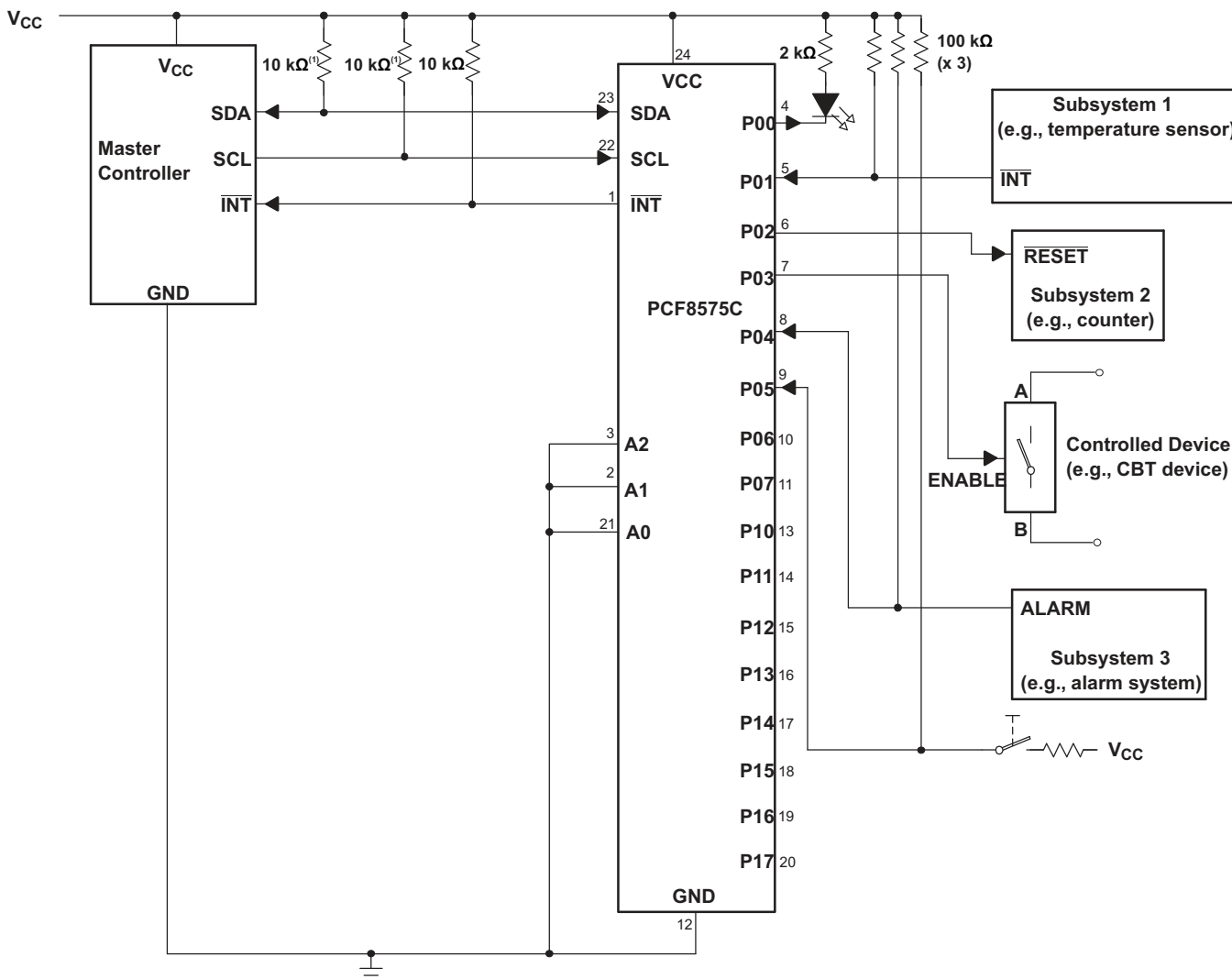
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Figure 15 shows an application in which the PCF8575C can be used.

### 9.2 Typical Application



(1) The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, will increase as a result.

- A. Device address is configured as 0100000 for this example.
- B. P0, P2, and P3 are configured as outputs.
- C. P1, P4, and P5 are configured as inputs.
- D. P6 and P7 are not used and must be configured as outputs.

Figure 15. Application Schematic

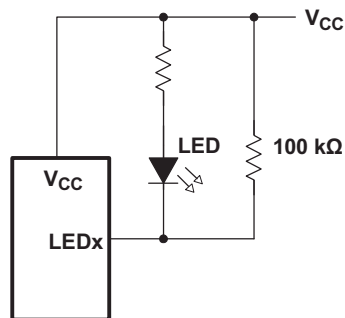
## Typical Application (continued)

### 9.2.1 Design Requirements

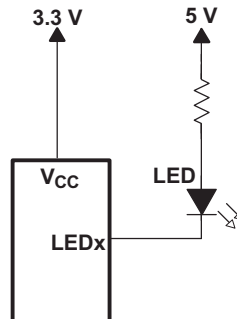
#### 9.2.1.1 Minimizing $I_{CC}$ When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to  $V_{CC}$  through a resistor as shown in Figure 15. For a P-port configured as an input,  $I_{CC}$  increases as  $V_I$  becomes lower than  $V_{CC}$ . The LED is a diode, with threshold voltage  $V_T$ , and when a P-port is configured as an input the LED will be off but  $V_I$  is a  $V_T$  drop below  $V_{CC}$ .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to  $V_{CC}$  when the P-ports are configured as input to minimize current consumption. Figure 16 shows a high-value resistor in parallel with the LED. Figure 17 shows  $V_{CC}$  less than the LED supply voltage by at least  $V_T$ . Both of these methods maintain the I/O  $V_I$  at or above  $V_{CC}$  and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.



**Figure 16. High-Value Resistor in Parallel With LED**



**Figure 17. Device Supplied by a Lower Voltage**

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

The pull-up resistors,  $R_p$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$ :

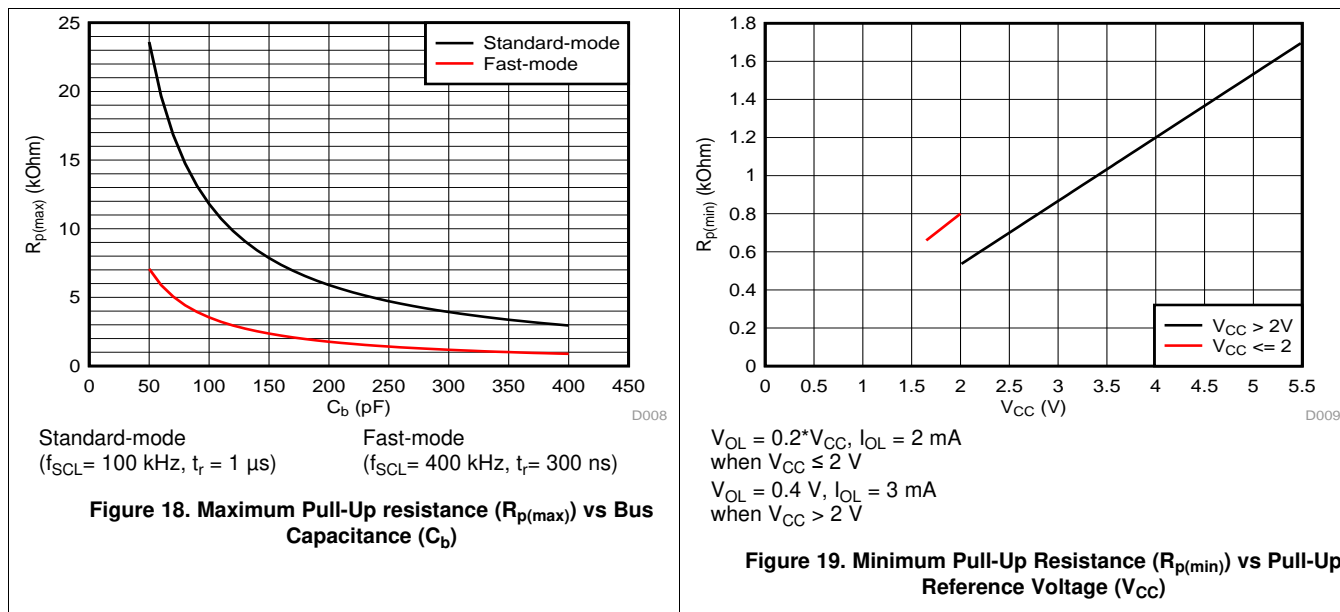
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \tag{1}$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$ :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{2}$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9534,  $C_i$  for SCL or  $C_{io}$  for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

### 9.2.3 Application Curves

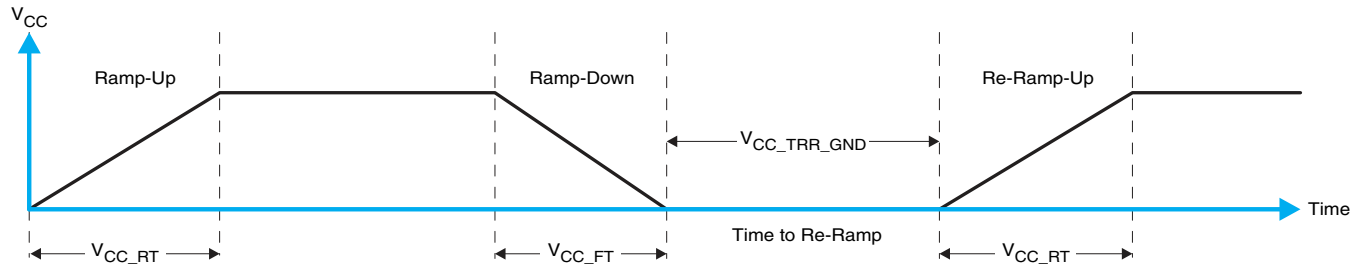


## 10 Power Supply Recommendations

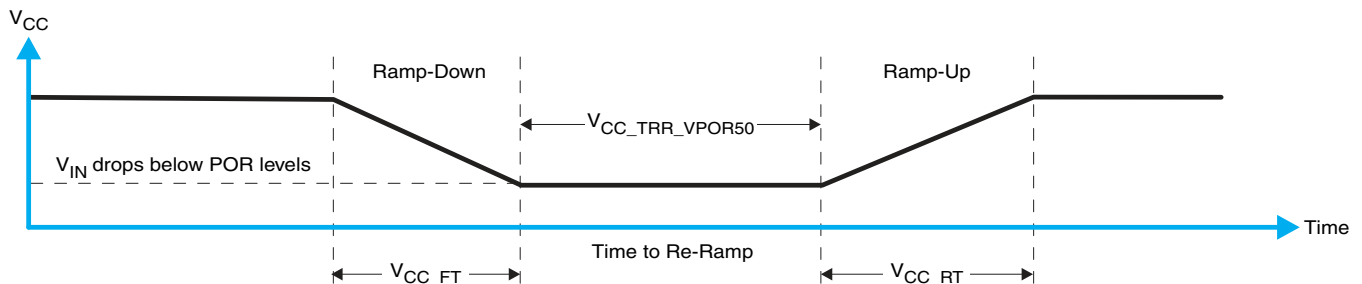
### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCF8575C can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 20](#) and [Figure 21](#).



**Figure 20.  $V_{CC}$  is Lowered Below 0.2 V or 0 V and Then Ramped Up to  $V_{CC}$**



**Figure 21.  $V_{CC}$  is Lowered Below the POR Threshold, Then Ramped Back Up to  $V_{CC}$**

[Table 1](#) specifies the performance of the power-on reset feature for PCF8575C for both types of power-on reset.

**Table 1. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES<sup>(1)</sup>**

PARAMETER			MIN	TYP	MAX	UNIT
$V_{CC\_FT}$	Fall rate	See <a href="#">Figure 20</a>	1		100	ms
$V_{CC\_RT}$	Rise rate	See <a href="#">Figure 20</a>	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when $V_{CC}$ drops to GND)	See <a href="#">Figure 20</a>	0.001			ms
$V_{CC\_TRR\_VPOR50}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV)	See <a href="#">Figure 21</a>	0.001			ms
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ $\mu$ s	See <a href="#">Figure 22</a>			1.2	V
$V_{CC\_GW}$	Glitch width that will not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCx}$	See <a href="#">Figure 22</a>				$\mu$ s
$V_{PORF}$	Voltage trip point of POR on falling $V_{CC}$		0.767		1.144	V
$V_{PORR}$	Voltage trip point of POR on rising $V_{CC}$		1.033		1.428	V

(1)  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 22 and Table 1 provide more information on how to measure these specifications.

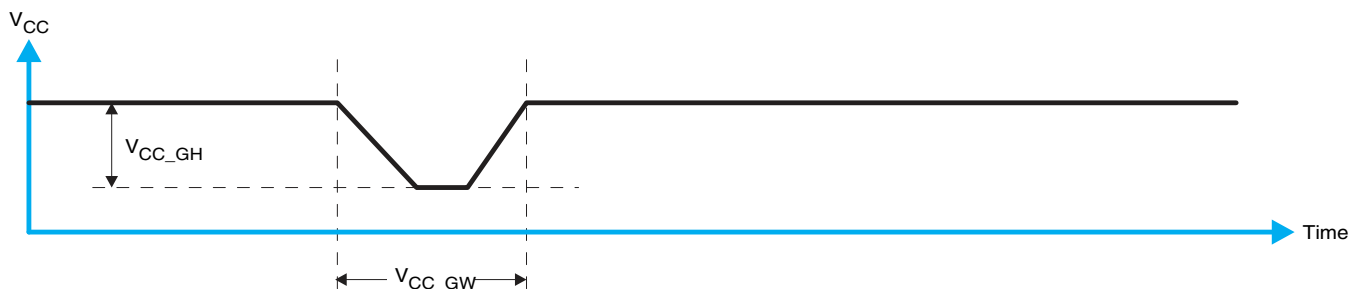


Figure 22. Glitch Width and Glitch Height

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 23 and Table 1 provide more details on this specification.

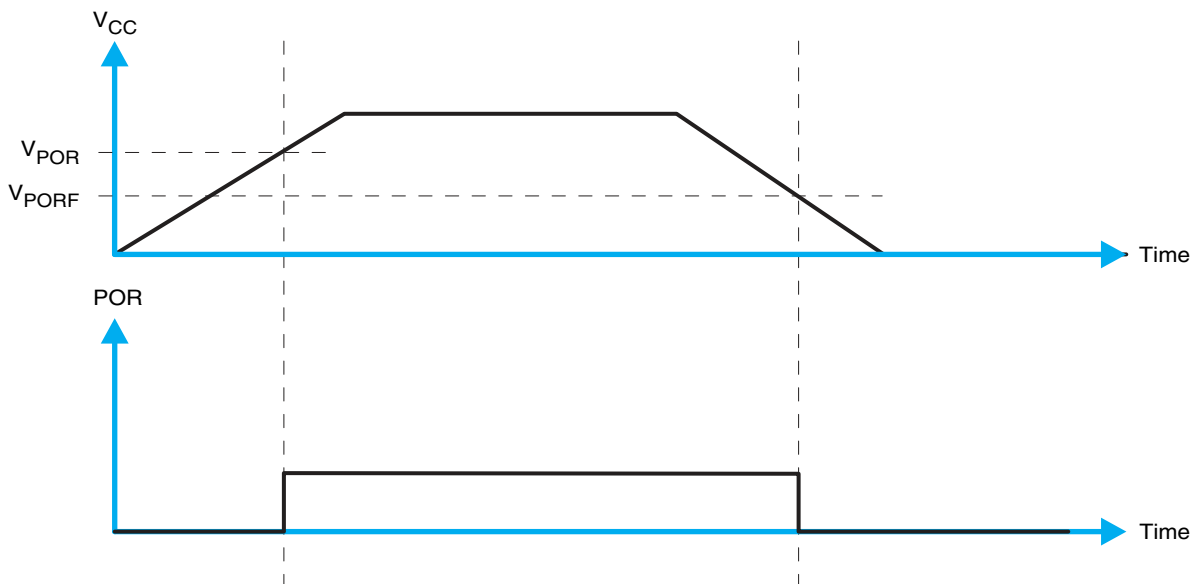


Figure 23.  $V_{POR}$

## 11 Layout

### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCF8575C device, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V<sub>CC</sub> pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8575C as possible. These best practices are shown in [Figure 24](#).

For the layout example provided in [Figure 24](#), it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V<sub>CC</sub>) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V<sub>CC</sub> or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in [Figure 24](#).

## 11.2 Layout Example

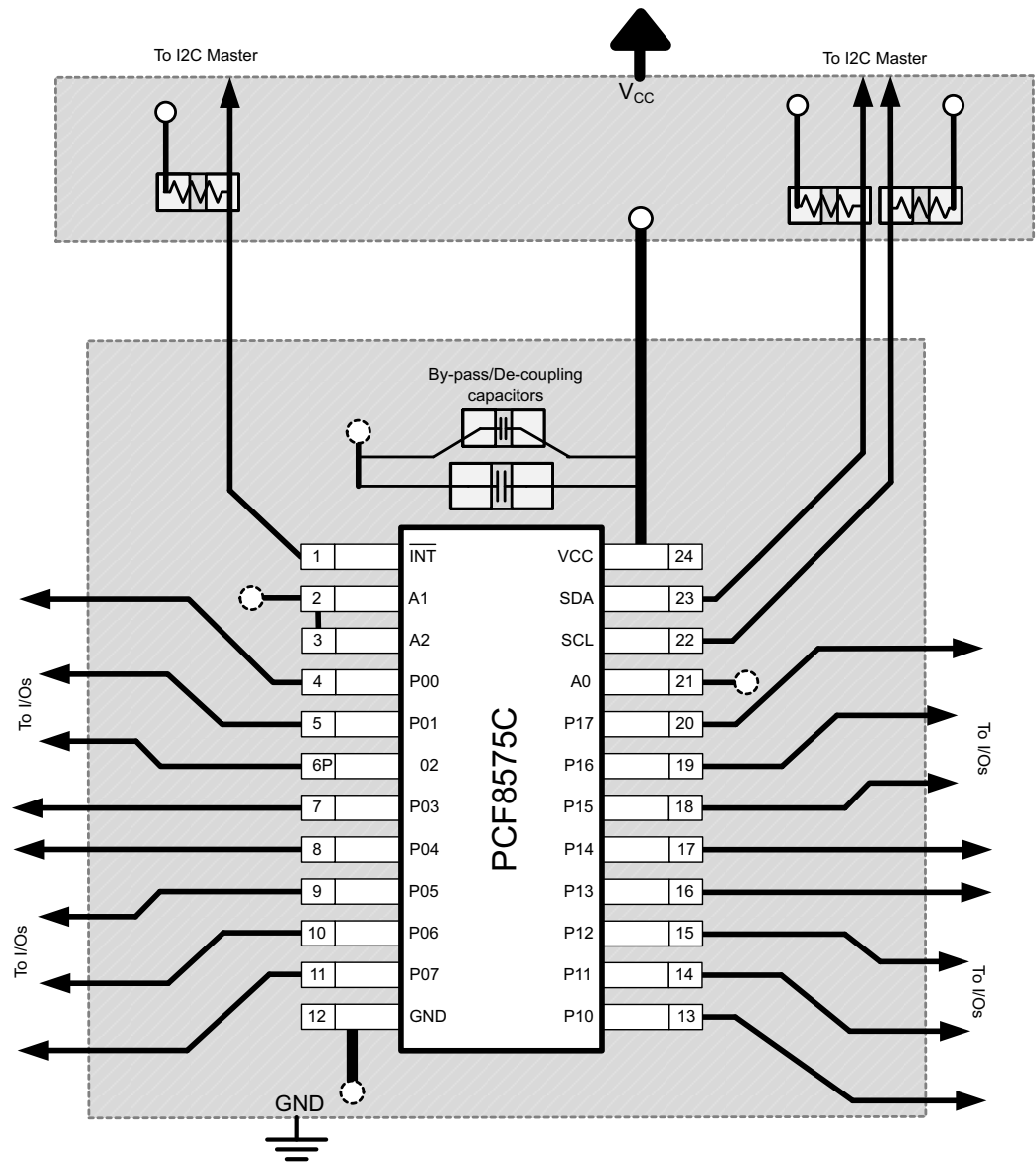
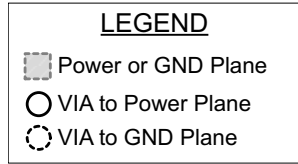


Figure 24. Layout Example for PCF8575C

## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8575CDB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	<a href="#">Samples</a>
PCF8575CDBE4	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	<a href="#">Samples</a>
PCF8575CDBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCF8575C	<a href="#">Samples</a>
PCF8575CDBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	<a href="#">Samples</a>
PCF8575CDGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	<a href="#">Samples</a>
PCF8575CDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575C	<a href="#">Samples</a>
PCF8575CDWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575C	<a href="#">Samples</a>
PCF8575CDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575C	<a href="#">Samples</a>
PCF8575CDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575C	<a href="#">Samples</a>
PCF8575CPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	<a href="#">Samples</a>
PCF8575CPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	<a href="#">Samples</a>
PCF8575CRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF575C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8575CDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCF8575CDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCF8575CDGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8575CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCF8575CPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCF8575CRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

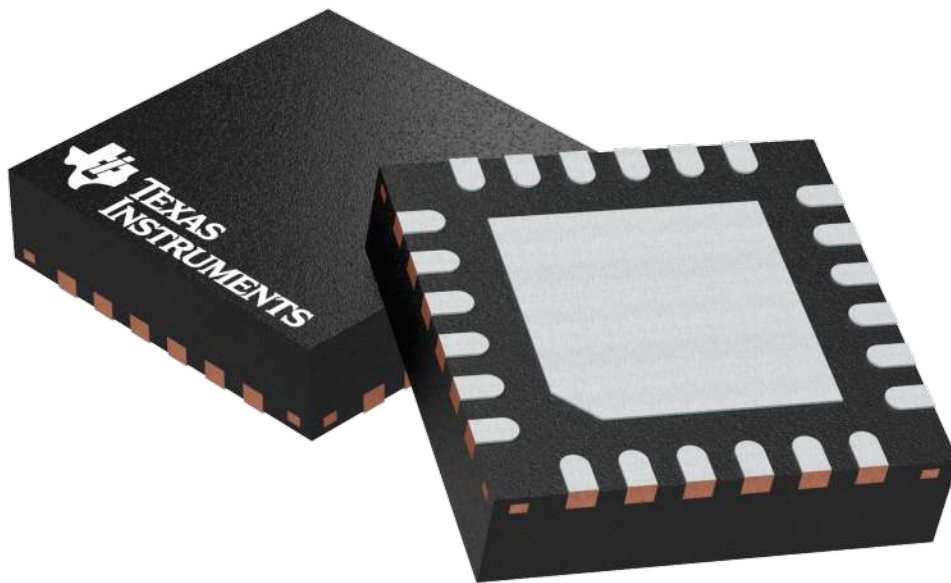
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8575CDBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
PCF8575CDBR	SSOP	DB	24	2000	367.0	367.0	38.0
PCF8575CDGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
PCF8575CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
PCF8575CPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
PCF8575CRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

**RGE 24**

**GENERIC PACKAGE VIEW**

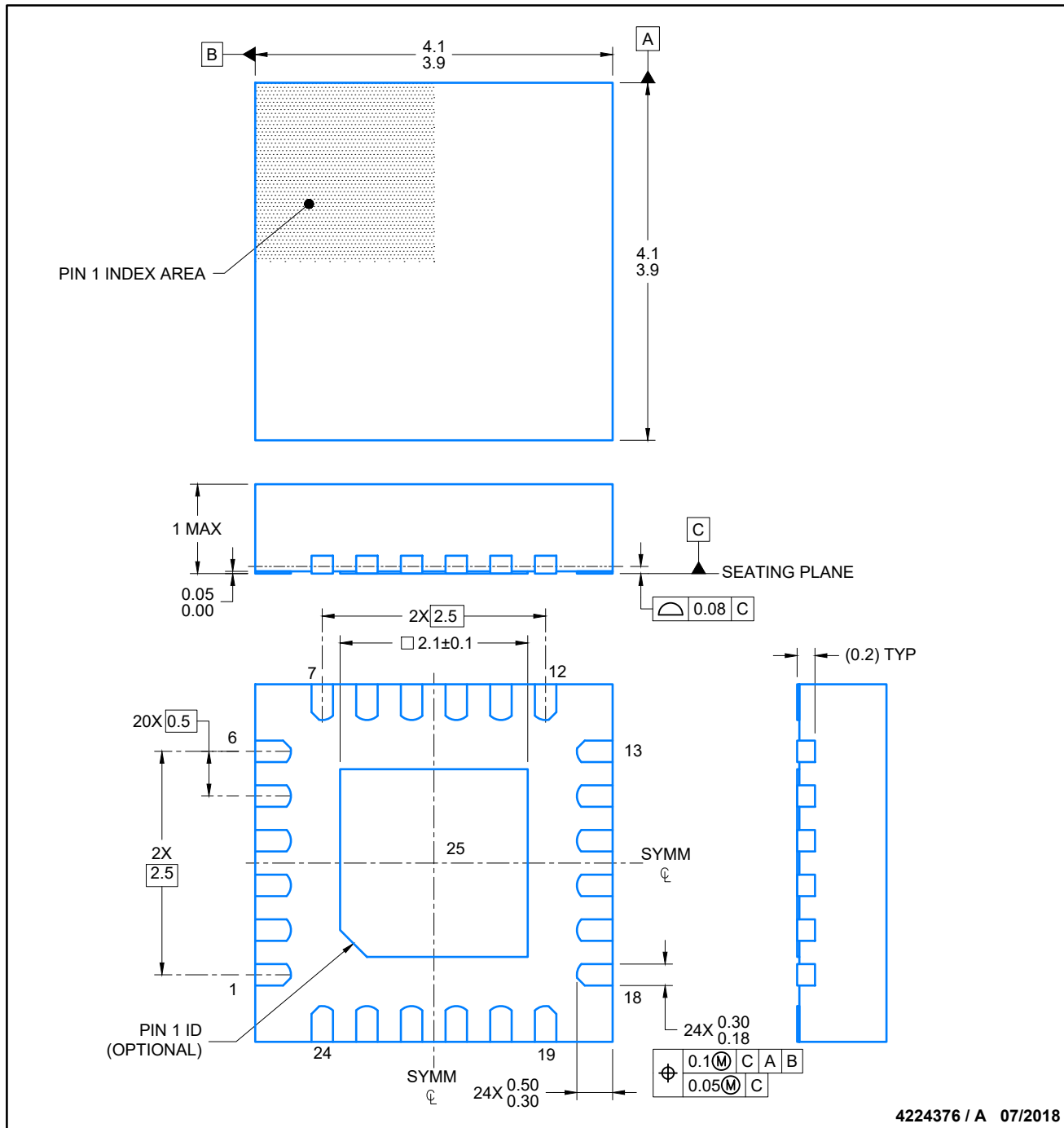
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



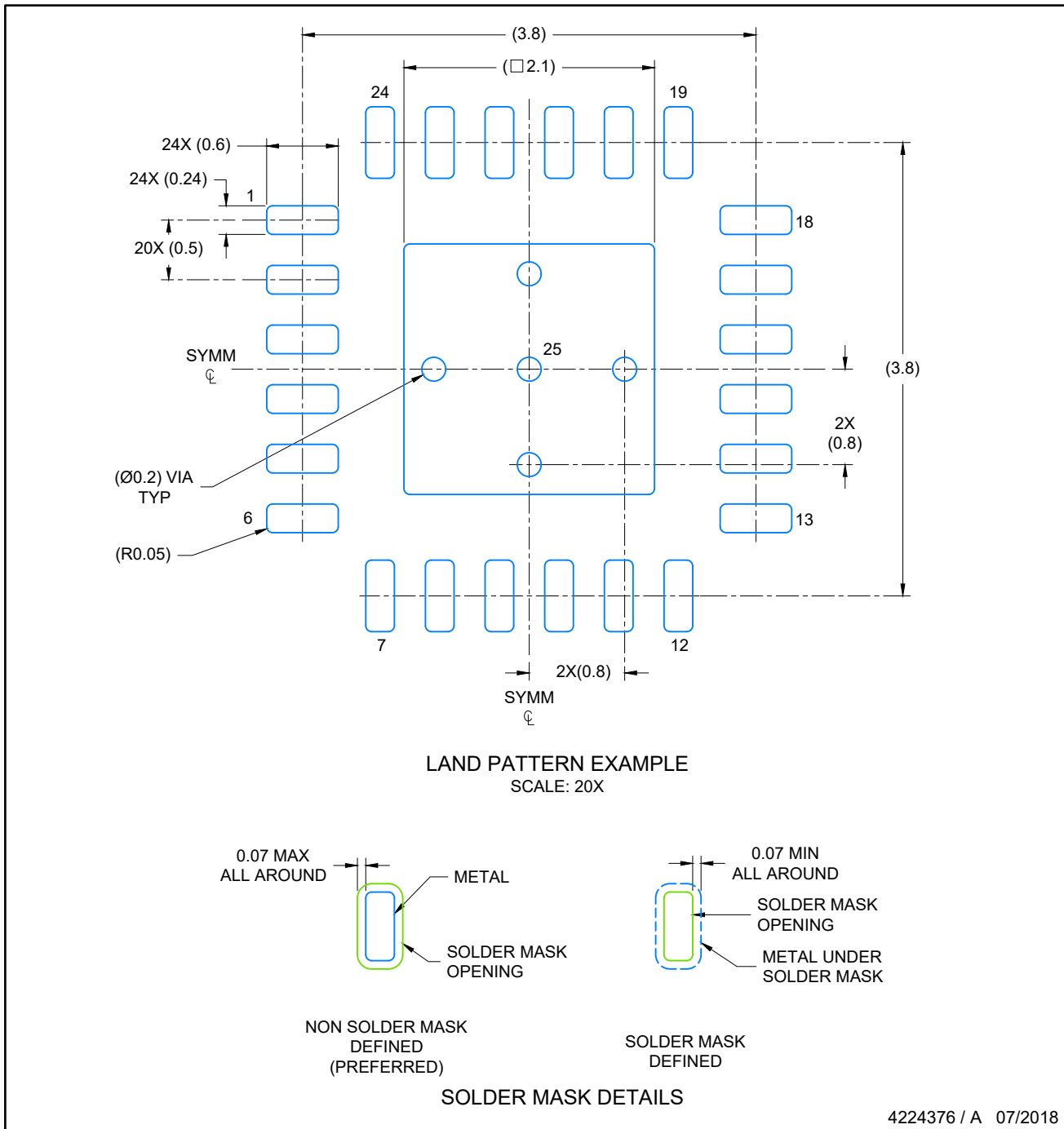
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

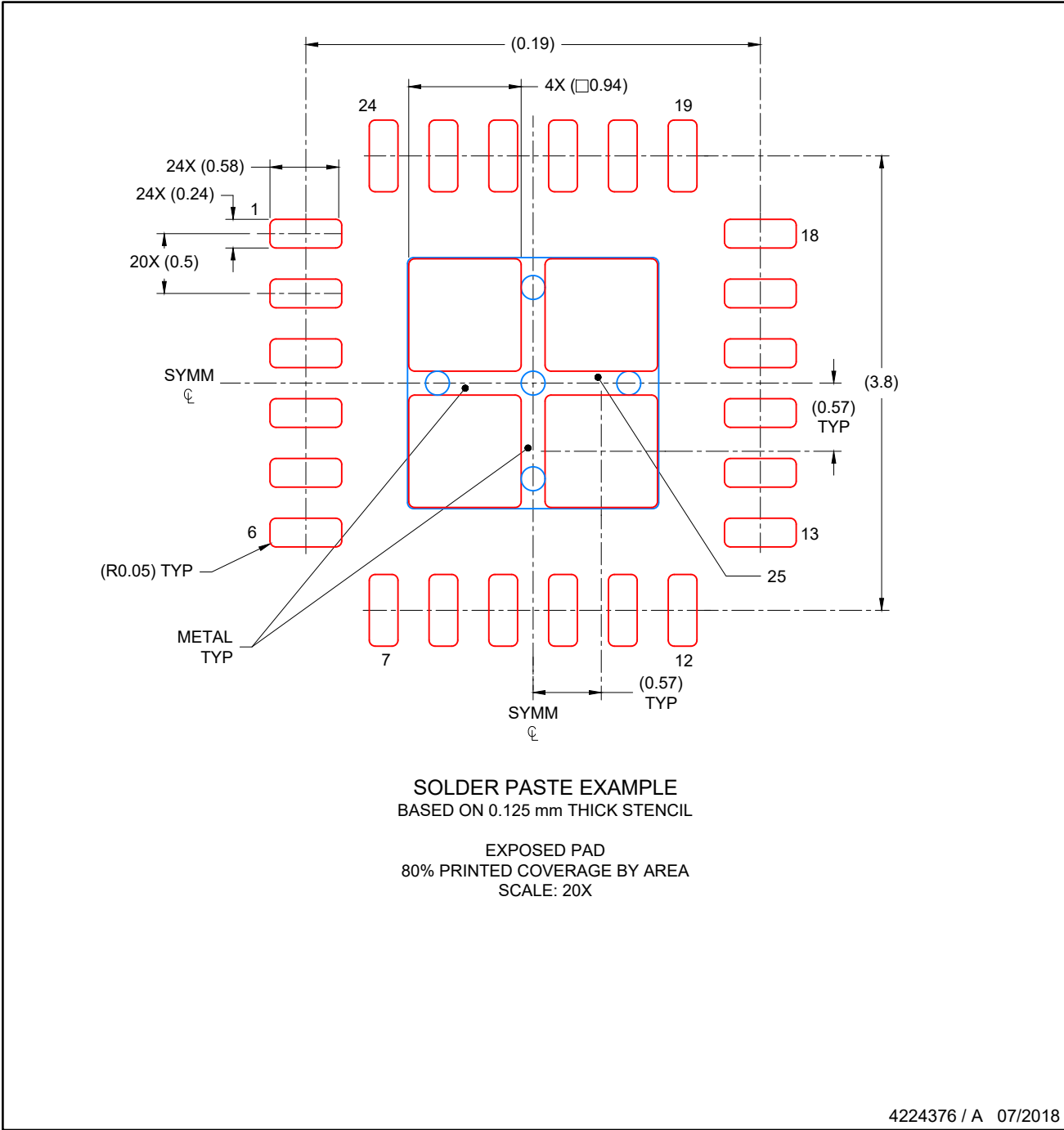
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGE0024C

PLASTIC QUAD FLATPACK- NO LEAD



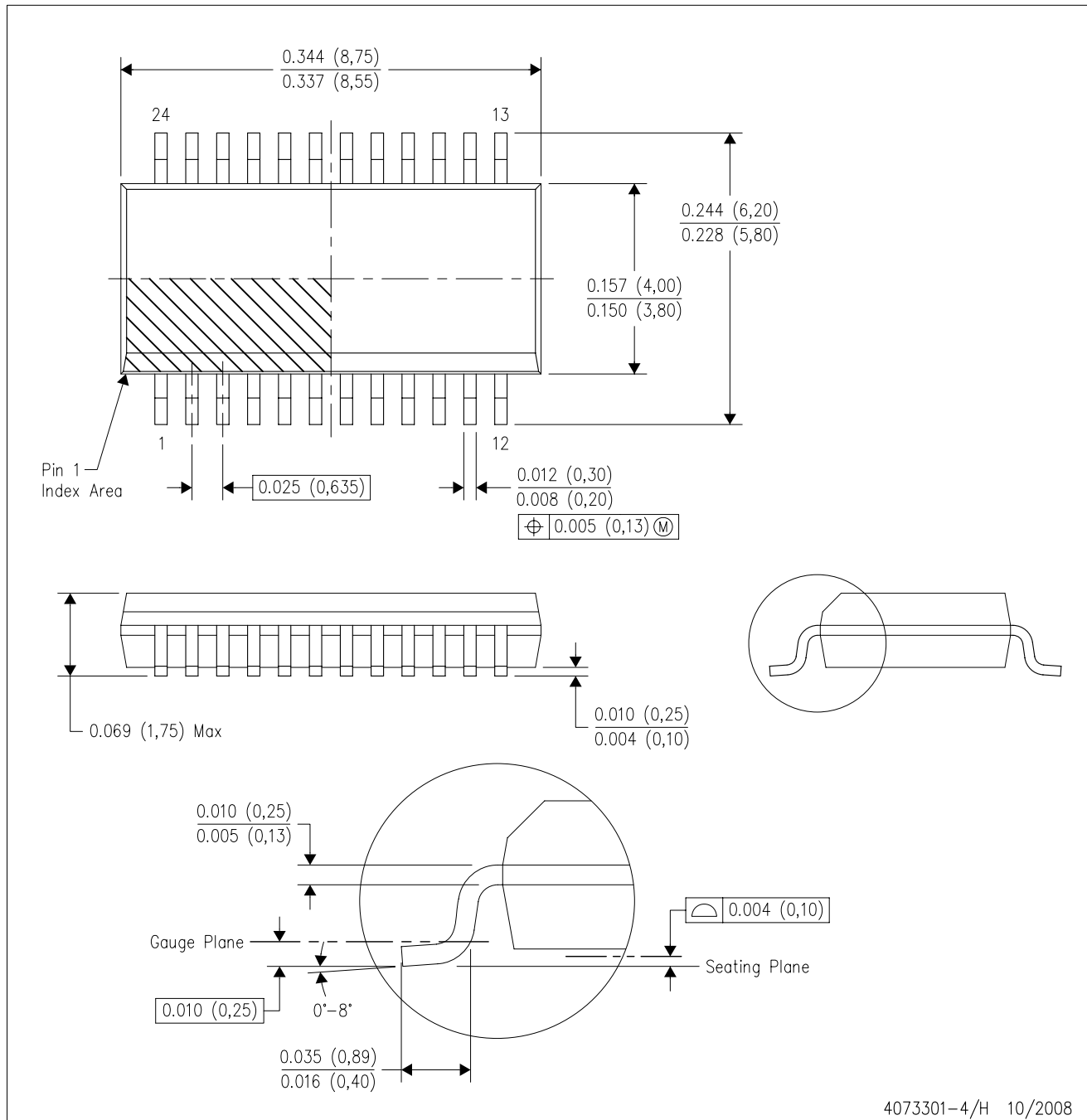
NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..



DBQ (R-PDSO-G24)

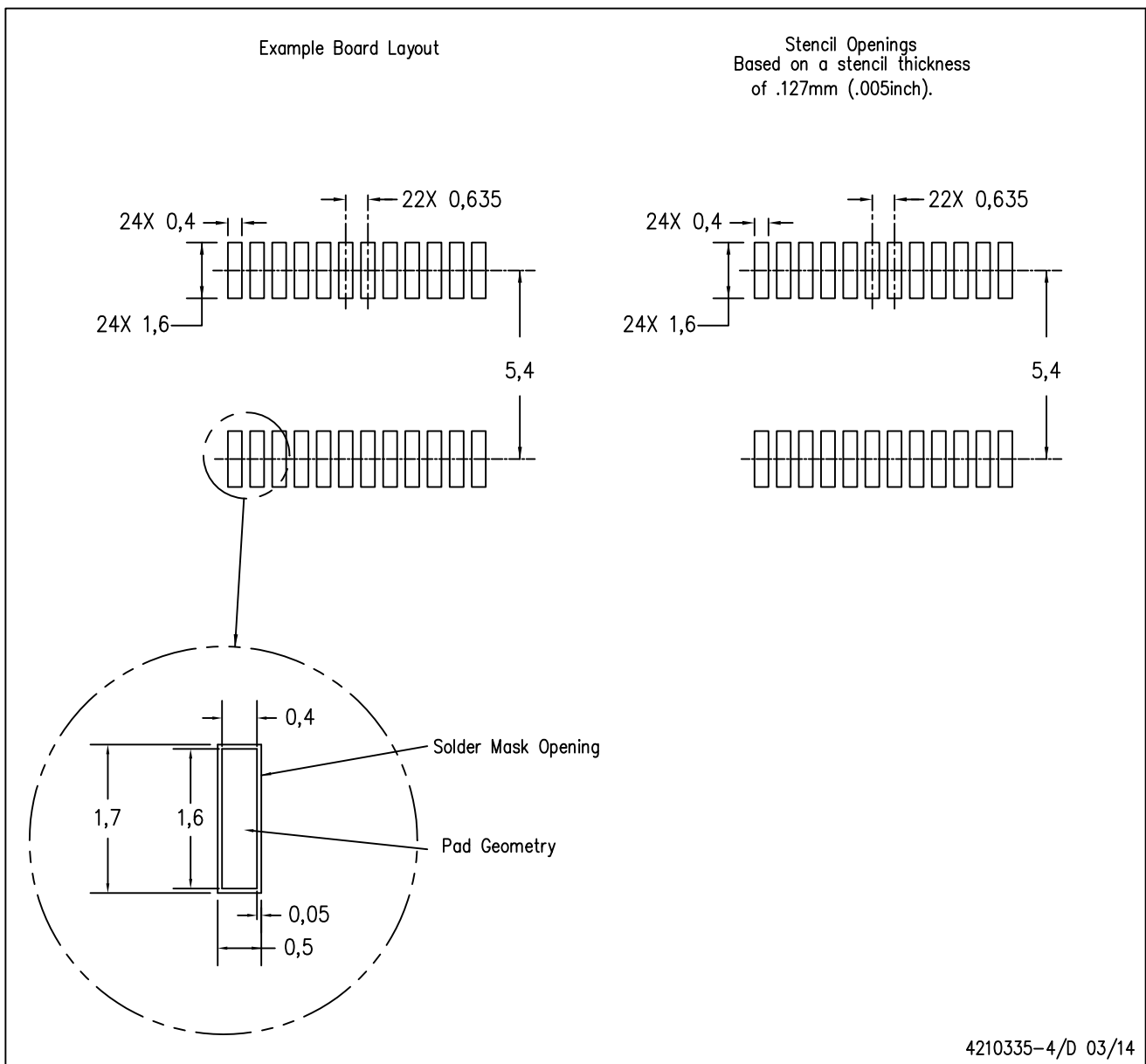
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AE.

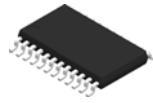
DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

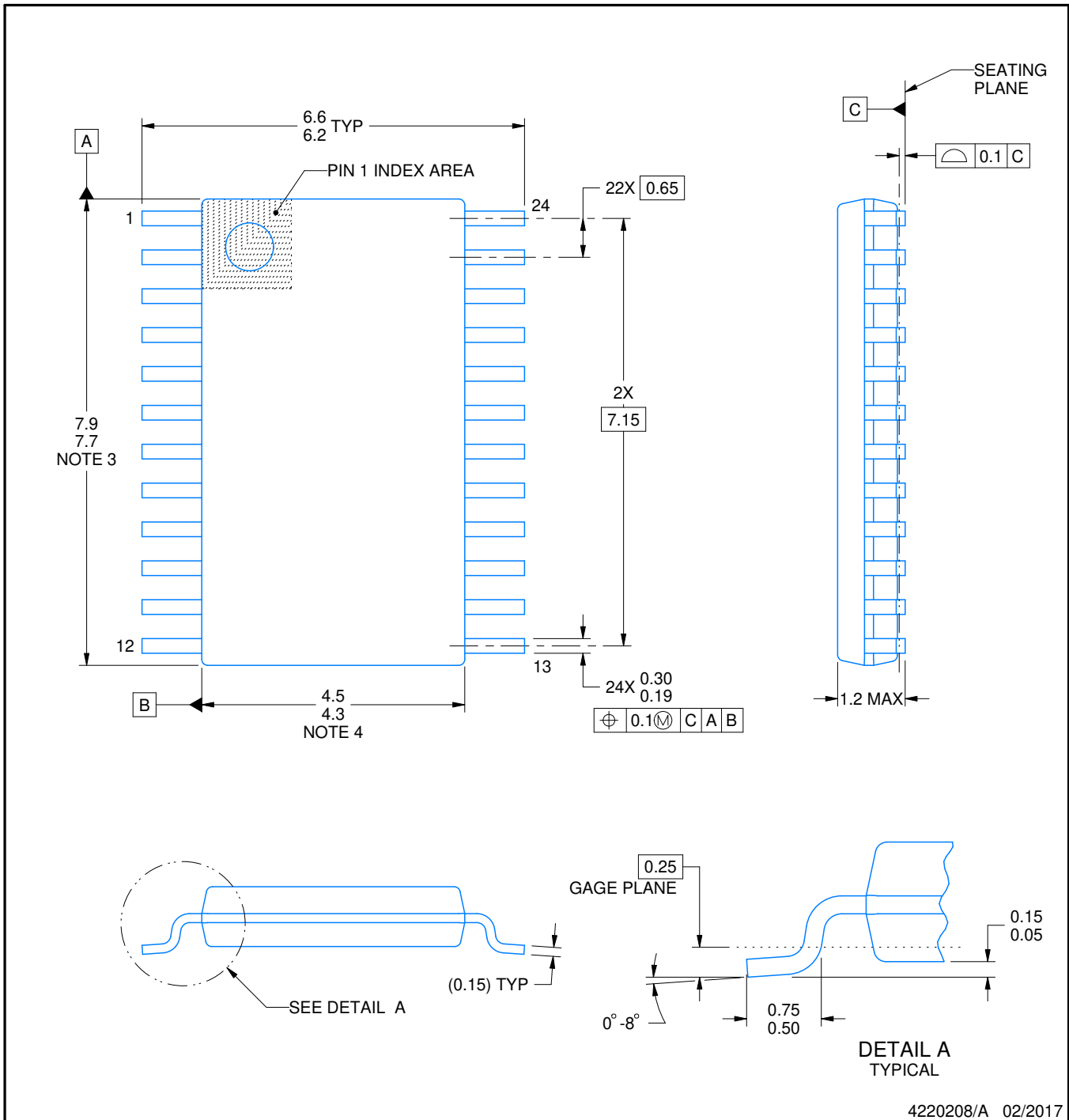
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

### NOTES:

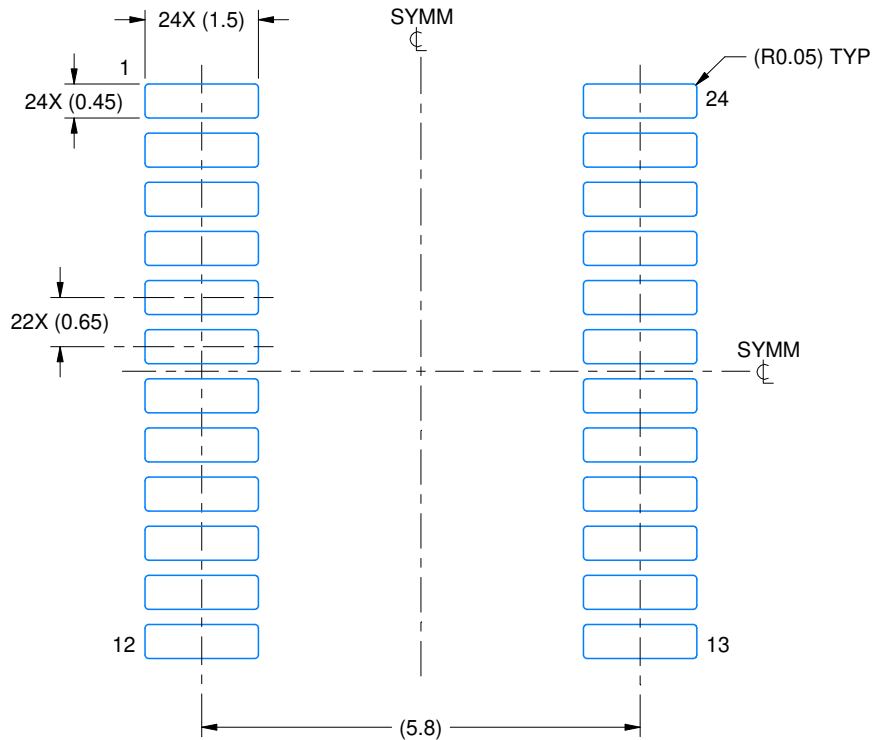
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

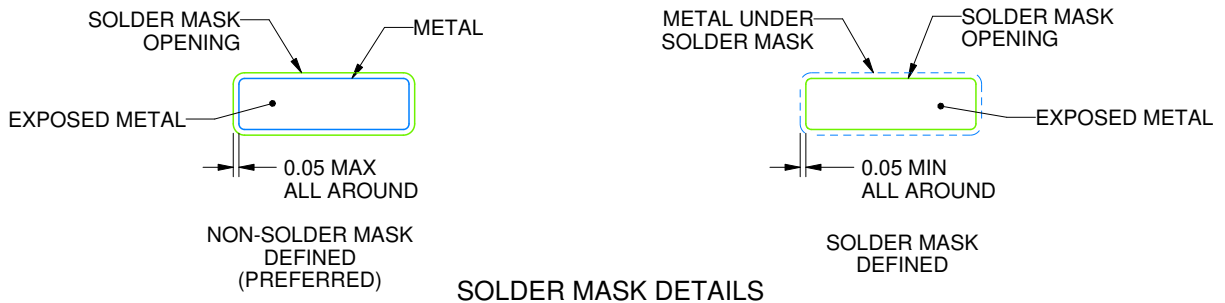
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

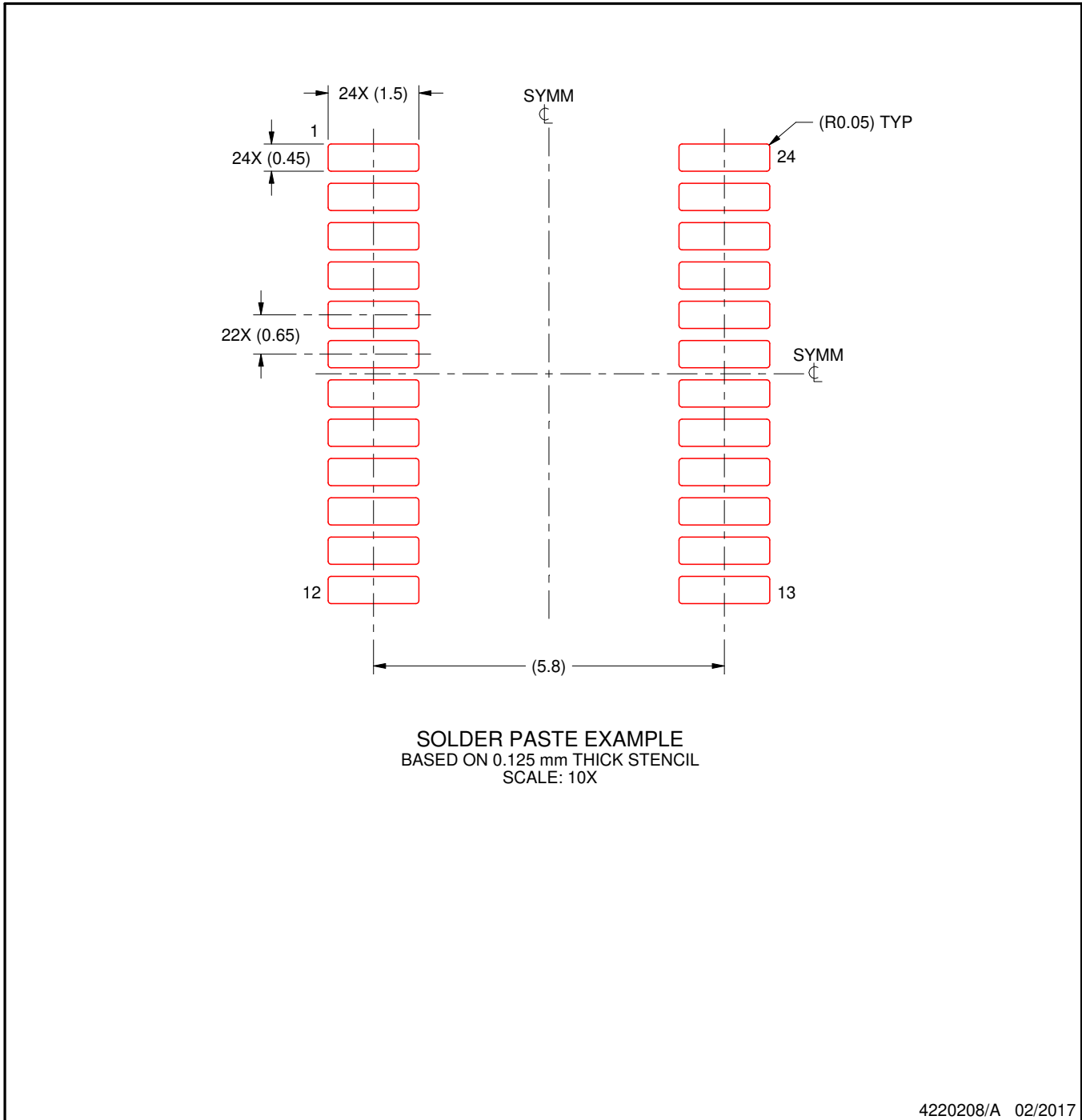
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

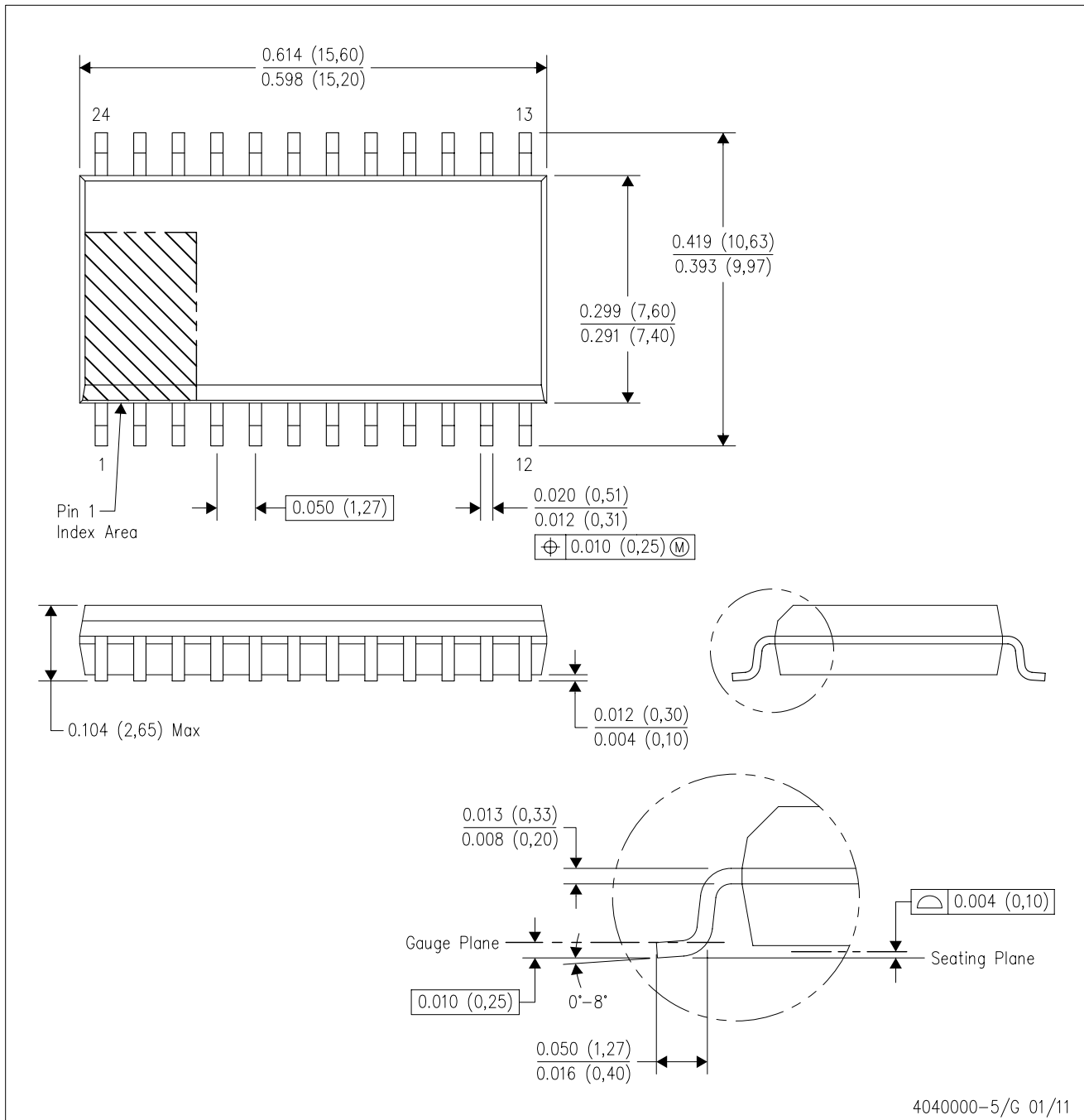
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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