

# IGLD60R070D1

## 600V CoolGaN™ enhancement-mode Power Transistor

### Features

- Enhancement mode transistor – Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- Qualified for industrial applications according to JEDEC Standards (JESD47 and JESD22)

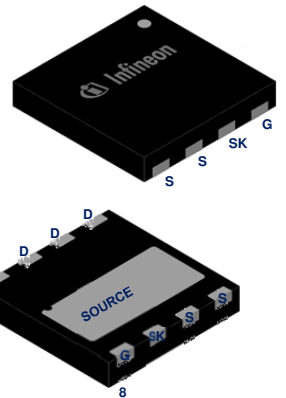
### Benefits

- Improves system efficiency
- Improves power density
- Enables higher operating frequency
- System cost reduction savings
- Reduces EMI

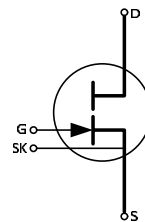
### Applications

Industrial, telecom, datacenter SMPS based on the half-bridge topology (half-bridge topologies for hard and soft switching such as Totem pole PFC, high frequency LLC).

**For other applications:** review CoolGaN™ reliability white paper and contact Infineon regional support



Gate	8
Drain	1,2,3,4
Kelvin Source	7
Source	5,6



**Table 1 Key Performance Parameters at T<sub>j</sub> = 25 °C**

Parameter	Value	Unit
V <sub>DS,max</sub>	600	V
R <sub>DS(on),max</sub>	70	mΩ
Q <sub>G,typ</sub>	5.8	nC
I <sub>D,pulse</sub>	60	A
Q <sub>oss @ 400 V</sub>	41	nC
Q <sub>rr</sub>	0	nC



**Table 2 Ordering Information**

Type / Ordering Code	Package	Marking	Related links
IGLD60R070D1	PG-LSON-8-1	60R070D1	see Appendix A

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## 1 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact your local Infineon sales office.

**Table 3 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain Source Voltage, continuous <sup>1</sup>	$V_{DS,max}$	-	-	600	V	$V_{GS} = 0\text{ V}$
Drain source destructive breakdown voltage <sup>2</sup>	$V_{DS,bd}$	800	-	-	V	$V_{GS} = 0\text{ V}$ , $I_{DS} = 12.2\text{ mA}$
Drain source voltage, pulsed <sup>2</sup>	$V_{DS,pulse}$	-	-	750	V	$T_j = 25\text{ °C}$ ; $V_{GS} \leq 0\text{ V}$ ; $\leq 1$ hour of total time $T_j = 125\text{ °C}$ , $V_{GS} \leq 0\text{ V}$ ; $\leq 1$ hour of total time
				650	V	
Switching surge voltage, pulsed <sup>2</sup>	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse} = 750\text{ V}$ ; turn on $I_{D,pulse} = 27\text{ A}$ ; $T_j = 105\text{ °C}$ ; $f \leq 100\text{ kHz}$ , $t \leq 100\text{ secs}$ (10 million pulses)
Continuous current, drain source	$I_D$	-	-	15	A	$T_C = 25\text{ °C}$ ;
Pulsed current, drain source <sup>3 4</sup>	$I_{D,pulse}$	-	-	60	A	$T_C = 25\text{ °C}$ ; $I_G = 26.1\text{ mA}$ ; See Figure 3;
Pulsed current, drain source <sup>4 5</sup>	$I_{D,pulse}$	-	-	35	A	$T_C = 125\text{ °C}$ ; $I_G = 26.1\text{ mA}$ ; See Figure 4;
Gate current, continuous <sup>4 5 6</sup>	$I_{G,avg}$	-	-	20	mA	$T_j = -55\text{ °C}$ to $150\text{ °C}$ ;
Gate current, pulsed <sup>4 6</sup>	$I_{G,pulse}$	-	-	2000	mA	$T_j = -55\text{ °C}$ to $150\text{ °C}$ ; $t_{PULSE} = 50\text{ ns}$ , $f = 100\text{ kHz}$
Gate source voltage, continuous <sup>6</sup>	$V_{GS}$	-10	-	-	V	$T_j = -55\text{ °C}$ to $150\text{ °C}$ ;
Gate source voltage, pulsed <sup>6</sup>	$V_{GS,pulse}$	-25	-	-	V	$T_j = -55\text{ °C}$ to $150\text{ °C}$ ; $t_{PULSE} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; open drain
Power dissipation	$P_{tot}$	-	-	114	W	$T_C = 25\text{ °C}$
Operating temperature	$T_j$	-55	-	150	°C	
Storage temperature	$T_{stg}$	-55	-	150	°C	Max shelf life depends on storage conditions.
Drain-source voltage slew-rate	$dV/dt$			200	V/ns	

<sup>1</sup> All devices are 100% tested at  $I_{DS} = 12.2\text{ mA}$  to assure  $V_{DS} \geq 800\text{ V}$

<sup>2</sup> Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation

<sup>3</sup> Limits derived from product characterization, parameter not measured during production

<sup>4</sup> Ensure that average gate drive current,  $I_{G,avg}$  is  $\leq 20\text{ mA}$ . Please see figure 27 for  $I_{G,avg}$ ,  $I_{G,pulse}$  and  $I_G$  details

<sup>5</sup> Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application

<sup>6</sup> We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for details

## 2 Thermal characteristics

**Table 4 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	$R_{thJC}$	-	-	1.1	°C/W	
Reflow soldering temperature	$T_{sold}$	-	-	260	°C	MSL3

### 3 Electrical characteristics

at  $T_j = 25\text{ °C}$ , unless specified otherwise

**Table 5 Static characteristics**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 0.7	1.2 1.0	1.6 1.4	V	$I_{DS} = 2.6\text{ mA}; V_{DS} = 10\text{ V}; T_j = 25\text{ °C}$ $I_{DS} = 2.6\text{ mA}; V_{DS} = 10\text{ V}; T_j = 125\text{ °C}$
Gate-Source reverse clamping voltage	$V_{GS, clamp}$	-	-	-8	V	$I_{GSS} = -1\text{ mA}$
Drain-Source leakage current	$I_{DSS}$	-	1 20	100 -	$\mu\text{A}$	$V_{DS} = 600\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$ $V_{DS} = 600\text{ V}; V_{GS} = 0\text{ V}; T_j = 150\text{ °C}$
Drain-Source leakage current at application conditions <sup>1</sup>	$I_{DSSapp}$	-	60	-	$\mu\text{A}$	$V_{DS} = 400\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ °C}$
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.055 0.100	0.070 -	$\Omega$	$I_G = 26.1\text{ mA}; I_D = 8\text{ A}; T_j = 25\text{ °C}$ $I_G = 26.1\text{ mA}; I_D = 8\text{ A}; T_j = 150\text{ °C}$
Gate resistance	$R_{G,int}$	-	0.78	-	$\Omega$	LCR impedance measurement; $f = f_{res}$ ; open drain;

**Table 6 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	380	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V};$ $f = 1\text{ MHz}$
Output capacitance	$C_{oss}$	-	72	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V};$ $f = 1\text{ MHz}$
Reverse Transfer capacitance	$C_{rss}$	-	0.3	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V};$ $f = 1\text{ MHz}$
Effective output capacitance, energy related <sup>2</sup>	$C_{o(er)}$	-	80	-	pF	$V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related <sup>3</sup>	$C_{o(tr)}$	-	102.5	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V};$ $I_D = \text{const}$
Output charge	$Q_{oss}$	-	41	-	nC	$V_{DS} = 0\text{ to }400\text{ V}$
Turn- on delay time	$t_{d(on)}$	-	10	-	ns	see Figure 23
Turn- off delay time	$t_{d(off)}$	-	14	-	ns	see Figure 23
Rise time	$t_r$	-	8	-	ns	see Figure 23
Fall time	$t_f$	-	15	-	ns	see Figure 23

<sup>1</sup> Parameter represents end of use leakage in applications

<sup>2</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

<sup>3</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

**Table 7 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	$Q_G$	-	5.8	-	nC	$I_{GS} = 0$ to 10 mA; $V_{DS} = 400$ V; $I_D = 8$ A

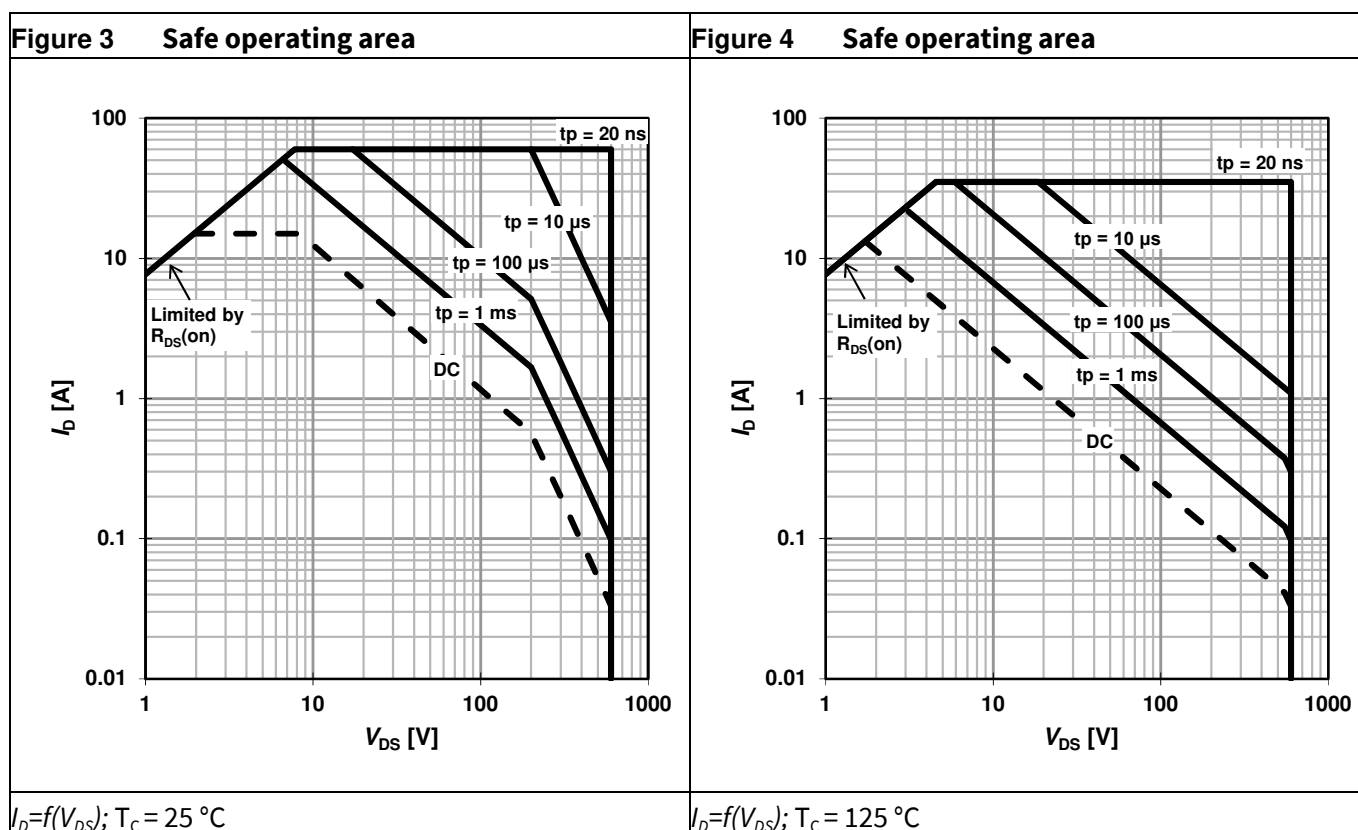
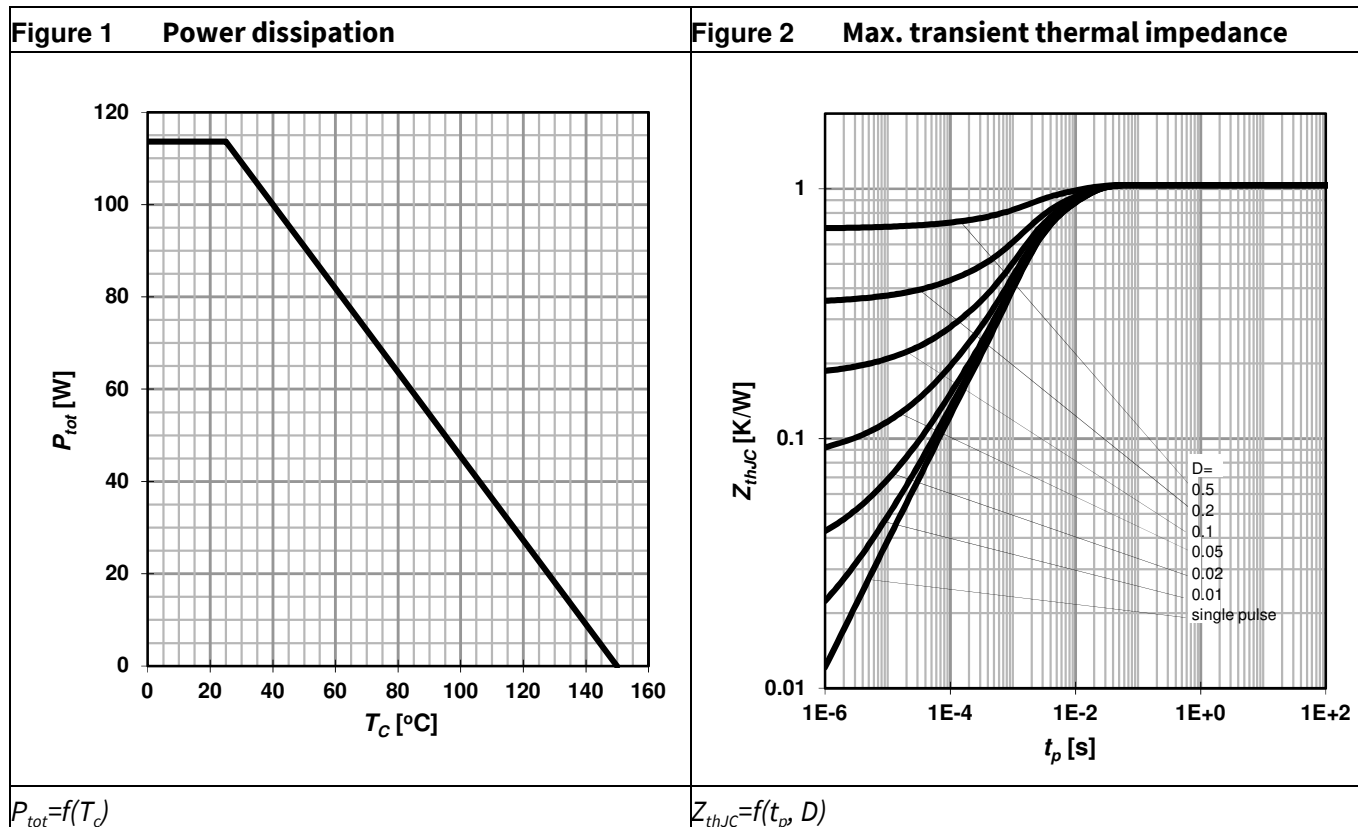
**Table 8 Reverse conduction characteristics**

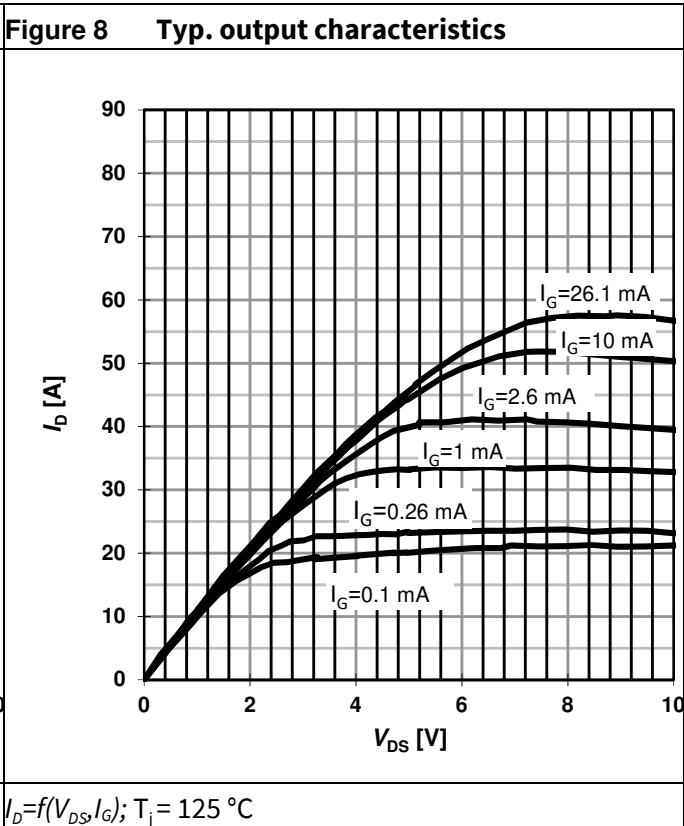
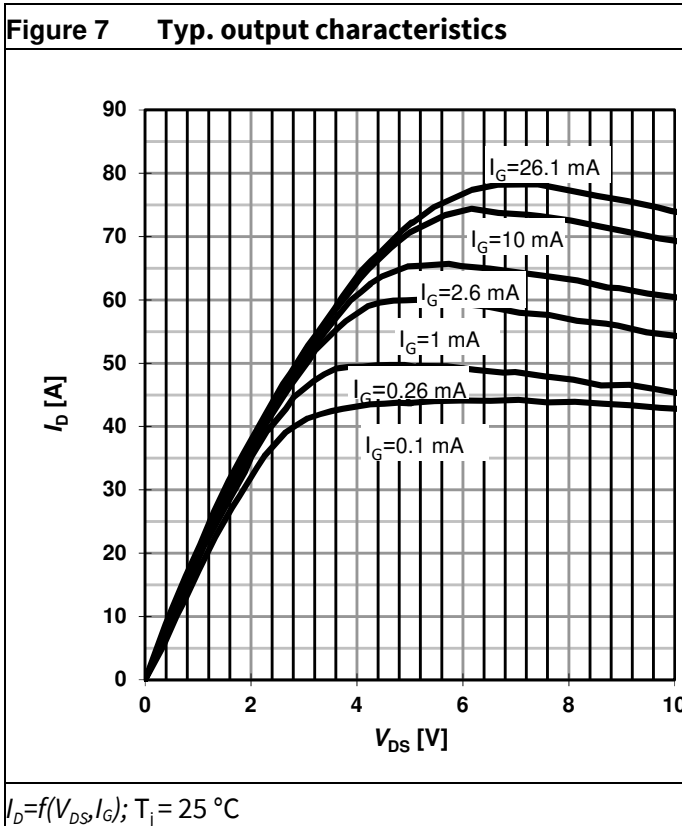
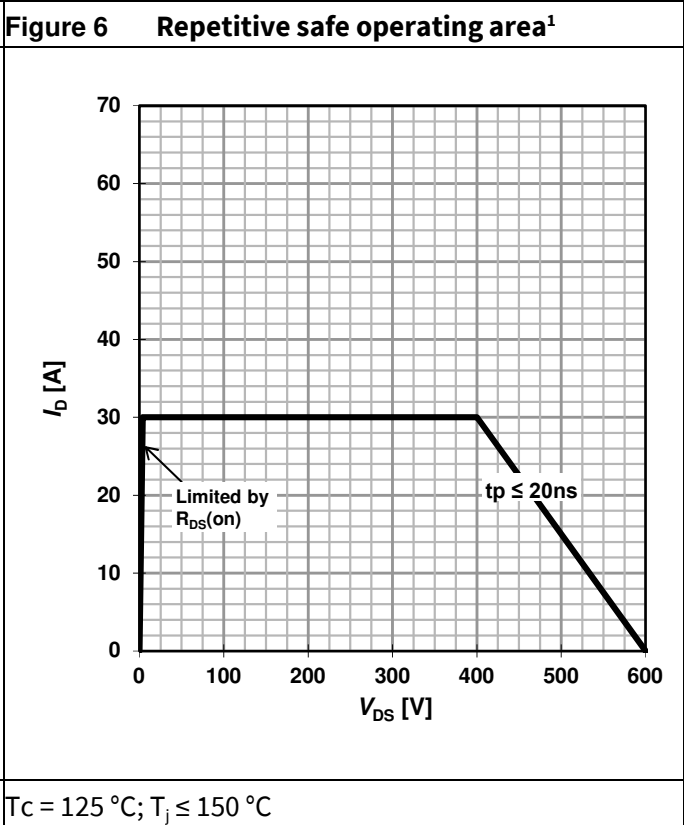
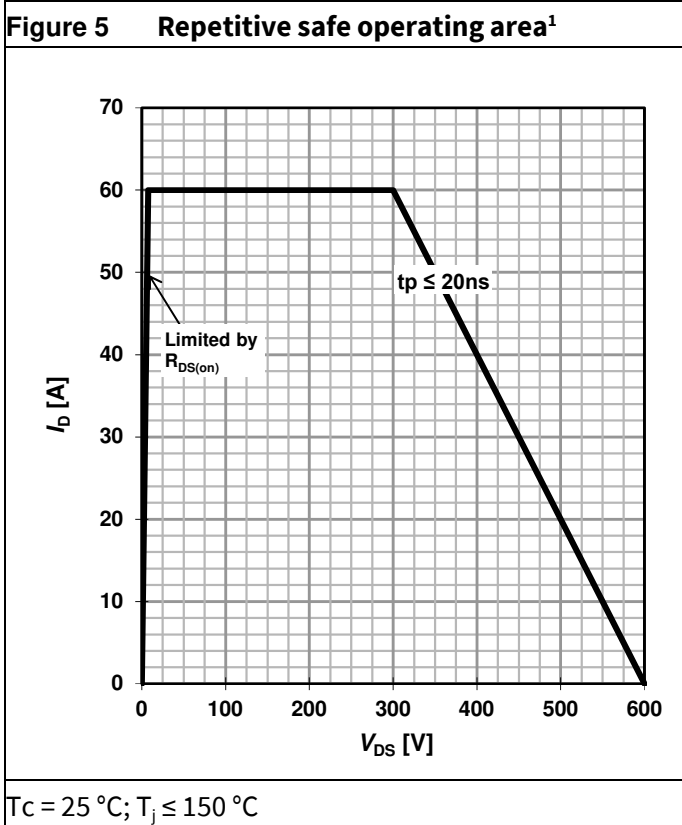
Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	$V_{SD}$	-	2.2	2.5	V	$V_{GS} = 0$ V; $I_{SD} = 8$ A
Pulsed current, reverse	$I_{S,pulse}$	-	-	60	A	$I_G = 26.1$ mA
Reverse recovery charge	$Q_{rr}^1$	-	0	-	nC	$I_S = 8$ A, $V_{DS} = 400$ V
Reverse recovery time	$t_{rr}$	-	0	-	ns	
Peak reverse recovery current	$I_{rrm}$	-	0	-	A	

<sup>1</sup> Excluding  $Q_{oss}$   
 Final Data Sheet

## 4 Electrical characteristics diagrams

at  $T_j = 25\text{ }^\circ\text{C}$ , unless specified otherwise

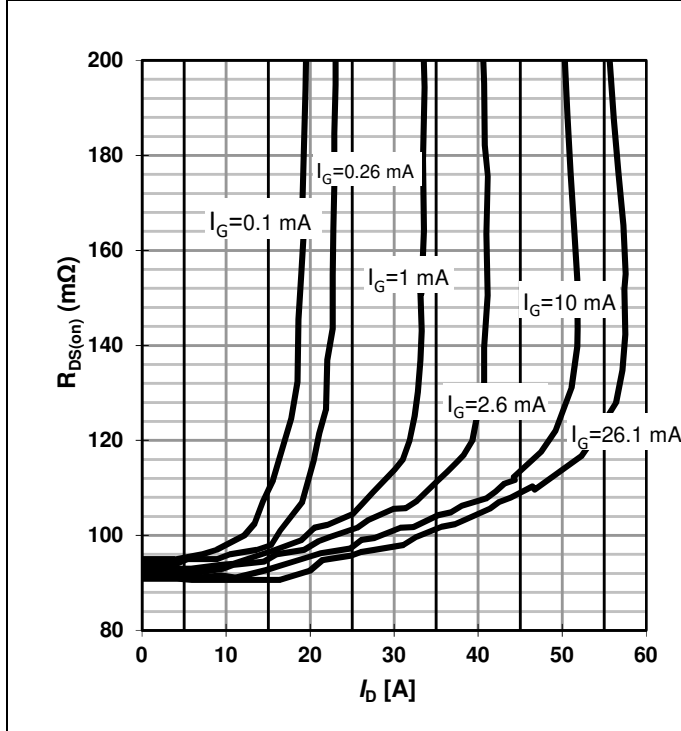




<sup>1</sup> Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application.

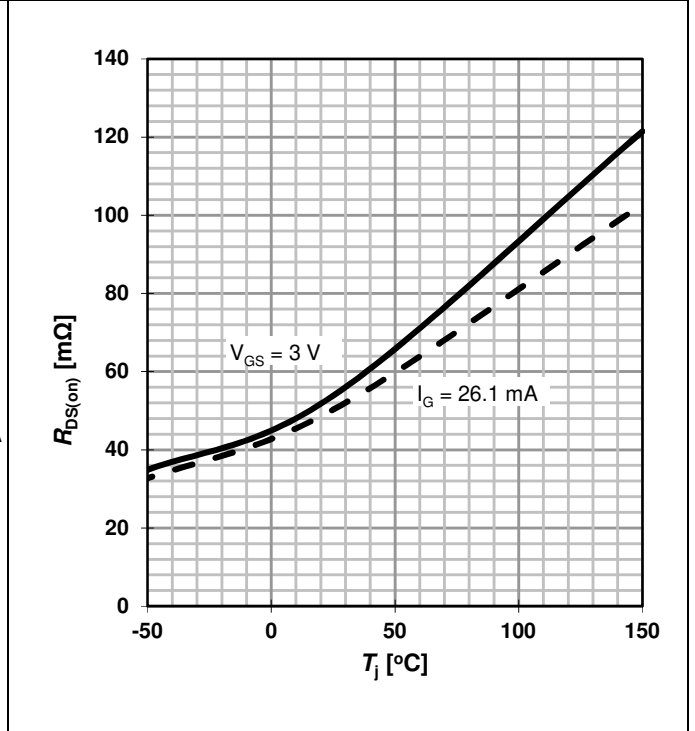


**Figure 9** Typ. Drain-source on-state resistance



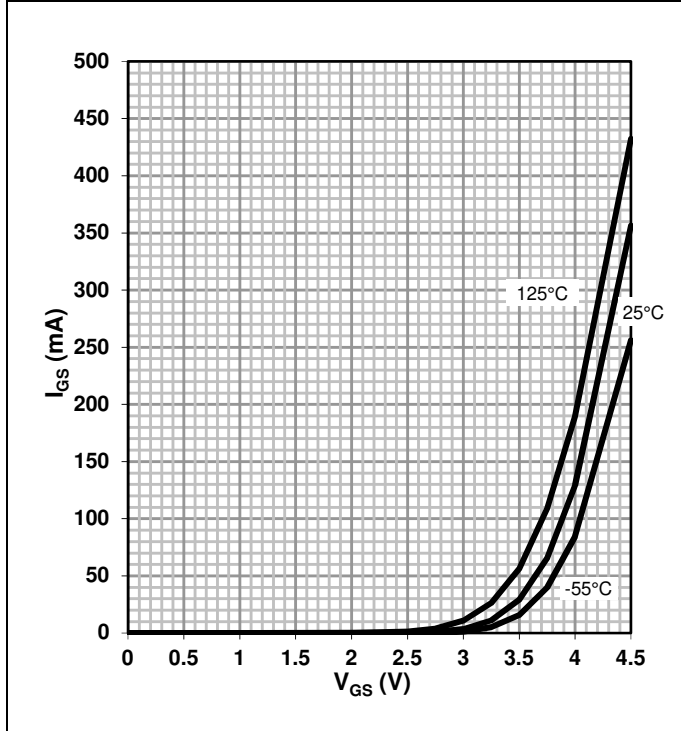
$R_{DS(on)} = f(I_D, I_G); T_j = 125^\circ\text{C}$

**Figure 10** Drain-source on-state resistance



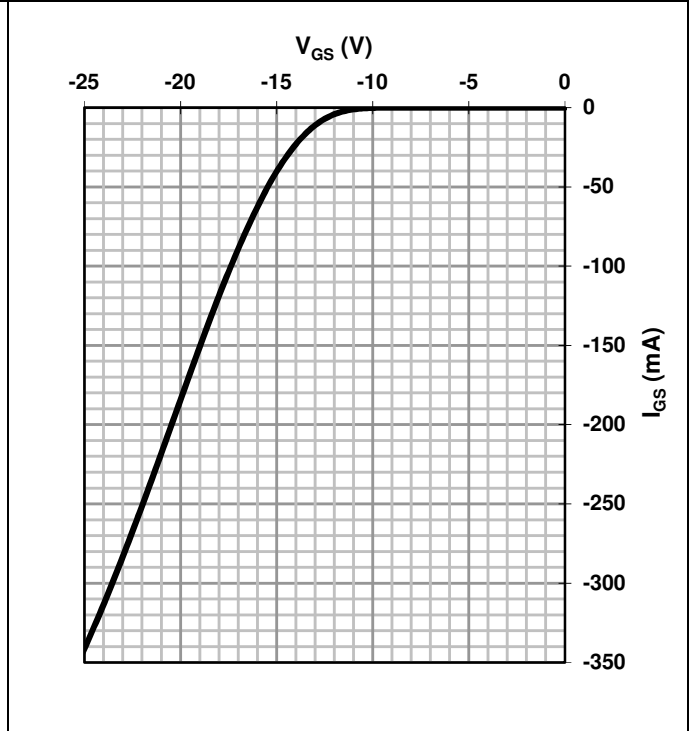
$R_{DS(on)} = f(T_j); I_D = 8$  A

**Figure 11** Typ. gate characteristics forward



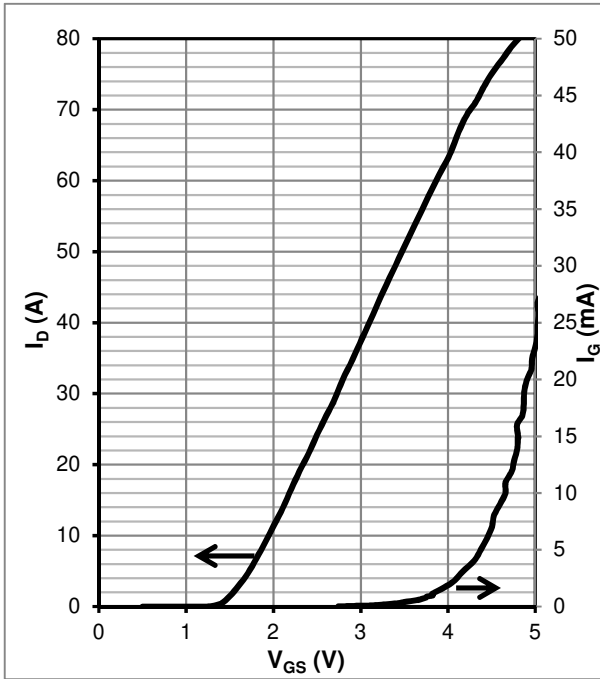
$I_{GS} = f(V_{GS}, T_j);$  open drain

**Figure 12** Typ. gate characteristics reverse



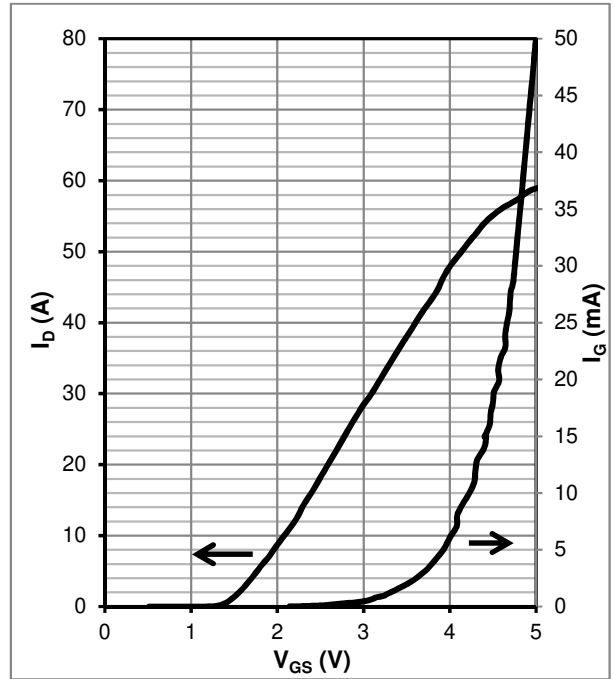
$I_{GS} = f(V_{GS}); T_j = 25^\circ\text{C}$

**Figure 13** Typ. transfer characteristics



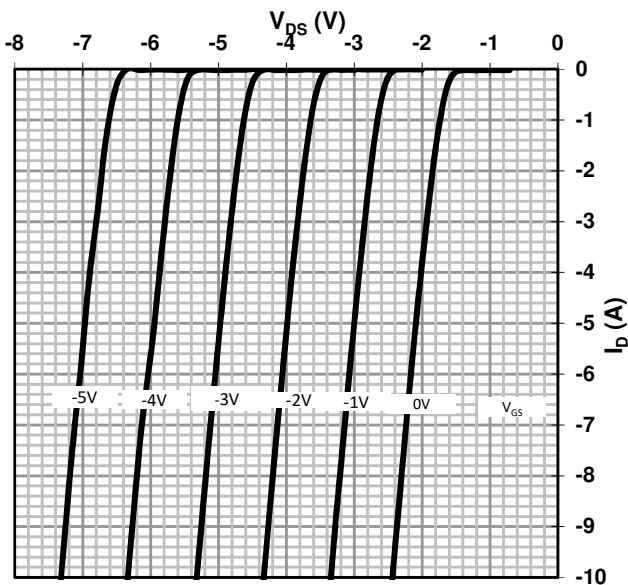
$I_D, I_G = f(V_{GS}); V_{DS} = 8 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

**Figure 14** Typ. transfer characteristics



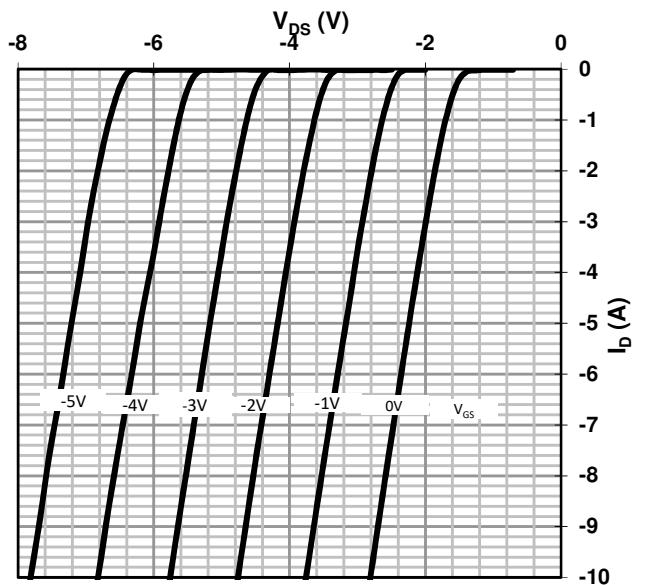
$I_D, I_G = f(V_{GS}); V_{DS} = 8 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$

**Figure 15** Typ. channel reverse characteristics



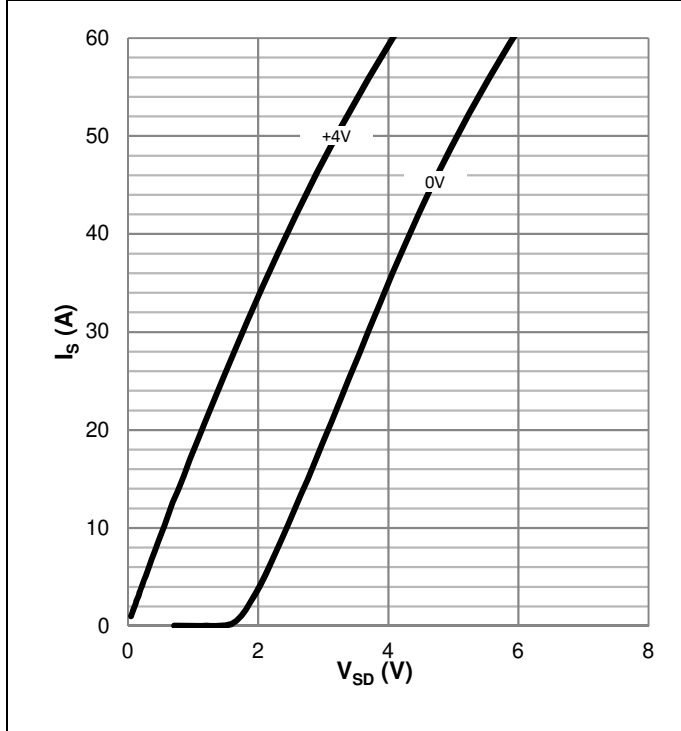
$V_{DS} = f(I_D, V_{GS}); T_j = 25 \text{ }^\circ\text{C}$

**Figure 16** Typ. channel reverse characteristics



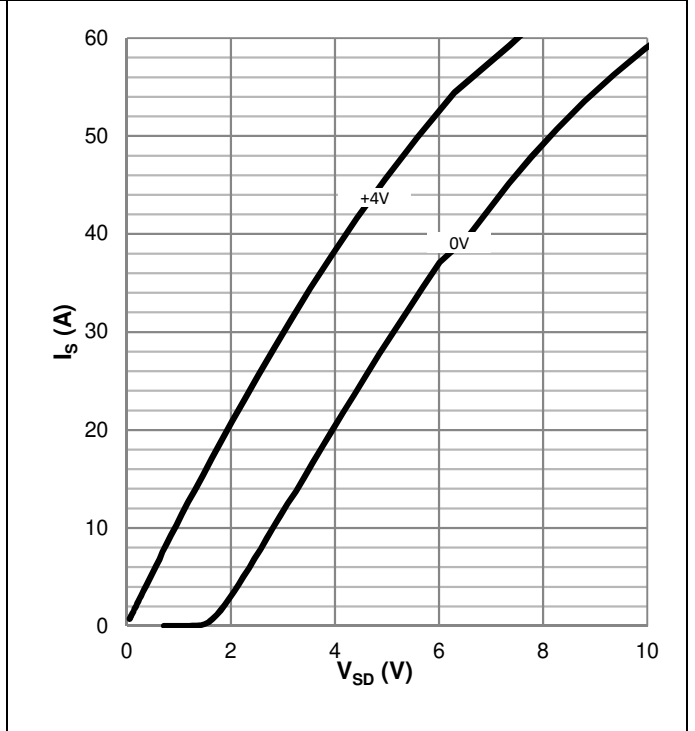
$V_{DS} = f(I_D, V_{GS}); T_j = 125 \text{ }^\circ\text{C}$

**Figure 17** Typ. channel reverse characteristics



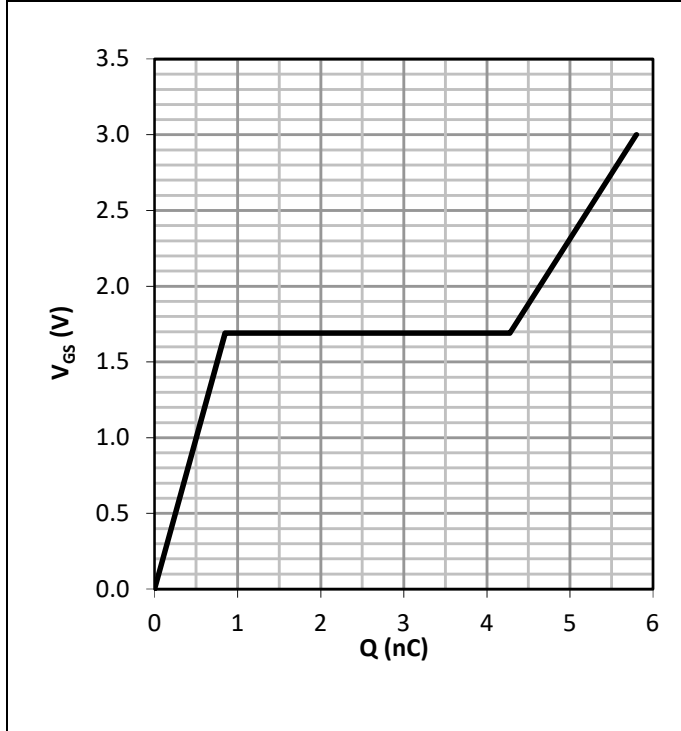
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ °C}$

**Figure 18** Typ. channel reverse characteristics



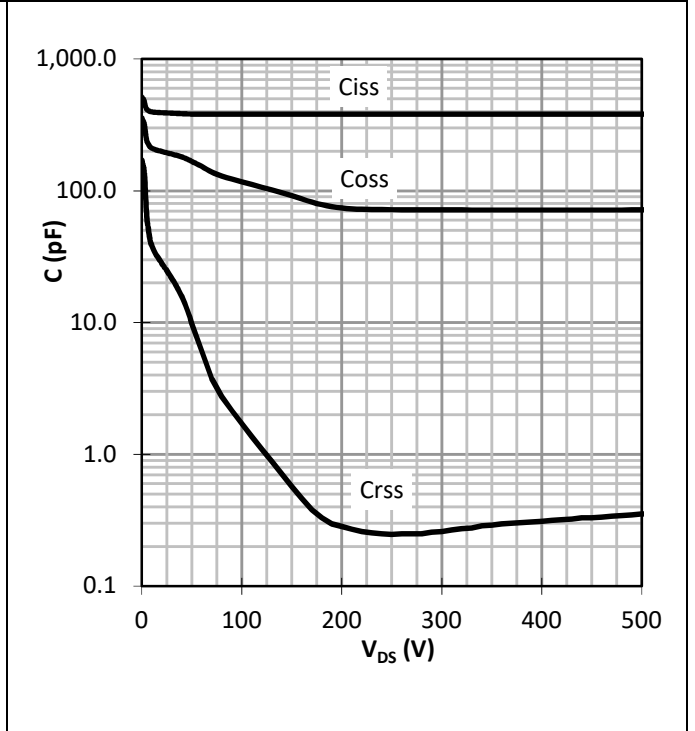
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ °C}$

**Figure 19** Typ. gate charge

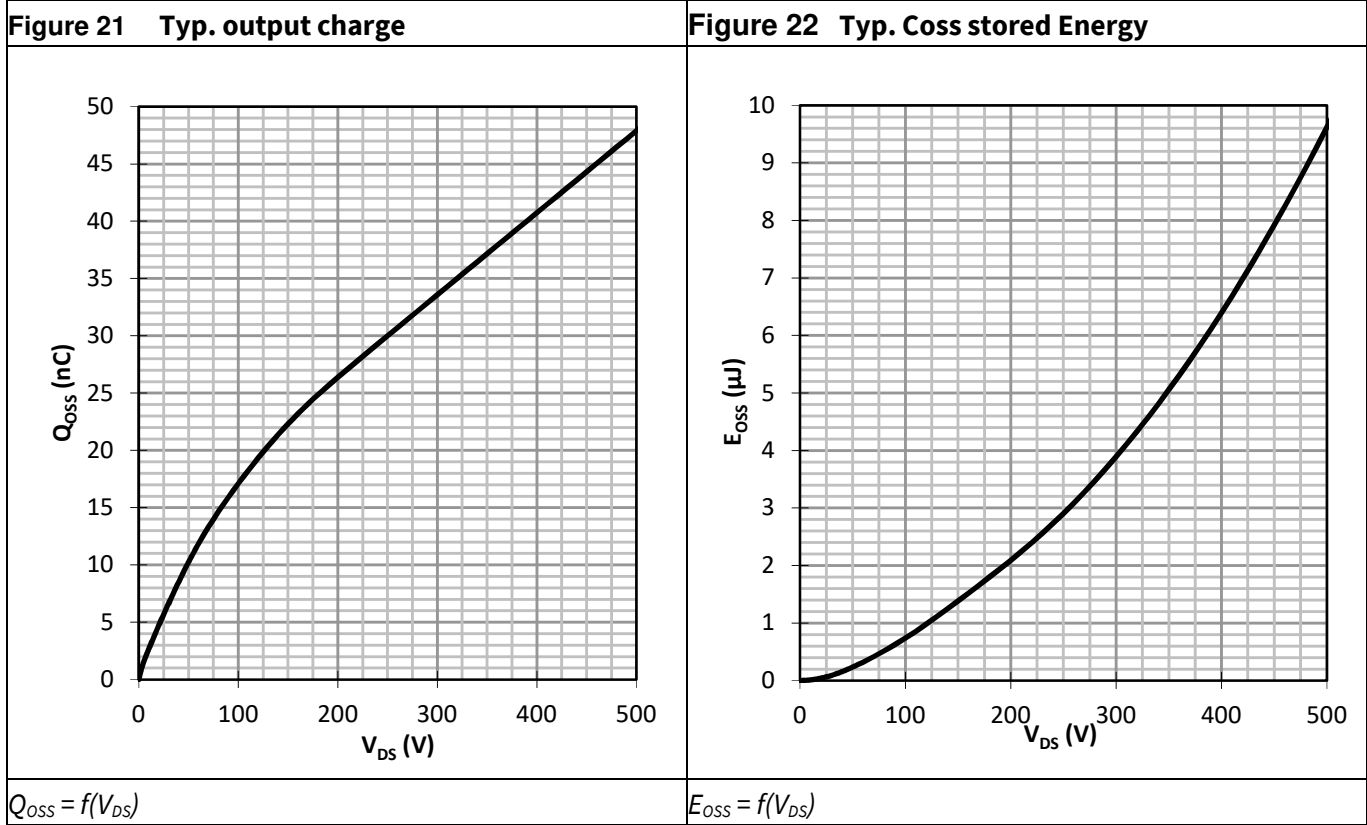


$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 8\text{ A}$

**Figure 20** Typ. capacitances

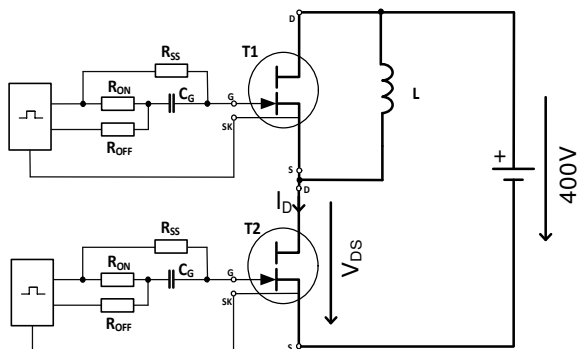


$C_{xSS} = f(V_{DS})$



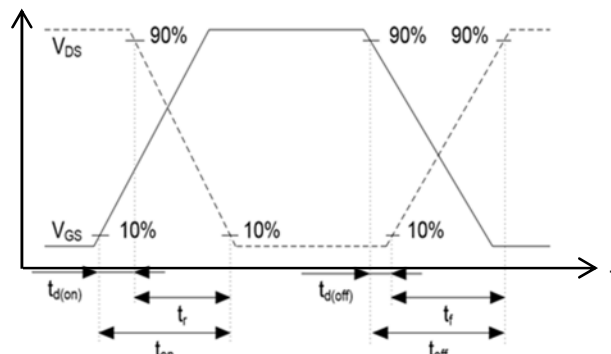
## 5 Test Circuits

**Figure 23 Switching times with inductive load**

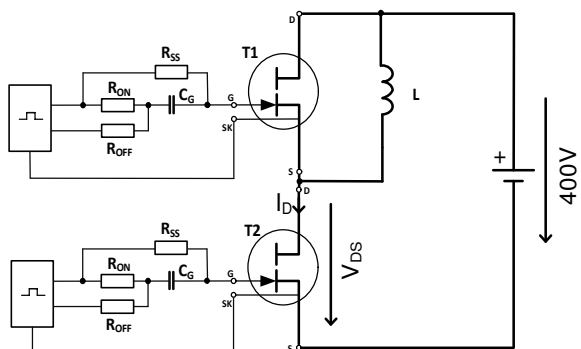


$I_D = 8A$ ,  $R_{ON} = 5\ \Omega$ ;  $R_{OFF} = 5\ \Omega$ ;  $R_{SS} = 300\ \Omega$ ;  
 $C_G = 3.3\ nF$ ;  $V_{DBV} = 12V$

**Figure 24 Switching times waveform**

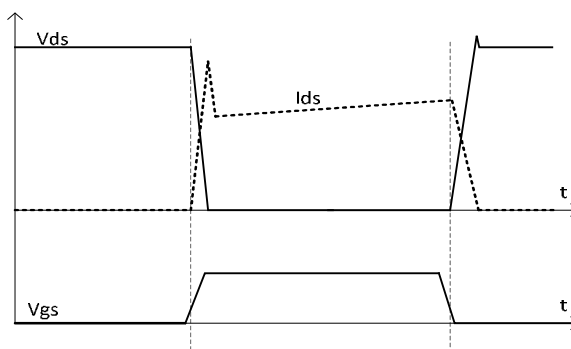


**Figure 25 Reverse Channel Characteristics Test**



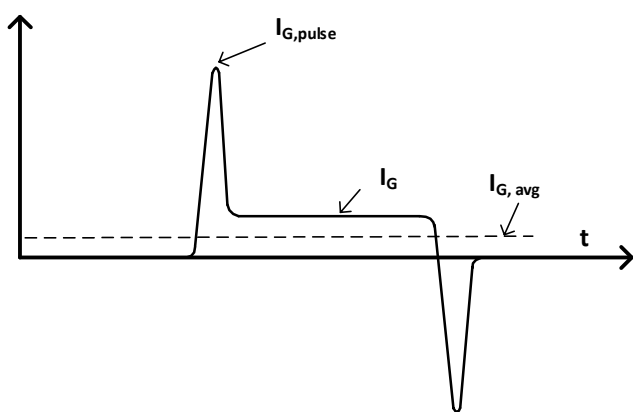
$I_D = 8A$ ,  $R_{ON} = 5\ \Omega$ ;  $R_{OFF} = 5\ \Omega$ ;  $R_{SS} = 300\ \Omega$ ;  
 $C_G = 3.3\ nF$ ;  $V_{DBV} = 12V$

**Figure 26 Typical Reverse Channel Recovery**



The recovery charge is  $Q_{oss}$  only, no additional  $Q_{rr}$

**Figure 27 Gate current switching waveform**



## 6 Package Outlines

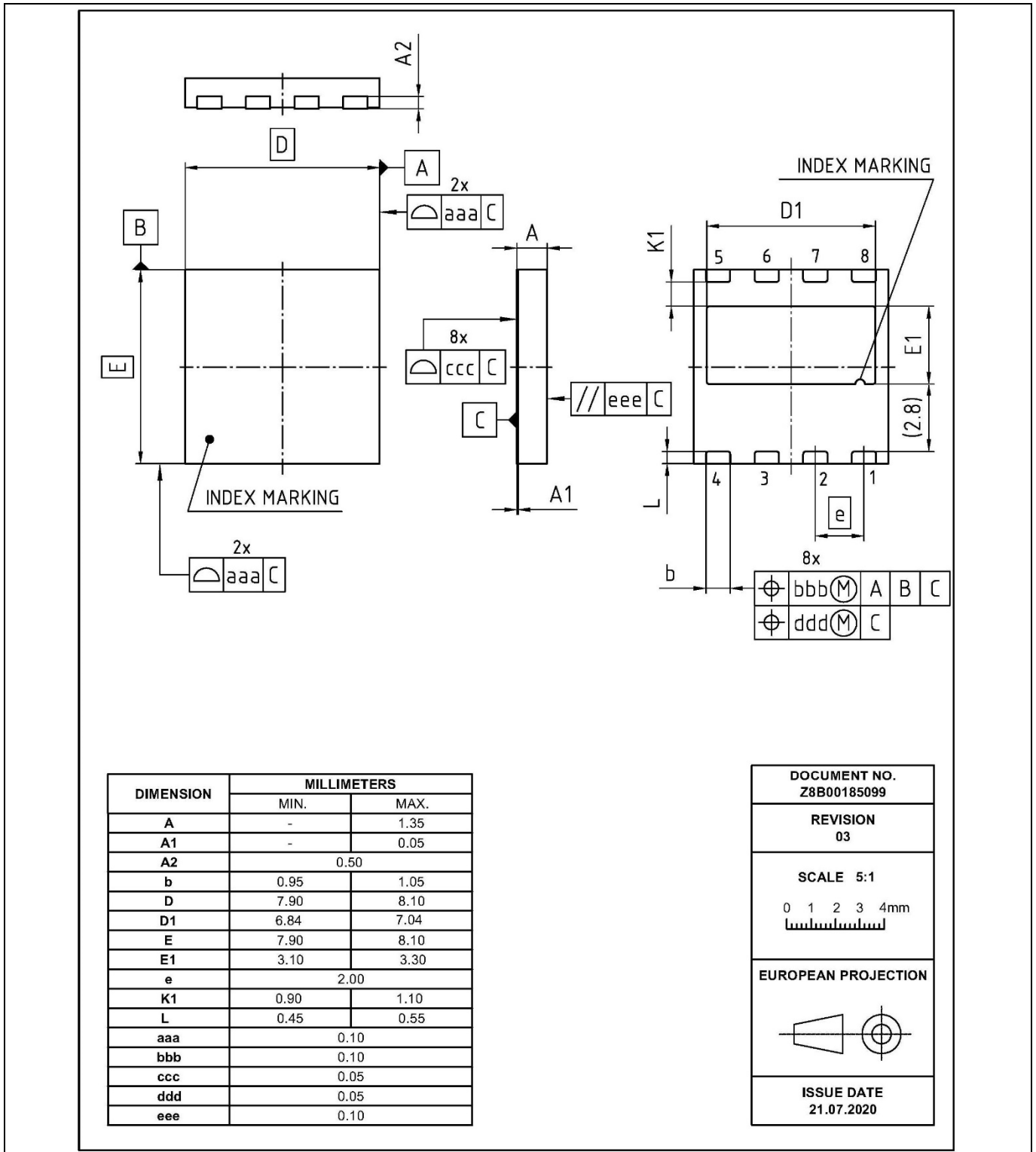


Figure 28 PG-LSON-8-1 Package Outline, dimensions (mm)

## 7 Appendix A

Table 9 Related links

- IFX CoolGaN™ webpage: [www.infineon.com/why-coolgan](http://www.infineon.com/why-coolgan)
- IFX CoolGaN™ reliability white paper: [www.infineon.com/gan-reliability](http://www.infineon.com/gan-reliability)
- IFX CoolGaN™ gate drive application note: [www.infineon.com/driving-coolgan](http://www.infineon.com/driving-coolgan)
- IFX CoolGaN™ applications information:
  - [www.infineon.com/gan-in-server-telecom](http://www.infineon.com/gan-in-server-telecom)
  - [www.infineon.com/gan-in-wirelesscharging](http://www.infineon.com/gan-in-wirelesscharging)
  - [www.infineon.com/gan-in-audio](http://www.infineon.com/gan-in-audio)
  - [www.infineon.com/gan-in-adapter-charger](http://www.infineon.com/gan-in-adapter-charger)

## 8 Revision History

### Major changes since the last revision

Revision	Date	Description of changes
2.0	2018-10-12	Final version release
2.1	2020-01-16	Added $V_{DS,bd}$ , $V_{DS,pulse}$ , $V_{DS,surge}$ specifications in maximum ratings table of page 3
2.11	2020-08-07	Updated package tolerances in Figure 28
2.12	2021-04-27	Updated $T_{sold}$ specification to 260°C in table 4; Updated $I_{GSS}$ specification at 125°C to -2 mA in table 5; updated repetitive SOA at $T_c = 125^\circ\text{C}$ to 30A in Figure 6; updated switching times and related test conditions
2.13	2021-10-26	Replaced $I_{GSS}$ specification with $V_{GS,clamp}$ in table 5

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