

## Evaluation Board for the **ADP2443** 3 A, 36 V, Synchronous, Step-Down Regulator

### FEATURES

- Full featured evaluation board for the **ADP2443**
- Compact solution size
- 4-layer high glass transition temperature ( $T_g$ ) printed circuit board (PCB) for superior thermal performance
- Convenient connections through vertical printed circuit tail pin headers
- Supply voltage
  - 4.5 V to 36 V for PVIN
- Synchronization capable
- Independent enable control
- Power-good output

### APPLICATIONS

- Full evaluation of the **ADP2443**

### EVALUATION KIT CONTENTS

- ADP2443-EVALZ** evaluation board

### DOCUMENT NEEDED

- ADP2443** data sheet

### EQUIPMENT NEEDED

- DC power supply
- Electronic load
- Oscilloscope

### GENERAL DESCRIPTION

The **ADP2443-EVALZ** evaluation board provides a complete and compact solution that allows users to evaluate all the performance of the **ADP2443** with a near ideal PCB layout.

The main device on the evaluation board, the **ADP2443**, is a synchronous step-down, dc-to-dc regulator with both high-side and low-side MOSFETs integrated to provide a high efficiency solution in a compact, 4 mm × 4 mm LFCSP package.

The evaluation board has independent enable control, which allows flexible configuration when evaluating the **ADP2443**.

Full details on the **ADP2443** regulator are provided in the **ADP2443** data sheet, available from Analog Devices, Inc. Consult the data sheet in conjunction with this user guide when working with this evaluation board.

### EVALUATION BOARD PHOTOGRAPH

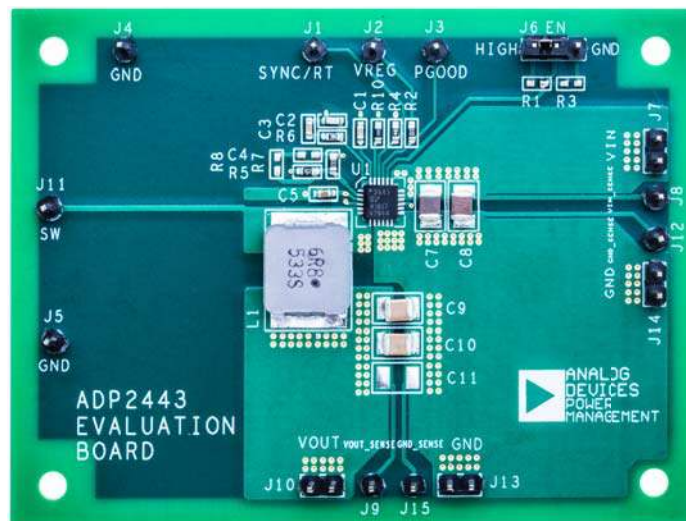


Figure 1.

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**REVISION HISTORY**

**9/2016—Revision 0: Initial Version**

## USING THE EVALUATION BOARD

### POWERING UP

The [ADP2443-EVALZ](#) evaluation board is supplied fully assembled and tested. Before applying power to the evaluation board, follow the procedures in this section.

#### **Jumper J6 (EN)**

To enable the regulator, short the middle pin of J6 (EN) high.

To disable the regulator, short the middle pin of J6 (EN) to GND.

#### **Input Power Source**

If the input dc power source includes a current meter, use that meter to monitor the input current. Connect the positive terminal of the power source to J7 (PVIN) of the evaluation board, and the negative terminal of the power source to J14 (GND) of the evaluation board.

If the dc power source does not include a current meter, connect a current meter in series with the input source voltage. Connect the positive lead (+) of the power source to the positive (+) ammeter terminal, the negative lead (–) of the power source to J14 (GND), and the negative lead (–) of the ammeter to J7 (PVIN).

#### **Output Load**

Before connecting the load, ensure that the regulator is turned off. Connect an electronic load or resistor for the regulator to set the load current.

Connect the positive terminal of the load to J10 (VOUT) of the evaluation board and connect the negative terminal of the load to J13 (GND).

#### **Input and Output Voltmeter**

Measure the input and output voltages using voltmeters. Ensure that the voltmeters are connected to the appropriate terminals of evaluation board and not to the load or power source. If the voltmeters are not connected directly to the evaluation board, the measured voltages are incorrect due to the voltage drop across the leads and/or connections between the evaluation board, the power source, and/or the load.

To measure the input voltage, connect the positive terminal of the voltmeter to J8 (PVIN\_SNS) and the negative terminal to J12 (GND\_SNS). Likewise, to measure the output voltage, connect the positive terminal of the voltmeter to J9 (VOUT\_SNS) and the negative terminal to J15 (GND\_SNS).

### **Turning On the Evaluation Board**

When the power source and load are connected to the evaluation board, it can be powered for operation.

Perform the following steps to turn on the board:

1. Set the input voltage to 24 V.
2. Ensure that EN is high, and monitor the output voltage.
3. Turn on the load, check that it is drawing the proper load current, and verify that the output voltage maintains its regulation.

## MEASURING EVALUATION BOARD PERFORMANCE

### **Measuring the Switching Waveform**

To observe the switching waveform with an oscilloscope, place the oscilloscope probe tip at Test Point J11 (SW) with the probe ground at J5 (GND). Set the scope to dc with the appropriate voltage and time divisions. The switching waveform limits alternate approximately between 0 V and the input voltage.

### **Measuring Load Regulation**

Test the load regulation by observing the change in the output voltage when increasing the output load current. To minimize the voltage drop, use short low resistance wires.

### **Measuring Line Regulation**

Vary the input voltage and examine the change in the output voltage with the fixed output current.

### **Line Transient Response**

Generate a step input voltage change and observe the behavior of the output voltage using an oscilloscope.

### **Load Transient Response**

Generate a load current transient at the output and observe the output voltage response using an oscilloscope. Attach the current probe to the wire between the output and the load to capture the current transient waveform.

### **Measuring Efficiency**

The efficiency,  $\eta$ , is measured by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of voltage drop.

### **Measuring Inductor Current**

Measure the inductor current by removing one end of the inductor from its pad and connecting a current loop in series. A current probe can be connected onto this wire.

**Measuring Output Voltage Ripple**

To observe the output voltage ripple, place the oscilloscope probe across the output capacitor with the probe ground lead connected to the negative (-) capacitor terminal and the probe tip placed at the positive (+) capacitor terminal. Set the oscilloscope to ac, 10 mV/division, 2 μs/division time base, and 20 MHz bandwidth.

A standard oscilloscope probe has a long wire ground clip. For high frequency measurements, this ground clip picks up high frequency noise and injects it into the measured output ripple. Figure 2 shows an easy way to measure the output ripple properly. Remove the oscilloscope probe sheath and wrap an unshielded wire around the oscilloscope probe. By keeping the ground length of the oscilloscope probe as short as possible, the true ripple can be measured.

**MODIFYING THE BOARD**

To modify the ADP2443 evaluation board configuration, unsolder, replace, or remove the appropriate passive components or jumpers on the board.

**Changing the Output Voltages**

The output voltage of the ADP2443-EVALZ evaluation board is preset to 5 V and the output voltage can be changed by replacing the feedback resistors, R5 and R7, with the resistor values shown in Table 1.

**Table 1. Resistive Divider for Various Output Voltages**

V <sub>OUT</sub> (V)	R7, ±1% (kΩ)	R5, ±1% (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	47.5	15
3.3	10	2.21
5.0	22	3

To limit the output voltage accuracy degradation due to the FB pin bias current (0.1 μA maximum) to less than 0.5% (maximum), ensure that the bottom divider string resistor, R5, is less than 30 kΩ.

The value of the top resistor, R7, is calculated using the following equation:

$$R7 = R5 \times \left( \frac{V_{OUT} - 0.6 \text{ V}}{0.6 \text{ V}} \right)$$

When the output voltage is changed, the values of the inductor (L1), the ramp resistor (R10), the output capacitors (C9, C10, and C11), and the compensation components (R6, C3, and C2) must be recalculated and changed to ensure stable operation (see the ADP2443 data sheet for details on external component selection).

**Changing the Switching Frequency**

The switching frequency (f<sub>sw</sub>) of the ADP2443-EVALZ evaluation board is preset to 600 kHz and the switching frequency setpoint can be changed by replacing the R4 resistor with a different value, as shown in the following equation:

$$f_{sw} \text{ (kHz)} = 168,000/R4 \text{ (k}\Omega\text{)}$$

A 560 kΩ resistor sets the frequency to 300 kHz, and a 280 kΩ resistor sets the frequency to 600 kHz.

When the switching frequency is changed, the values of the inductor (L1), the ramp resistor (R10), the output capacitors (C9, C10, and C11), and the compensation networks (R6, C3, and C2) must be recalculated and changed for stable operation (see the ADP2443 data sheet for details on external component selection).

**Changing the Soft Start Time**

The soft start time of the ADP2443 on the evaluation board is programmed to 3.8 ms.

To change the soft start time, t<sub>ss</sub>, replace the C1 capacitor value using the following equation:

$$C1 \text{ (nF)} = 5.83 \times t_{ss} \text{ (ms)}$$

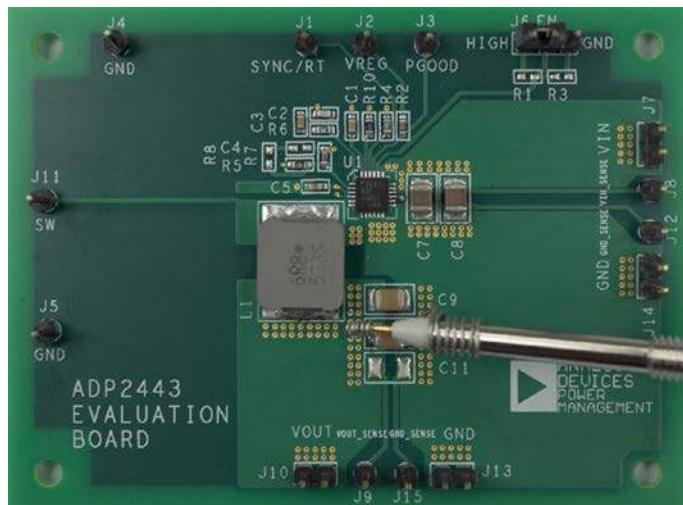


Figure 2. Measuring Output Voltage Ripple

**External Synchronization**

To synchronize the regulator to an external clock signal, apply an external clock signal to J1 (SYNC/RT) of the evaluation board.

The clock signal must have a logic high level from 1.3 V to 5 V and a logic low level below 0.4 V. Set the external clock pulse width to more than 100 ns and the frequency range between 200 kHz and 1.8 MHz.

During synchronization, the regulator operates in CCM mode and the rising edge of the switching waveform runs 180° out of phase to the external clock rising edge.

For reliable synchronization, connect a resistor (R4) from the RT/SYNC pin to GND to program the internal oscillator to run at 80% to 120% of the external synchronization clock signal.

# EVALUATION BOARD SCHEMATIC AND ARTWORK

## SCHEMATIC

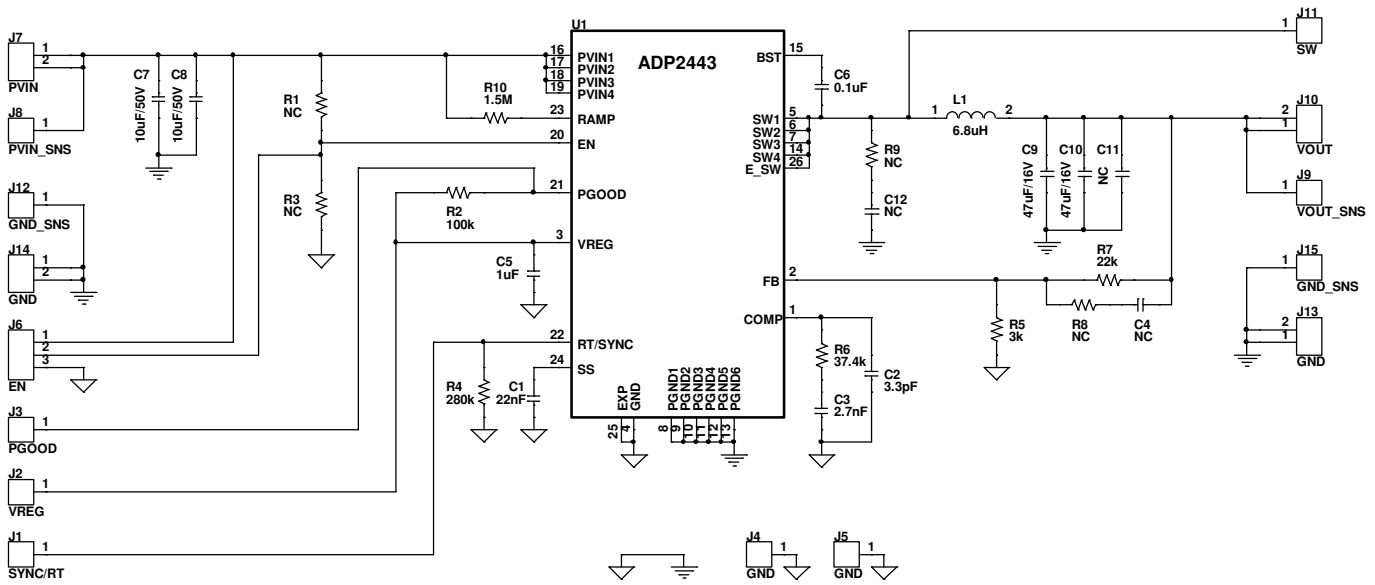


Figure 3. Evaluation Board Schematic for the [ADP2443-EVALZ](#)

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PCB LAYOUT

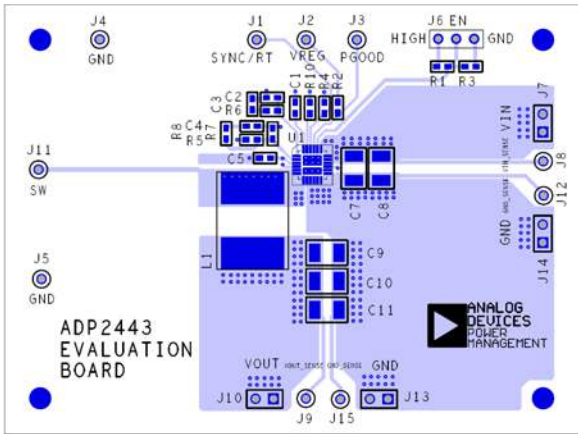


Figure 4. Layer 1, Component Side

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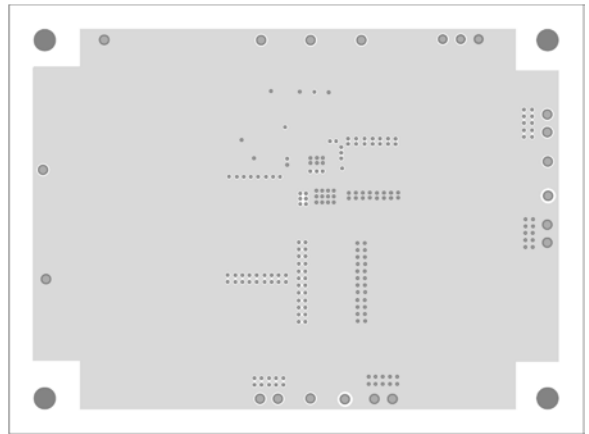


Figure 6. Layer 2, Ground Plane

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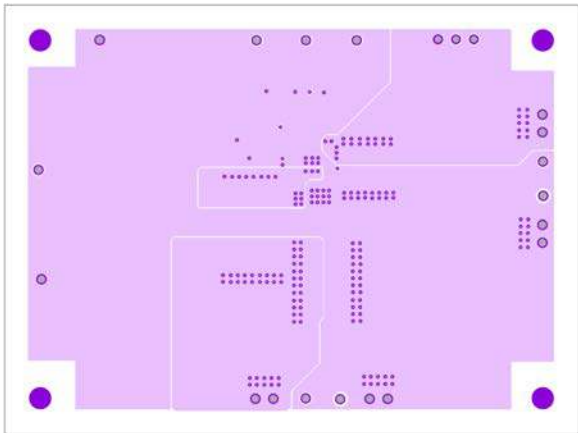


Figure 5. Layer 3, Power Plane

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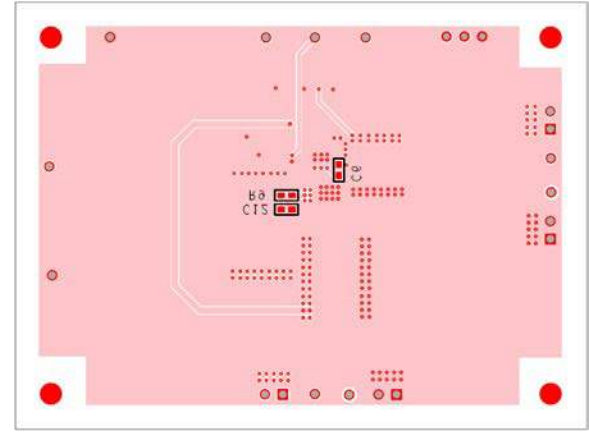


Figure 7. Layer 4, Bottom Side

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**ORDERING INFORMATION****BILL OF MATERIALS**Table 2. Bill of Materials for [ADP2443-EVALZ](#)

Qty	Reference Designator	Description	Part Number/Vendor
1	C1	Capacitor, 22 nF, 16 V, 0603	GRM188R71C223KA01D/Murata
1	C2	Capacitor, 3.3 pF, 50 V, 0603	GRM1885C1H3R3CZ01D/Murata
1	C3	Capacitor, 2700 pF, 50 V, 0603	GRM188R71H272KA01D/Murata
2	C4, C12	Optional capacitor, 0603	Optional/Murata
1	C5	Capacitor, 1 μF, 16 V, 0603	GRM188R61C105KA93D/Murata
1	C6	Capacitor, 0.1 μF, 16 V, 0603	GRM188R71C104KA01D/Murata
2	C7, C8	Capacitor, 10 μF, 50 V, 1210	GRM32ER71H106KA12L/Murata
2	C9, C10	Capacitor, 47 μF, 16 V, 1210	GRM32ER61C476KE15K/Murata
1	C11	Optional capacitor, 1210	Optional/Murata
1	L1 <sup>1</sup>	Inductor, FDVE1040, L = 6.8 μH, IRAT = 7.1 A, DCR = 18.4 mΩ	FDVE1040-6R8M/Toko
4	R1, R3, R8, R9	Optional resistor, 0603	Optional/Vishay Dale
1	R2	Resistor, 100 kΩ, 1%, 0603	CRCW0603100KFKEA/Vishay Dale
1	R4	Resistor, 280 kΩ, 1%, 0603	CRCW0603280KFKEA/Vishay Dale
1	R5	Resistor, 3 kΩ, 1%, 0603	CRCW06033K00FKEA/Vishay Dale
1	R6	Resistor, 37.4 kΩ, 1%, 0603	CRCW060337K4FKEA/Vishay Dale
1	R7	Resistor, 22 kΩ, 1%, 0603	CRCW060322K0FKEA/Vishay Dale
1	R10	Resistor, 1.5 MΩ, 1%, 0603	CRCW06031M50FKEA/Vishay Dale
1	U1	36 V, 3 A, synchronous, step-down regulator, 24-lead, LFCSP, with exposed pad	<a href="#">ADP2443</a> /Analog Devices, Inc.
10	J1, J2, J3, J4, J5, J8, J9, J11, J12, J15	Test point, 2.54 mm pitch single inline (SIL) vertical PC tail pin header, 6.1 mm mating pin height, tin, single inline package (SIP1)	M20-9990245/Harwin
4	J7, J10, J13, J14	Connector, 2.54 mm pitch SIL vertical PC tail pin header, 6.1 mm mating pin height, tin, 2-way, SIP2	M20-9990245/Harwin
1	J6	Jumper, 0.1-inch header, 3-way, SIP3	M20-9990346/Harwin

<sup>1</sup> IRAT is the saturation current of the inductor. DCR is the dc resistance of the inductor.



## NOTES



### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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