EVANS A Quantic Company	Product Specification **3THP4050303** **CAPACITOR MODULE**	NUMBER	3THP4050303
		ISSUE	01
		REVISION	A
		DATE	11/9/21

1.0 Scope

This document contains specific electrical, mechanical, and environmental requirements and specifications for the 3THP4050303 Hybrid® capacitor bank.

2.0 Construction

2.1 General

The three internal capacitors of the capacitor bank shall utilize sintered tantalum anodes and ruthenium oxide coated cathodes operating in aqueous electrolyte. The components shall be hermetically sealed in a welded tantalum case with a glass-to-metal anode terminal seal. The capacitors are potted in an aluminum housing with a screw-attached cover.

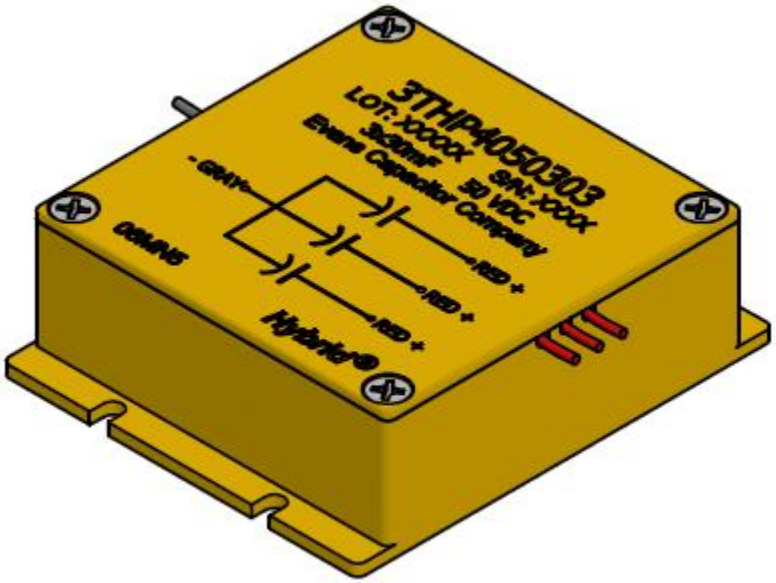
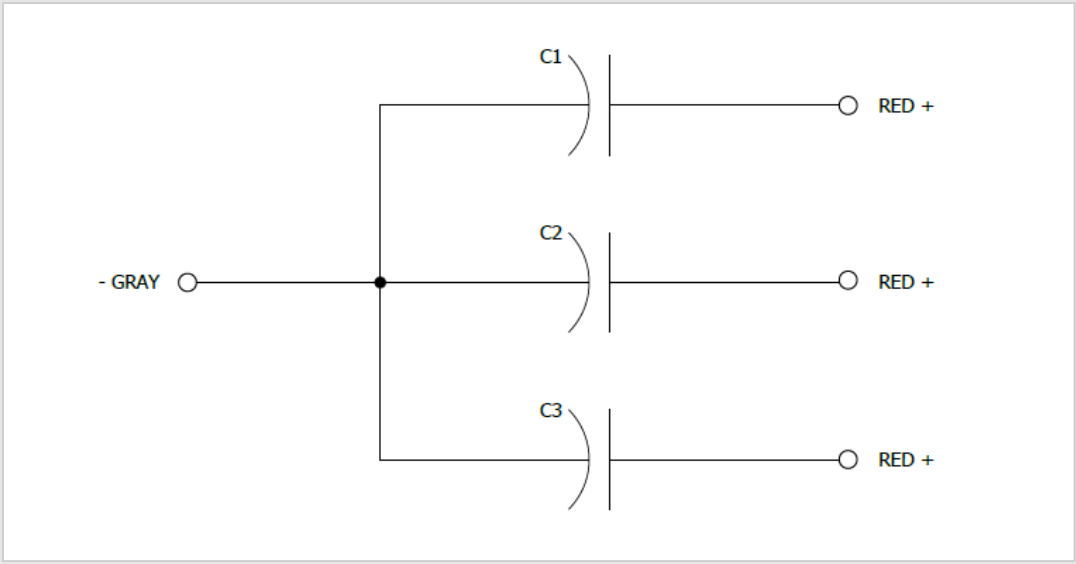


Figure 1: Isometric View



C1-C3 ARE ECC P/N: THQ4050303

Figure 2: C3P050303 capacitor bank schematic

2.2 Package

The configuration and dimensions shall be as per Figure 3.

2.3 Mass

700 grams (Typical).

2.4 Hermetic Seal

The capacitor bank shall use hermetically sealed capacitors such that the case does not leak electrolyte or vent any gas when exposed to a vacuum, per MIL-STD- 202, Method 112, Condition C, Procedure IIIa.

2.5 Part Markings

The capacitor bank shall be permanently and legibly laser engraved on the cover of the case per Figure 4. The markings shall be resistant to solvents per MIL-STD-202, Method 215J.

2.6 Solderability

The terminations shall be solderable per ANSI J-STD-002.

2.7 Resistance to Soldering Heat

The capacitor bank must withstand solder dipping of the leads at 260°C for 10 seconds per MIL-STD-202, Method 210, Condition B. The capacitor assembly must not be visibly damaged, and the electrical characteristics must not be affected.

2.8 Terminal Strength

The capacitor bank leads must withstand a 5-pound pull test for 30 seconds per Mil-Std-202, Method 211, Condition A. The capacitor bank must not be visibly damaged, and the electrical characteristics must not be affected.

2.9 Fungus Resistance

The capacitor bank materials shall not support fungus growth and shall not be a nutrient to fungus.

3.0 Environmental Requirements

3.1 Operating Temperature

–55°C to +85°C

3.2 Storage Temperature

-62°C to +130°C

3.3 Environmental Testing

The capacitor bank shall be designed to withstand environmental testing in accordance with Table 1. During testing the capacitor bank case shall be rigidly clamped to the test fixture with the leads restrained. The capacitor must not be visibly damaged, and the electrical characteristics must remain within specification.

Table 1 – Environmental Testing

	TEST	TEST METHOD	CONDITION	REMARKS
1	SHOCK	MIL-STD-202 METHOD 213	G	11 mS, 50g
2	VIBRATION	MIL-STD-202 METHOD 204	D	12 Sweeps/Axis, 20g peak
3	VIBRATION	MIL-STD-202 METHOD 214	I, Letter D	1.5 Hours/Axis, 12g rms
4	MOISTURE RESIS.	MIL-STD-202 METHOD 106		6 V Polarity
5	THERMAL SHOCK	MIL-STD-202 METHOD 107	A	
6	ALTITUDE	MIL-STD-202 METHOD 105	D	100 000 ft test

4.0 Electrical Requirements

4.1 Capacitance

The capacitance values are listed in Table 2 at 120 Hz and 25°C.

4.2 Working Voltage

The working voltage ratings are listed in Table 2.

4.3 Surge Voltage

The test shall be 1000 cycles at 110% of rated voltage at 85°C. Each cycle shall consist of a 30 second surge voltage application followed by a 330 second discharge period. The part shall be charged and discharged through a 1000-ohm resistor. The capacitor bank must not be visibly damaged, and the electrical characteristics must remain within specification.

4.4 Equivalent Series Resistance

The maximum equivalent series resistance (ESR) is listed in Table 2. at 1 kHz and 25°C. Measured at lead ends

4.5 Maximum Discharge Current

The capacitor bank shall be capable of non-repetitive discharges into a “zero ohm” short without damage.

Table 2 – Electrical Specifications

Output	Rated (VDC) 85°C	Rated (VDC) 125°C	Capacitance (±20%)	DCL (max)	ESR (typ.)
C1	50	30	30,000 µF	400 µA	35 mΩ
C2	50	30	30,000 µF	400 µA	35 mΩ
C3	50	30	30,000 µF	400 µA	35 mΩ

FINAL ESR IS A COMBINATION OF CAPACITOR ESR (<25MΩ), PCB (< 7MΩ), AND WIRE (<4 MΩ)

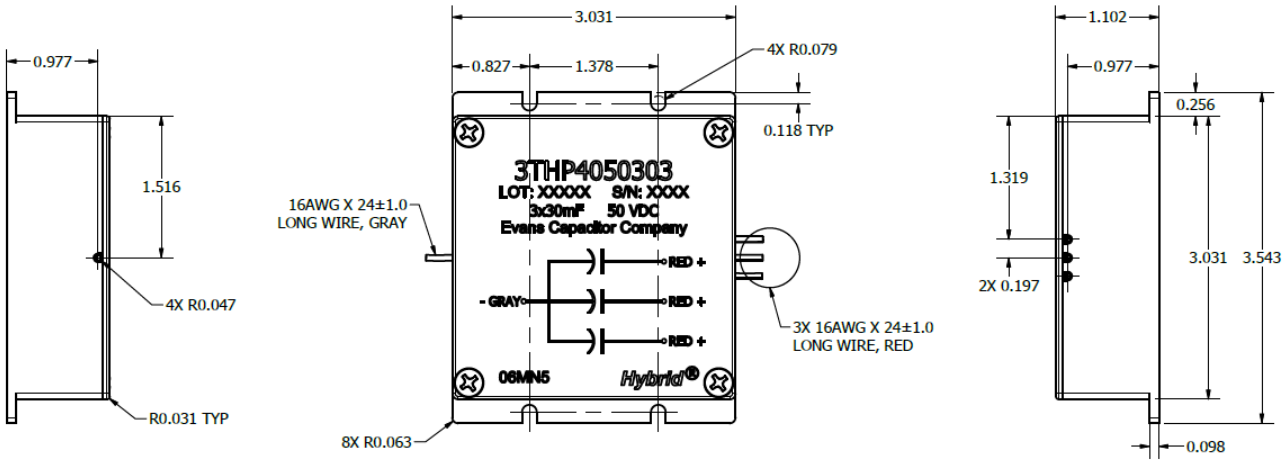
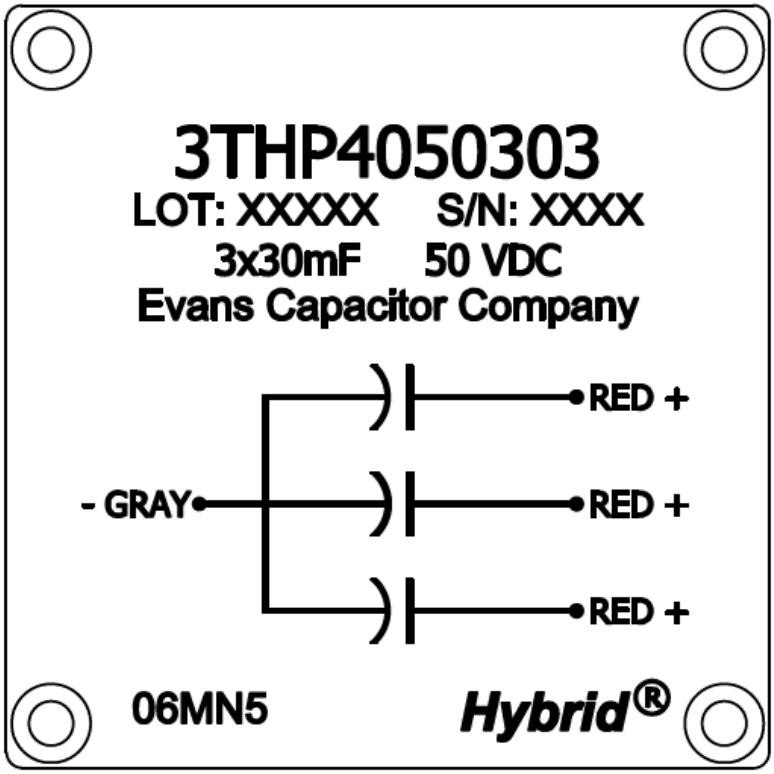


Figure 3: Part Sketch



THE PART MARKINGS SHALL BE LASER ENGRAVED

Figure 4: Part Marking