Low Voltage SPDT Analog Switch 2:1 Mux/Demux Bus Switch

Description

The DIODES PI5A3157B is a high-bandwidth, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, 1.65V to 5.5V, the PI5A3157B has a maximum ON resistance of 12Ω at 1.65V, 9Ω at 2.3V & 6Ω at 4.5V.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

The control input, S, is independent of supply voltage.

PI5A3157B is an improved direct replacement for the NC7SB3157.

Application(s)

- Cell Phones
- PDAs
- MP3 Players
- Portable Instrumentation
- Battery Powered Communications
- Computer Peripherals

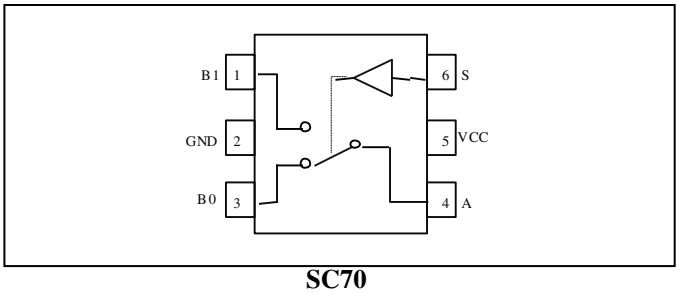
Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 8Ω at 3.0V
- Wide VCC Range: 1.65V to 5.5V
- Rail-to-Rail Signal Range
- Control Input Overvoltage Tolerance: 5.5V
- Fast Transition Speed: 2ns at 5.0V
- High Off Isolation: -63dB @ 10MHz
- Break-Before-Make Switching
- High Bandwidth: 350MHz
- Extended Industrial Temperature Range: -40°C to 85°C
- The PI5A3157B is an improved direct replacement for the NC7SB3157
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 6-pin, X1DFN 1mm×1mm (XDB)
  - 6-pin, SC70 (C6) (Not Recommended for New Design)
  - 6-Pin, SC70 (C)

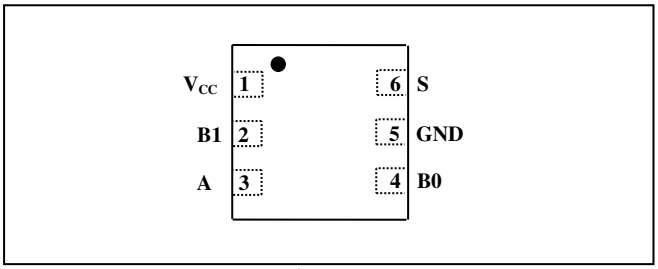
Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration

Top Transparent View



SC70



X1DFN

Pin Description

Pin#		Pin Name	Description
SC70	X1DFN		
1	2	B1	Data Port
2	5	GND	Ground
3	4	B0	Data Port (Normally connected)
4	3	A	Common Output/Data Port
5	1	V_{CC}	Positive Power Supply
6	6	S	Logic Control

Logic Function Table

Logic Inputs(S)	Function
0	B_0 connect to A
1	B_1 connect to A

Maximum Ratings

Storage Temperature.....-65°C to +150°C
Ambient Temperature with Power Applied.....-40°C to +85°C
Supply Voltage V_{CC} .....-0.5V to +7.0V
DC Control Input Voltage V_S .....-0.5V to +7.0V
DC Input Voltage V_{IN} .....-0.5V to V_{CC} +0.5V
DC Output Current V_{OUT}.....128mA
DC V_{CC} or Ground Current I_{CC} /I_{GND} .....±100mA
Maximum Junction Temperature.....125°C
Junction Lead Temperature (T_L)
(Soldering, 10 seconds) ..... 260°C
Power Dissipation (P_D) @ +85°C 180mW
ESD(HBM)..... 2000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	1.65	-	5.5	V
V_S	Control Input Voltage	-	0	-	5.5	V
V_{IN}	Switch Input Voltage	-	0	-	V_{CC}	V
V_{OUT}	Output Voltage	-	0	-	V_{CC}	V
T_A	Operating Temperature	-	-40	25	85	°C
Ts						
tr, tf	Input Rise and Fall Time	Control Input V_{CC} = 2.3V to 3.6V	0	-	10	ns/V
		Control Input V_{CC} = 4.5V to 5.5V	0	-	5	ns/V

Note: Control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

(T_A = –40°C to 85°C, unless otherwise noted.)

Parameter	Description	Test Conditions	Temperature (T_A:°C)	Min.	Typ.	Max.	Units
V_{IAR}	Analog Input Signal Range	V_{CC}	-40°C to 85°C	0	-	V_{CC}	V
R_{ON}	ON Resistance(1)	V_{CC}=4.5V, I_O = 30mA, V_{IN} = 0V	25°C	-	4	6	Ω
		V_{CC}=4.5V, I_O=-30mA, V_{IN} =2.4V		-	5	8	
		V_{CC}=4.5V, I_O =-30mA, V_{IN} =4.5V		-	7	11	
		V_{CC}=4.5V, I_O =30mA, V_{IN} = 0V	-40°C to 85°C	-	-	6	
		V_{CC}=4.5V, I_O =-30mA, V_{IN} =2.4V		-	-	8	
		V_{CC}=4.5V, I_O =-30mA, V_{IN} =4.5V		-	-	11	
		V_{CC}=3.0V, I_O =24mA, V_{IN} =0V	25°C	-	5	8	
		V_{CC}=3.0V, I_O =-24mA, V_{IN} =3.0V		-	10	15	
		V_{CC}=3.0V, I_O =24mA, V_{IN} =0V	-40°C to 85°C	-	-	8	
		V_{CC}=3.0V, I_O=-24mA, V_{IN} =3.0V		-	-	15	
		V_{CC}=2.3V, I_O =8mA, V_{IN} =0V	25°C	-	6	9	
		V_{CC}=2.3V, I_O =-8mA, V_{IN} =2.3V		-	13	20	
		V_{CC}=2.3V, I_O =8mA, V_{IN} =0V	-40°C to 85°C	-	-	9	
		V_{CC}=2.3V, I_O=-8mA, V_{IN} =2.3V		-	-	20	
		V_{CC}=1.65V, I_O =4mA, V_{IN} =0V	25°C	-	8	12	
		V_{CC}=1.65V, I_O=-4mA, V_{IN}=1.65V		-	20	30	
		V_{CC}=1.65V, I_O =4mA, V_{IN} = 0V	-40°C to 85°C	-	-	12	
		V_{CC}=1.65V, I_O=-4mA, V_{IN}=1.65V		-	-	30	

Parameter	Description	Test Conditions	Temperature (T_A:°C)	Min.	Typ.	Max.	Units
ΔR_{ON}	ON Resistance Match Between Channels(1,2,3)	V_{CC}=4.5V, I_A=-30mA, V_{IN}=3.15V	25°C	-	0.15	-	Ω
		V_{CC}=3.0V, I_A=-24mA, V_{IN} =2.1V		-	0.2	-	
		V_{CC}=2.3V, I_A =-8mA, V_{IN} =1.6V		-	0.3	-	
		V_{CC}=1.65V, I_A=-4mA, V_{IN}=0V		-	0.5	-	
R_{ONF}	ON Resistance Flatness(1,2,4)	V_{CC}=5.0V, I_A =-30mA, 0≤ V_{IN}≤V_{CC}	25°C	-	6	-	Ω
		V_{CC}=3.3V, I_A =-24mA, 0≤V_{IN}≤V_{CC}		-	12	-	
		V_{CC}=2.5V, I_A =-8mA, 0≤ V_{IN}≤V_{CC}		-	22	-	
		V_{CC}=1.8V, I_A =-4mA, 0≤ V_{IN}≤V_{CC}		-	90	-	
V_{IH}	Input High Voltage (Logic High Level)	V_{CC}=1.65V	-40°C to 85°C	1	-	-	V
		V_{CC} = 2.3V		1.2	-	-	
		V_{CC} = 3V		1.3	-	-	
		V_{CC} = 4.2V		1.5	-	-	
		V_{CC} = 5.5V		1.8	-	-	
V_{IL}	Input Low Voltage (Logic Low Level)	V_{CC}=1.65V	-40°C to 85°C	-	-	0.4	V
		V_{CC} = 2.3V		-	-	0.6	
		V_{CC} = 3V		-	-	0.8	
		V_{CC} = 4.2V		-	-	1	
		V_{CC} = 5.5V		-	-	1.2	
I_{LKC}	Input Leakage Current	0≤V_{IN}≤5.5V, V_{CC}=0V to 5.5V	25°C	-	-	±0.1	µA
			-40°C to 85°C	-	-	±1.0	
I_{OFF}	OFF State Leakage Current	0≤V_{IN}≤5.5V, V_{CC}=1.65V to 5.5V	25°C	-	-	±0.1	µA
			-40°C to 85°C	-	-	±10	
I_{CC}	Quiescent Supply Current	All channels ON or OFF, V_{IN} = V_{CC} or GND, I_{OUT}=0, V_{CC} = 5.5V	25°C	-	-	1	µA
			-40°C to 85°C	-	-	5	

Notes:
1. Measured by voltage drop between A and B pins at the indicated current through the device. ON resistance is determined by the lower of the voltages on two ports (A or B).
2. Parameter is characterized but not tested in production.
3. DR_{ON} = R_{ON} max – R_{ON} min. measured at identical V_{CC}, temperature and voltage levels.
4. Flatness is defined as difference between maximum and minimum value of ON resistance over the specified range of conditions. Guaranteed by design.

Capacitance

(T_A = 25°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Control Input	V_{CC} = 5.0V, f =1 MHz(1)	-	2.5	-	pF
C_{IO-B}	For B Port, Switch OFF		-	5.0	-	
C_{IOA-ON}	For A Port, Switch ON		-	15.0	-	

Notes:
1. Capacitance is characterized but not tested in production

Switch and AC Characteristics

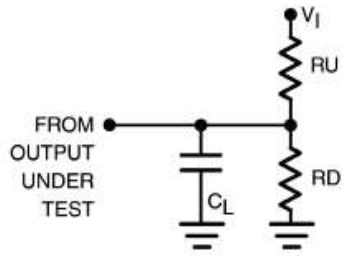
Parameter	Description	Test Conditions	Supply Voltage	Temperature (T_A: °C)	Min	Typ	Max	Units
t_{PLH} t_{PHL}	Propagation Delay: A to Bn	See test circuit diagrams 1 and 2. V_I Open(2)	V_{CC} =1.65V to 1.95V	–40 to 85°C	-	-	3.5	ns
			V_{CC} =2.3V to 2.7V		-	-	1.1	
			V_{CC} =3.0V to 3.6V		-	-	0.9	
			V_{CC} =4.5V to 5.5V		-	-	0.6	
t_{PZL} t_{PZH}	Output Enable Turn ON Time: A to Bn	See test circuit diagrams 1&2. V_I = 2V_{CC} for t_{PZL},	V_{CC} =1.65V to 1.95V	–40 to 85°C	6	-	13	
			V_{CC} =2.3V to 2.7V		3.5	-	8.0	
			V_{CC} =3.0V to 3.6V		2.5	-	6.9	

Parameter	Description	Test Conditions	Supply Voltage	Temperature (T_A: °C)	Min	Typ	Max	Units
		V_I = 0V for t_{PZH}	V_{CC} =4.5V to 5.5V		1.7	-	5.2	
t_{PLZ} t_{PHZ}	Output Disable Turn OFF Time: A to Bn	See test circuit diagrams 1 and 2. V_I= 2V_{CC} for t_{PLZ}, V_I = 0V for t_{PHZ}	V_{CC} =1.65V to 1.95V	–40 to 85°C	3	-	13	
			V_{CC} =2.3V to 2.7V		2	-	9	
			V_{CC} =3.0V to 3.6V		1.5	-	7.0	
			V_{CC} =4.5V to 5.5V		0.8	-	4.5	
t_{BM}	Break Before Make Time	See test circuit diagram 3.	V_{CC} =1.65V to 1.95V	–40 to 85°C	-	3.7	-	
			V_{CC} =2.3V to 2.7V		-	2.5	-	
			V_{CC} =3.0V to 3.6V		-	2.5	-	
			V_{CC} =4.5V to 5.5V		-	1.6	-	
Q	Charge Injection	C_L = 0.1nF, V_{GEN} = 0V, R_{GEN}=0Ω. See test circuit 4.	V_{CC} = 5.0V	25°C	-	10	-	pC
			V_{CC} = 3.3V		-	6	-	
OIRR	Off Isolation	R_L=50Ω, V_{GEN}=0V, R_{GEN} =0Ω, f =10MHz. See test circuit 5(3)	V_{CC} =1.65V to 5.5V	25°C	-	-63	-	dB
X_{TALK}	Crosstalk Isolation	See test circuit 6(4)	V_{CC} =1.65V to 5.5V	25°C	-	-64	-	
f_{3dB}	–3dB Bandwidth	See test circuit 9	V_{CC} =1.65V to 5.5V	25°C	-	350	-	MHz
T_{HD}	Total Harmonic Distortion	R_L=600Ω, V_{IN}=0.5Vpp, f=20Hz to 20kHz	V_{CC} = 5.0V	25°C	-	0.012	-	%

Notes:

1. Guaranteed by design.
2. The device contributes no other propagation delay other than the RC delay of the switch ON resistance and the 50pF load capacitance, when driven by an ideal voltage source with zero output impedance.
3. Off Isolation = 20 Log_{10} [V_{Bn}/V_A] and is measured in dB.
4. Crosstalk Isolation = 20 Log_{10} [V_{B1}/V_{B0}] and is measured in dB.

Test Circuits and Timing Diagrams



Note: Input driven by 50ohm source terminated in 500ohm
Note: C_L Includes load and stray capacitance
Note: Input PRR=1.0MHz, t_W=500nS

Figure 1. AC Test Circuit

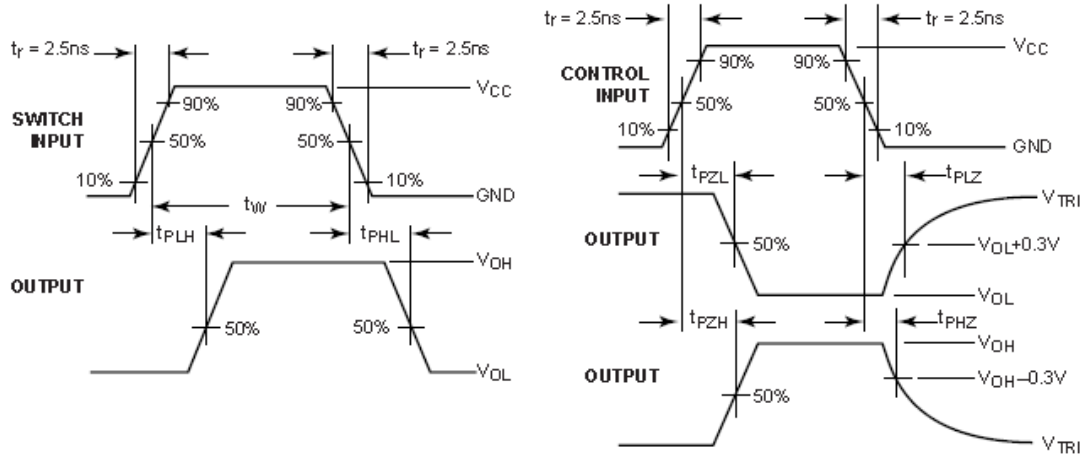


Figure 2. AC Waveforms

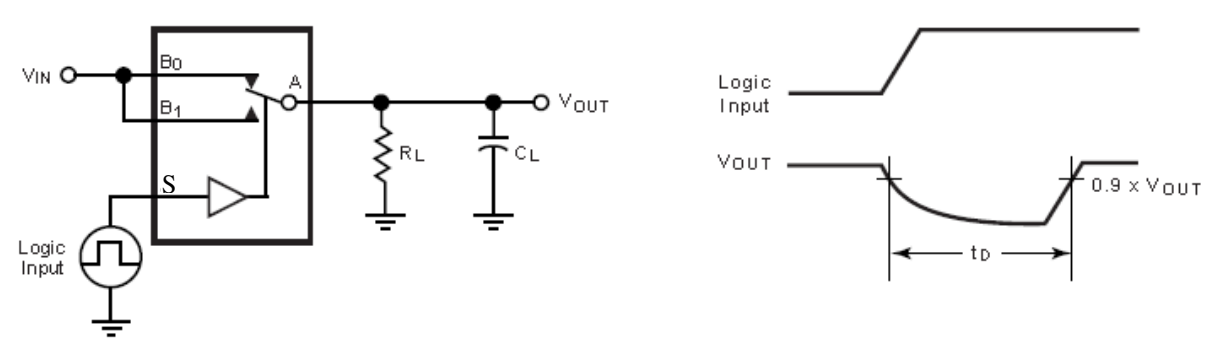


Figure 3. Break Before Make Interval Timing

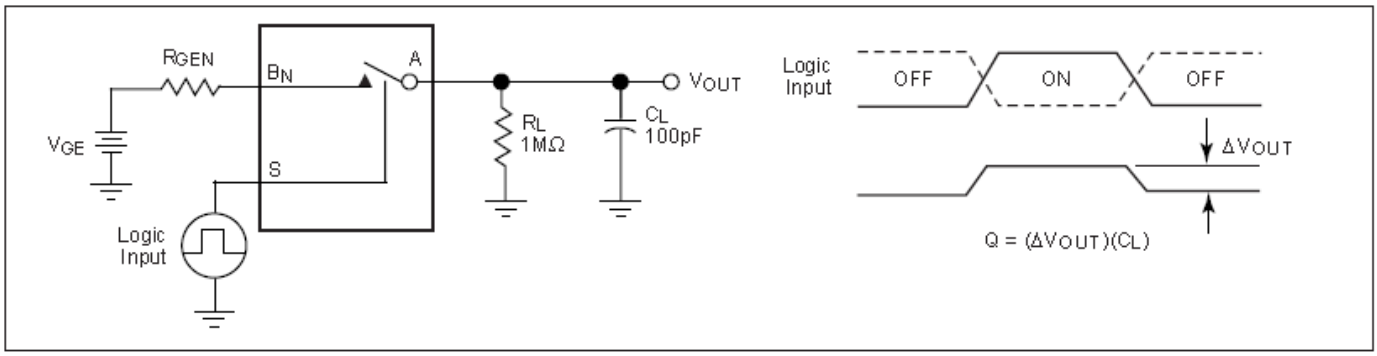


Figure 4. Charge Injection Test

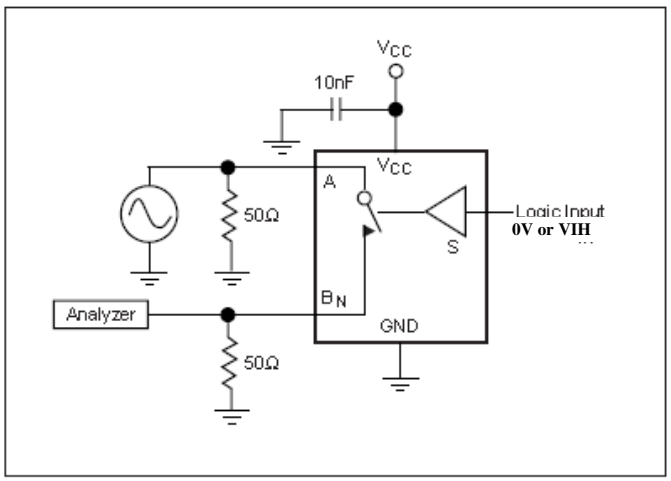


Figure 5. Off Isolation

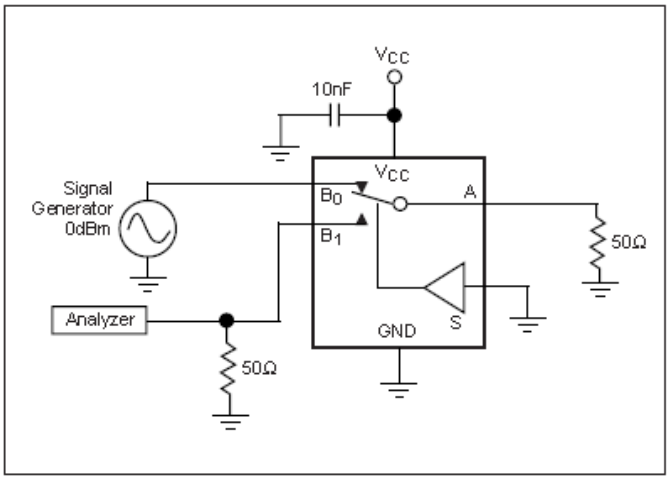


Figure 6. Crosstalk

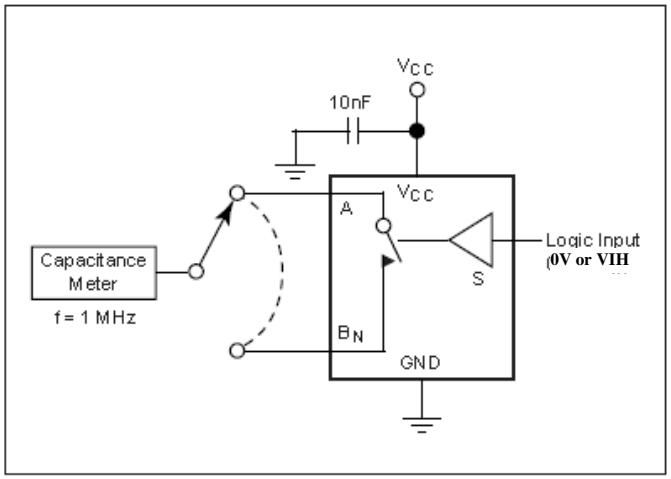


Figure 7. Channel Off Capacitance

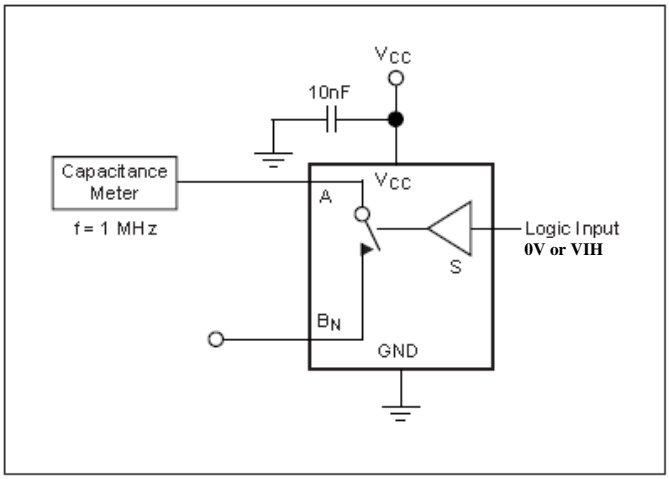


Figure 8. Channel On Capacitance

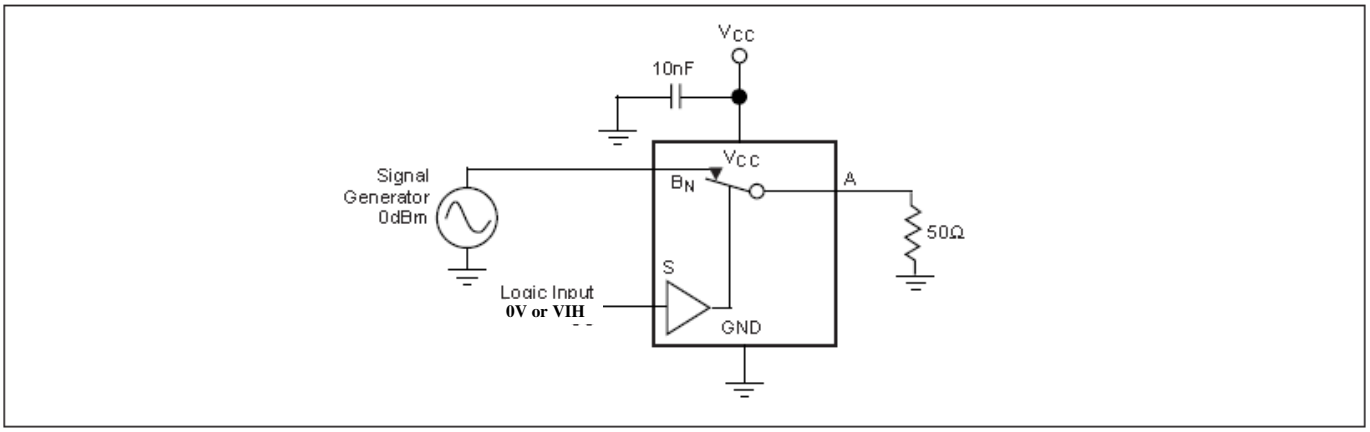
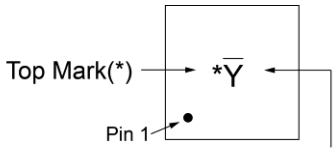


Figure 9. Bandwidth

Part Marking

XDB Package

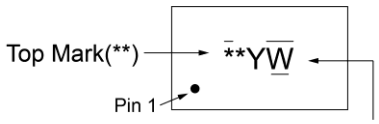


Y: One Character Shorted Date Code
Bar Above Date Code means Cu Wire

C6 Package

kD: PI5A3157BC6E
XX: Date Code (Year & Workweek)
The bar of "D" means Fab3 of Magnachip

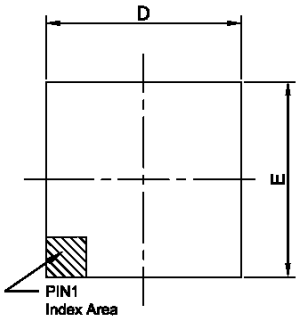
C Package



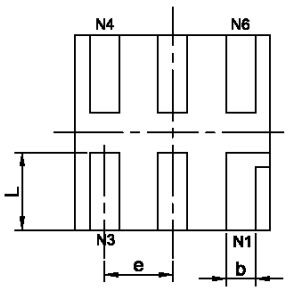
Y: Date Code (Year)
W: Date Code (Workweek)
Bar Above "W" means Cu Wire

Packaging Mechanical

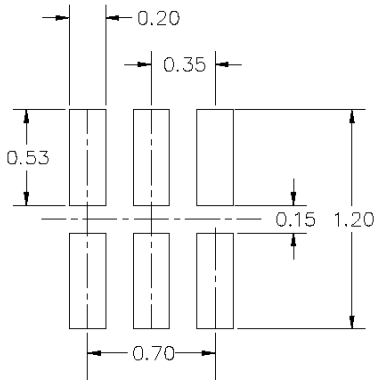
6-X1DFN (XDB)



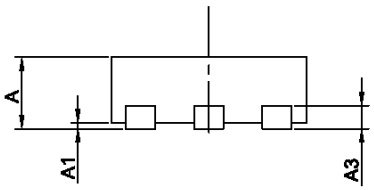
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN(Unit:mm)



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	–	0.40
A1	0.00	0.05
A3	0.13 REF	
D	0.95	1.05
E	0.95	1.05
b	0.14	0.20
L	0.35	0.45
e	0.35 BSC	

Note:
1. Ref: JEDEC MO-287A
2. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

DIODES INCORPORATED PERICOM A PRODUCT LINE OF DIODES INCORPORATED ENABLING SERIAL CONNECTIVITY

DATE: 04/28/16

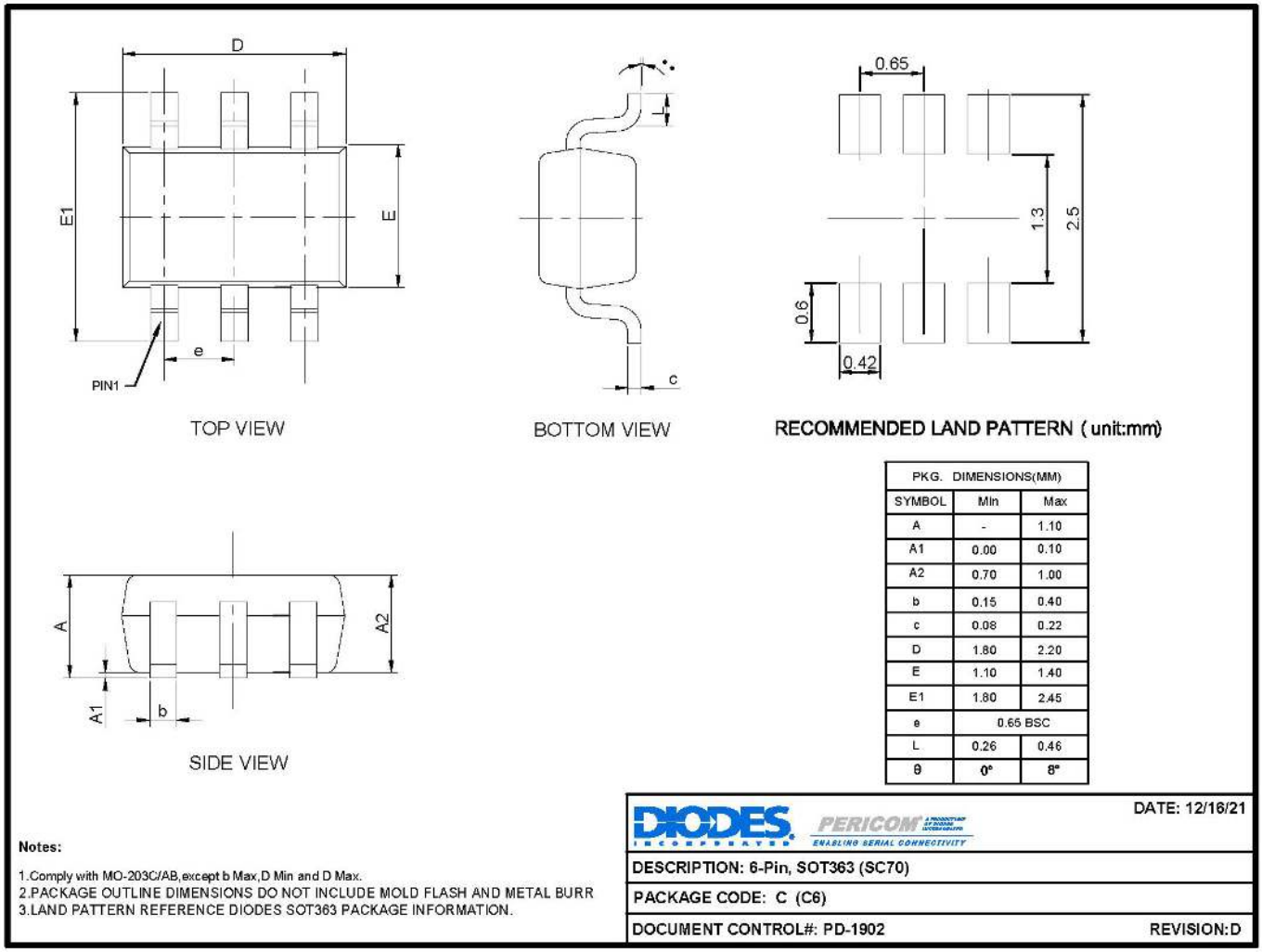
DESCRIPTION: 6-Pin, X2DFN, 1X1

PACKAGE CODE: XDB (XDB6)

DOCUMENT CONTROL #: PD2206 **REVISION: –**

16-0041

6-SC70 (C6)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	-	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.15	0.40
c	0.08	0.22
D	1.80	2.20
E	1.10	1.40
E1	1.80	2.45
e	0.65 BSC	
L	0.26	0.46
θ	0°	8°

Notes:

1.Comply with MO-203C/AB,except b Max,D Min and D Max.
2.PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR
3.LAND PATTERN REFERENCE DIODES SOT363 PACKAGE INFORMATION.

DATE: 12/16/21

DESCRIPTION: 6-Pin, SOT363 (SC70)

PACKAGE CODE: C (C6)

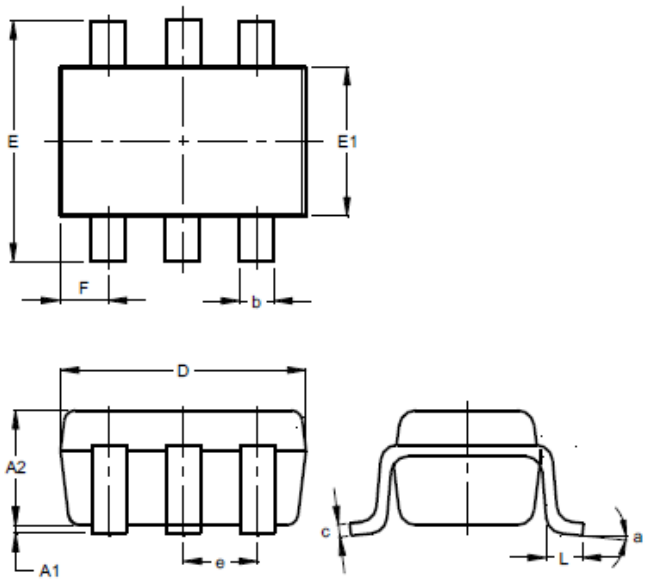
DOCUMENT CONTROL#: PD-1902 REVISION:D

21-1534

6-SC70 (C)

Package Outline Dimensions

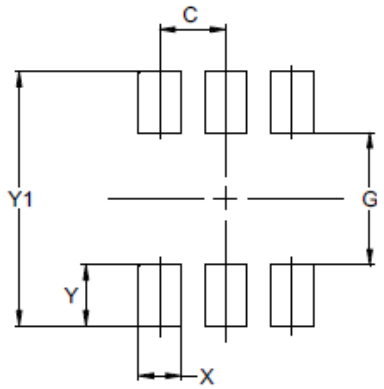
SOT363



SOT363			
Dim	Min	Max	Typ
A1	0.00	0.10	0.05
A2	0.90	1.00	0.95
b	0.10	0.30	0.25
c	0.10	0.22	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
F	0.40	0.45	0.425
L	0.25	0.40	0.30
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

SOT363



Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.420
Y	0.600
Y1	2.500

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Number	Package Code	Package Description	Top Marking
PI5A3157BXDBEX	XDB	6-Pin, 1x1 (X1DFN)	* $\overline{Y}$
PI5A3157BC6EX	C6	6-Pin, SOT363 (SC70) (Not Recommended for New Design)	$\overline{k}$ $\overline{D}$ X$\underline{X}$
PI5A3157BCEX	C	6-Pin, SOT363 (SC70)	$\overline{*}$ *Y $\overline{\underline{W}}$

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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