TEXAS INSTRUMENTS

TPS54110EVM-044 1.5-Amp

SWIFT™ Regulator Evaluation Module

User's Guide

December 2003

PMP Systems Power

SLVU102

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Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and the use of the TPS54110EVM−044 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

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Chapter 1

Introduction

This chapter contains background information for the TPS54110 with support documentation for the TPS54110EVM-044 evaluation module (HPA044). The TPS54110EVM-044 performance specifications are provided, along with a schematic and bill of material.

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1.1 Background

The TPS54110 dc/dc converter is designed to provide up to 1.5-A output from a 3-V to 6-V input voltage source. Rated input voltage and output current range is given in Table 1−1. This evaluation module is designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54110 regulator, and does not reflect the high efficiencies that may be achieved when designing with this part. The switching frequency is set at a nominal 700 kHz, allowing the use of a relatively small footprint 1-µH output inductor. The high-side and low-side MOSFETs are incorporated inside the TPS54110 package allowing for compact designs with minimal external circuitry. The low drain-to-source on resistance of the internal MOSFETs allows the TPS54110 to achieve high efficiencies and helps to keep the temperature low at high output currents. The compensation components are provided external to the IC, and allow for an adjustable output voltage and a customizable loop response. The TPS54110 is a full-featured device including undervoltage lockout, adjustable slow-start timing, adjustable switching frequency, enable, and power good functions.

Table 1−1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54110EVM−044	3 V to 6 V	0 to 1.5 A

1.2 Performance Specification Summary

A summary of the TPS54110EVM-044 performance specifications is provided in Table 1−2. Specifications are given for an input voltage of 3.3 V and an output voltage of 1.5 V unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted. The maximum input voltage for the TPS54110 is 6 V.

Table 1−2. TPS54110EVM-044 Performance Specification Summary

Specification		Test Conditions	Min	Typ	Max	Units
Input voltage range			3.0	3.3 or 5.0	6.0	V
Output voltage set point				1.5		V
Output current range		V_I = 3 V to 5.5 V	−1.5		1.5	A
Line regulation		I_O = 0−1.5 A, V_I = 3 V to 6 V		±0.02%		
Load regulation		V_I = 3.3 V, I_O = 0 A to 1.5 A		±0.08%		
Load transient response	Voltage change	I_O = 0.37 A to 1.12 A		−35		mV_{PK}
	Recovery time			120		µs
	Voltage change	I_O = 1.12 A to 0.37 A		25		mV_{PK}
	Recovery time			120		µs
Loop bandwidth		V_I = 3 V		89		kHz
Phase margin		V_I = 3 V		66		°
Loop bandwidth		V_I = 6 V		152		kHz
Phase margin		V_I = 6 V		58		°
Input ripple voltage				90	200	mV_{PP}
Output ripple voltage				25	35	mV_{PP}
Output rise time				3.5		ms
Operating frequency			680	700	720	kHz
Maximum efficiency		V_I = 3.3 V, V_O = 1.5 V, I_O = 0.6 A		78%		

1.3 Modifications

The TPS54110EVM−044 is designed to demonstrate the small size that can be attained when designing with the TPS54110; therefore, many of the features, which allow for extensive modifications, have been omitted from this EVM. For reference designators, see the schematic in Figure 4−1.

1.3.1 Output Voltage Set Point

Changing the value of R2 can change the output voltage in the range of 0.9 V to 3.3 V. The value of R2 for a specific output voltage can be calculated by using Equation 1−1. Table 1−3 list the values for R2 for some common output voltages. Note that 3.3-V output is not available with V_I less than 4 V.

Equation 1−1.

$$R2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V}$$

Table 1−3. Output Voltage Programming

Output Voltage (V)	R2 Value (Ω)
1.2	28.7 k
1.5	14.7 k
1.8	9.76 k
2.5	5.49 k
3.3	3.74 k

The minimum output voltage is limited by the minimum controllable on time of the device, 200 ns, and depends on the duty cycle and operating frequency. The approximate minimum output voltage can be calculated using Equation 1−2:

Equation 1−2.

$$V_{O(min)} = 200\ nsec \times f_S \times V_{I(max)}$$

1.3.2 Switching Frequency

The switching frequency is set to 700 kHz with R4. The switching frequency of this EVM should not be adjusted. Any lowering of the switching frequency results in increased output ripple current in the inductor L1 unless the value of L1 is increased.

1.3.3 Input Filter

An onboard electrolytic input capacitor may be added at C1.

Chapter 2

Test Setup and Results

This chapter describes how to properly connect, set up, and use the TPS54110EVM−044 evaluation module. The chapter also includes test results typical for the TPS54110EVM−044 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

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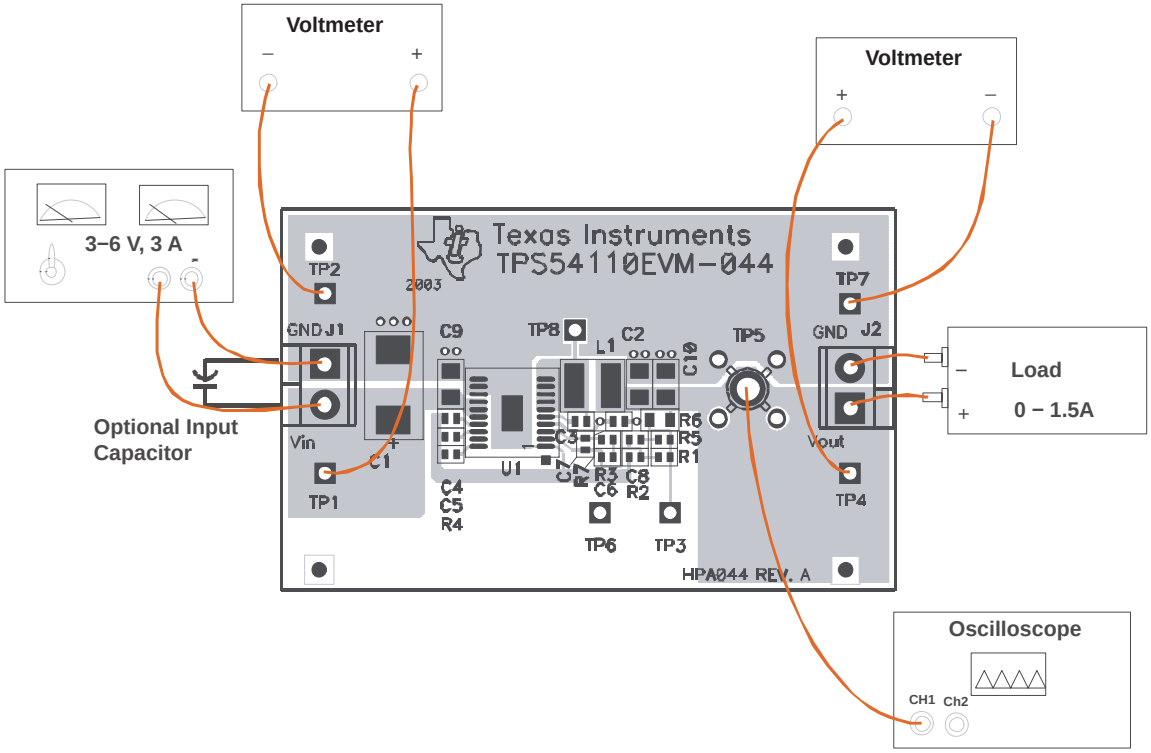
2.1 Input/Output Connections

The TPS54110EVM−44 has the following two input/output connectors: V_I (J1), and V_O (J2). A diagram showing the connection points is shown in Figure 2−1. A power supply capable of supplying 3 A should be connected to J1 through a pair of 20 awg wires. The load should be connected to J2 through a pair of 20 awg wires. The maximum load current capability should be 1.5 A. Wire lengths should be minimized to reduce losses in the wires. Test point TP5 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage. The TPS54110 is intended to be used as a point of load regulator. In typical applications, it is usually located close to the input voltage source. When using the TPS54110EVM−044 with an external power supply as the source for V_I, an additional bulk capacitor may be required, depending on the output impedance of the source and length of the hook-up wires. The test results presented are obtained using a 470-µF, 16-V additional input capacitor. Alternately, C1 can be populated with an input filter capacitor.

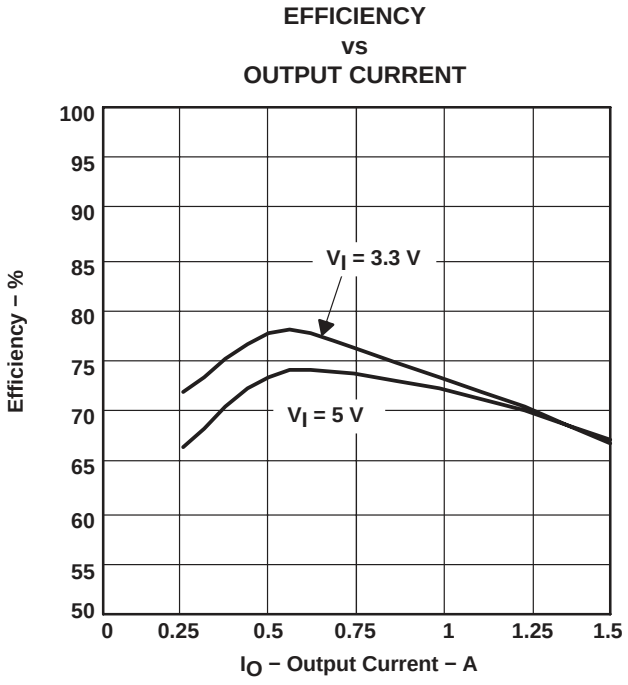
Figure 2−1. Connection Diagram



2.2 Efficiency

The TPS54110EVM−44 efficiency peaks at load current of about 0.5 A to 0.75 A, and then decreases as the load current increases towards full load. Figure 2−2 shows the efficiency for the TPS54110 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

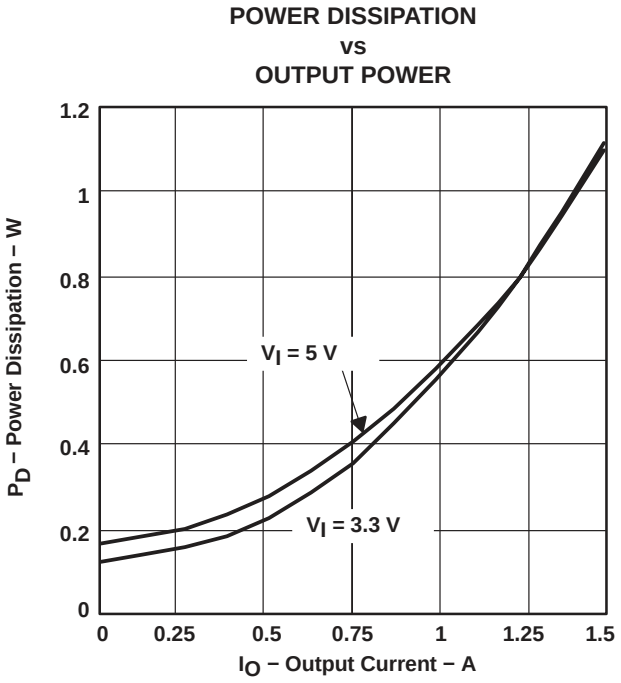
Figure 2−2. Measured Efficiency, TPS54110



2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a good board layout, allows the TPS54110EVM−044 EVMs to output full-rated load current while maintaining safe junction temperatures. With a 3.3-V input source and a 1.5-A load, the junction temperature is approximately 60°C wheras the case temperature is approximately 55°C. The total circuit losses at 25°C are shown in Figure 2−3. Power dissipation is shown for input voltages of 3.3 V, and 5 V. For additional information on the dissipation ratings of the devices, see the individual product data sheets.

Figure 2−3. Measured Circuit Losses



2.4 Output Voltage Regulation

The output voltage load regulation of the TPS54110EVM−044 is shown in Figure 2−4; the output voltage line regulation is shown in Figure 2−5. Measurements are given for an ambient temperature of 25°C.

Figure 2−4. Load Regulation

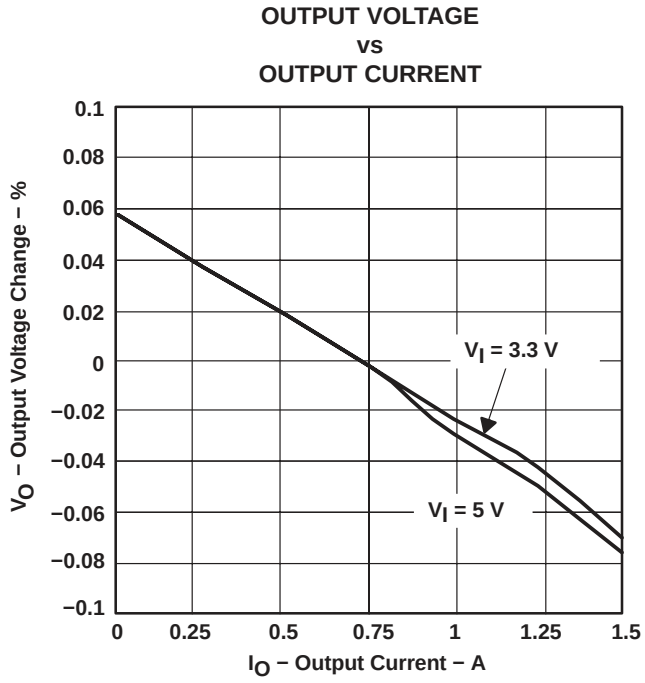
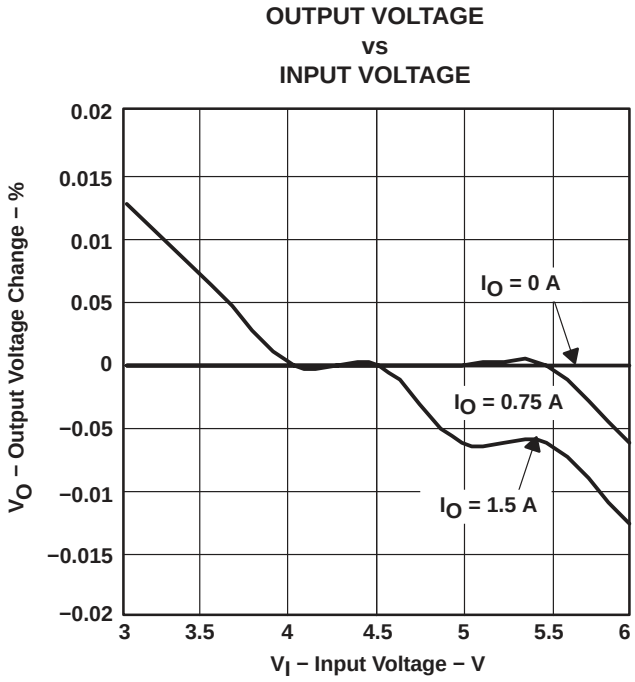


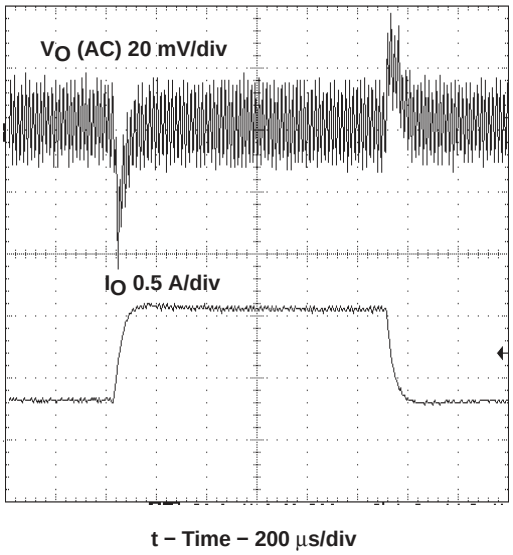
Figure 2−5. Line Regulation



2.5 Load Transients

The TPS54110EVM−044 response to load transients is shown in Figure 2−6. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2−6. Load Transient Response, TPS54110



2.6 Loop Characteristic

The TPS54110EVM−044 loop response characteristics are shown in Figure 2−7 and Figure 2−8. Gain and phase plots are shown for each device at minimum and maximum operating voltage.

Figure 2−7. Measured Loop Response, TPS54110, V_I = 3 V

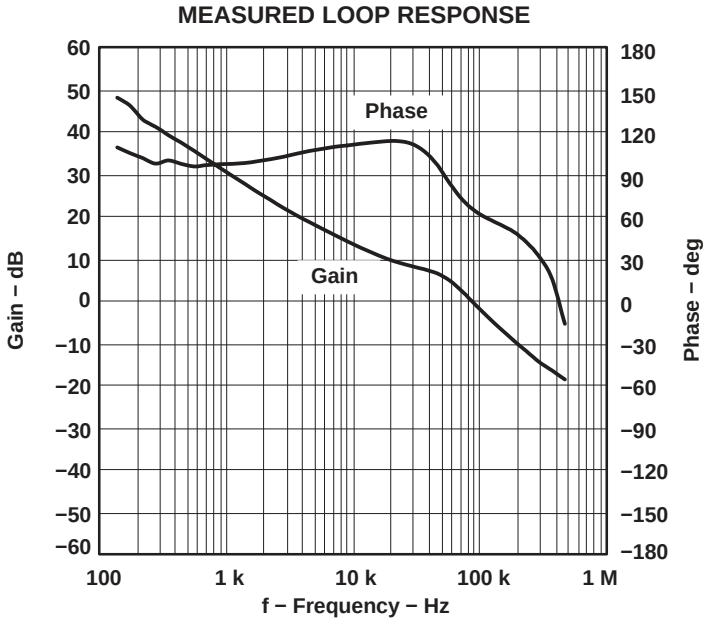
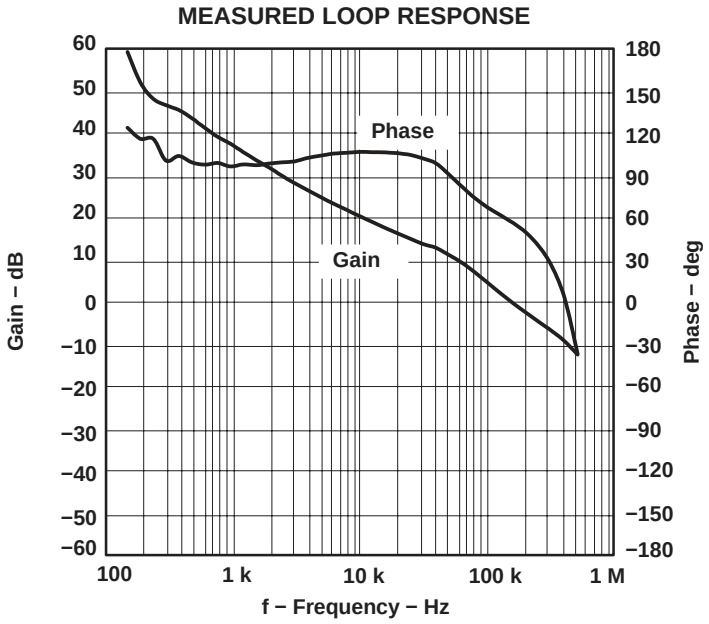


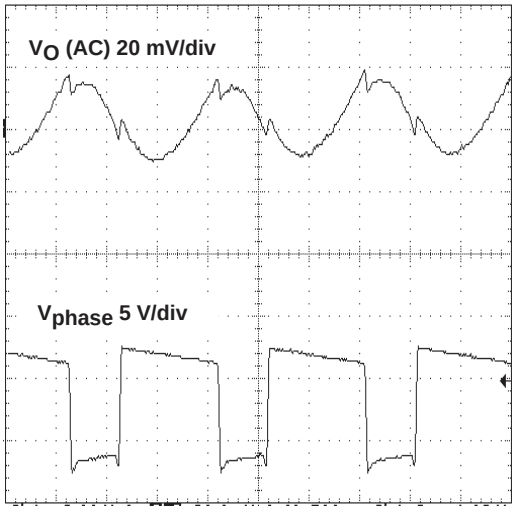
Figure 2−8. Measured Loop Response, TPS54110, V_I = 6 V



2.7 Output Voltage Ripple

The TPS54110EVM−044 output voltage ripple is shown in Figure 2−9. The input voltage is 3.3 V for the TPS54110. Output current is the rated full load of 1.5 A. Voltage is measured directly across output capacitors.

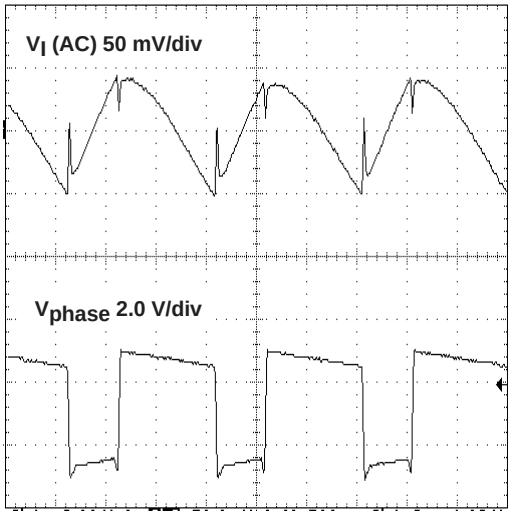
Figure 2−9. Measured Output Voltage Ripple, TPS54110



2.8 Input Voltage Ripple

The TPS54110EVM−044 input voltage ripple is shown in Figure 2−10. The input voltage is 3.3 V for the TPS54110. Output current for each device is rated full load of 1.5 A.

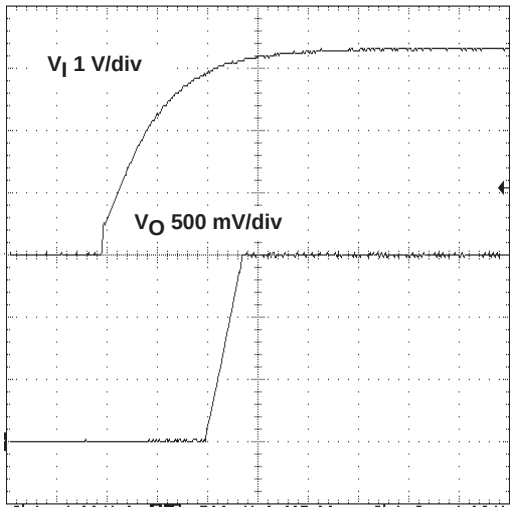
Figure 2−10. Input Voltage Ripple, TPS54110



2.9 Powering Up

The TPS54110 regulator provides an internal slow-start circuit to ramp the output voltage up at a steady rate. When the input voltage reches the UVLO start up threshold, the output begins to ramp up at the internally set rate until the final output set point is reached. The output voltage waveforms during power up do not depend on load currents. Longer delay and ramp times can be programmed using an external slow-start capacitor in the C5 location. Alternately, the SS/ENA pin can be used as an enable pin. When SS/ENA is held low, the output is disabled. Releasing the SS/ENA pin allows the output to ramp up.

Figure 2−11. Powering Up



Chapter 3

Board Layout

This chapter provides a description of the TPS54110EVM−044 board layout and layer illustrations.

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3.1 Layout

The board layout for the TPS54110EVM−044 is shown in Figure 3−1 through Figure 3−3. The top side layer of the TPS54110EVM−044 is laid out in a manner typical of a user application that is optimized for small size. A small footprint Coilcraft DO3314−103MX inductor and 0805 10-µF ceramic capacitor are used in the output filter. 0402 case size components are used when possible to further reduce circuit area. The top and bottom layers are 1.5-oz. copper.

The top layer contains the main power traces for V_I, V_O, and $V_{(phase)}$. Also, on the top layer are connections for the remaining pins of the TPS54110 and a large area filled with ground. The bottom layer contains ground and V_O copper areas, and some signal routing. The top and bottom ground traces are connected with multiple vias placed around the board including 10 vias directly under the TPS54110 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C5 and C9), bias-decoupling capacitor (C4), and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high-frequency bypass output capacitor.

Figure 3−1. Top Side Layout

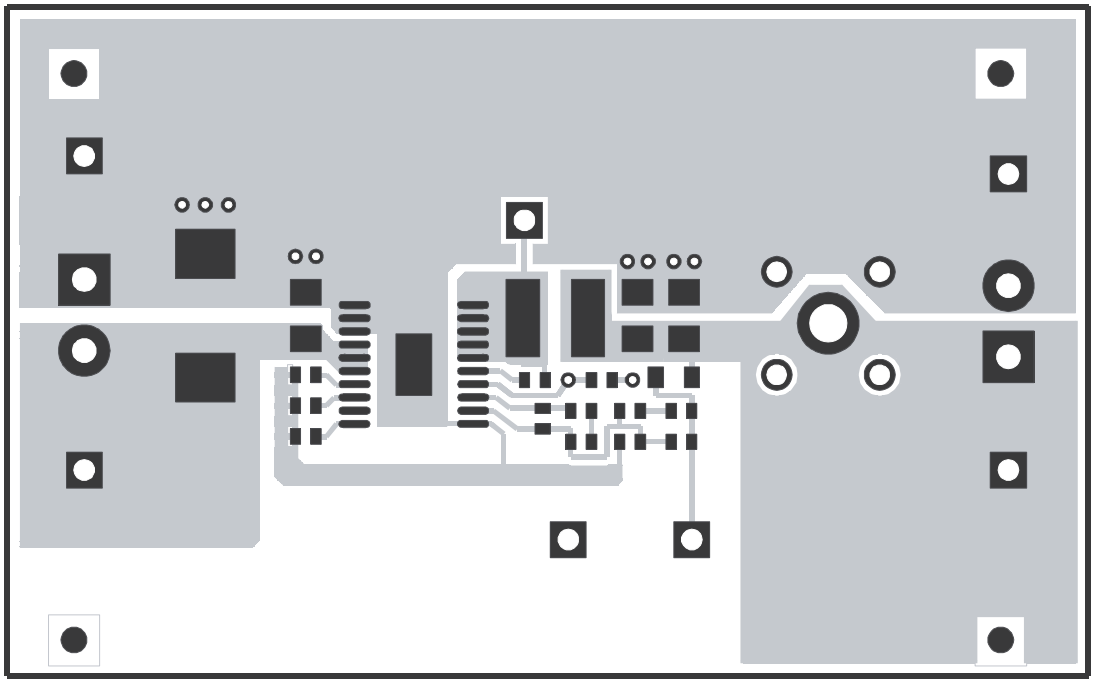


Figure 3−2. Bottom Side Layout

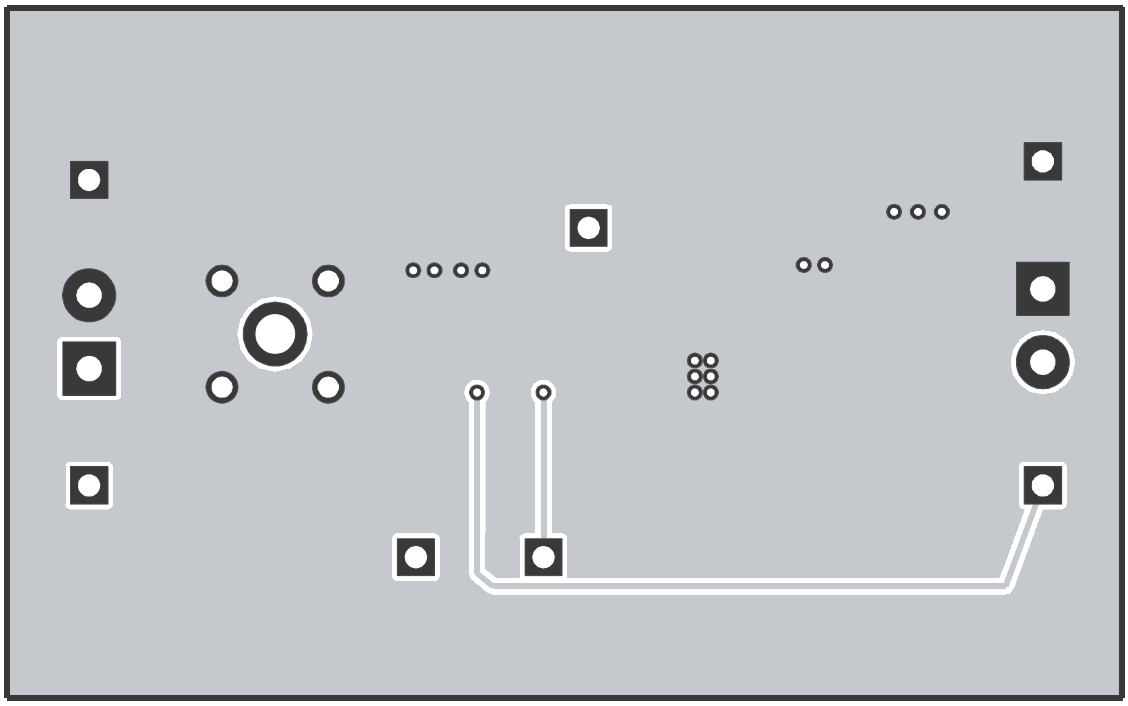
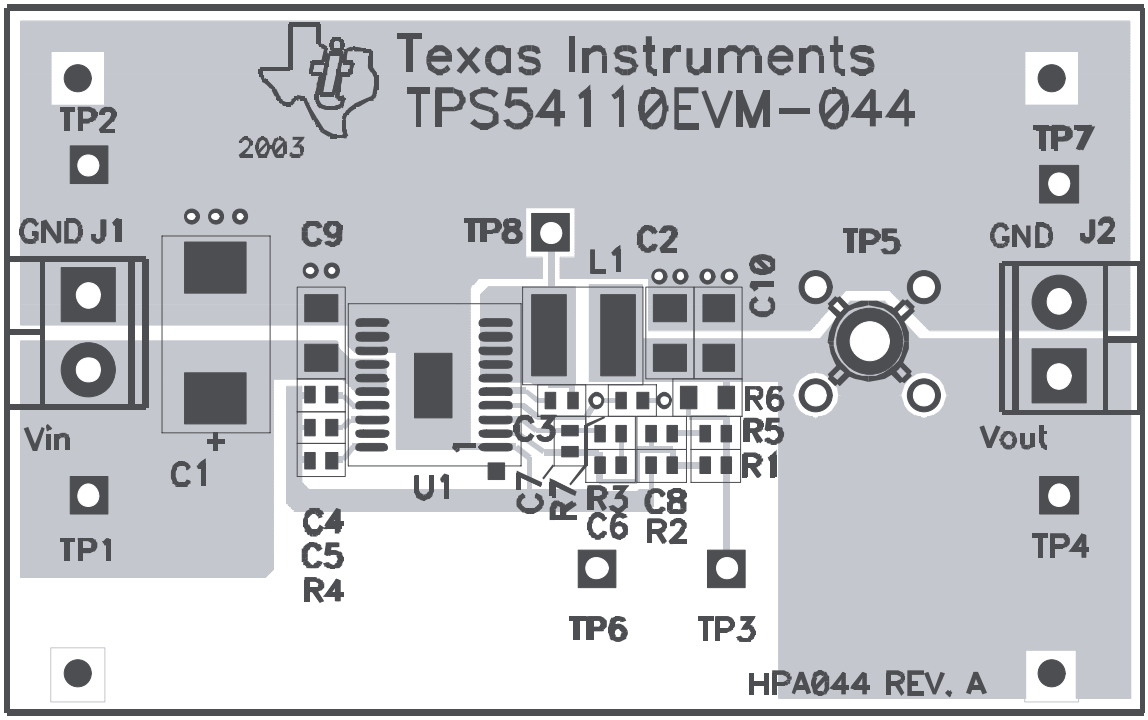


Figure 3−3. Top Side Assembly



Chapter 4

Schematic and Bill of Materials

The TPS54110EVM−044 schematic and bill of materials are presented in this chapter.

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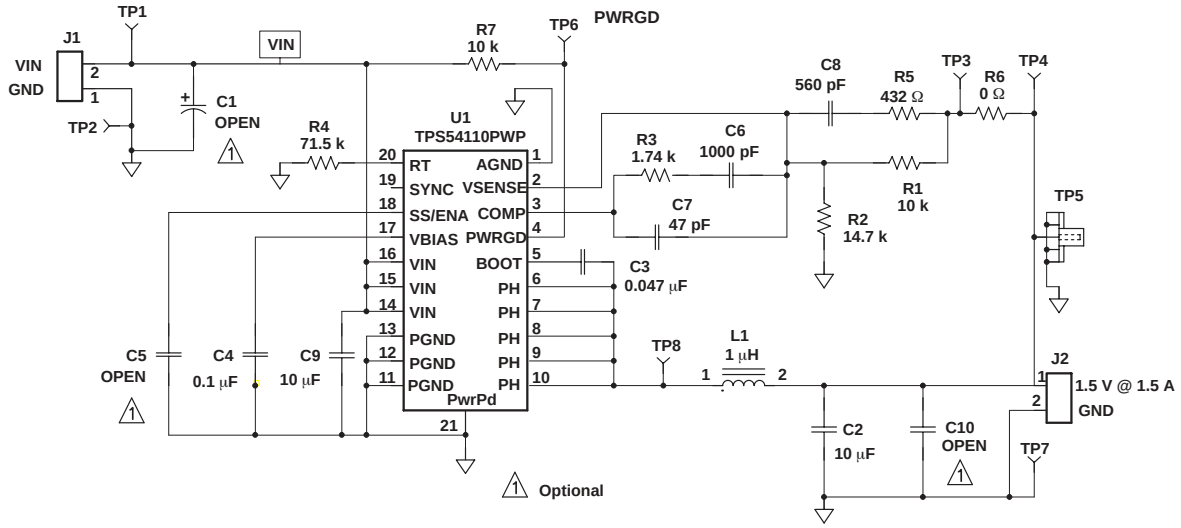
4.1 Schematic

The schematic for the TPS54110EVM−044 is shown in Figure 4−1.

Figure 4−1. TPS54110EVM-044 Schematic



4.2 Bill of Materials

The bill of materials for the TPS54110EVM−044 is given by

Table 4−1. TPS54110EVM-044 Bill of Materials

Count	Ref Des	Description	Size	MFR	Part Number
−	C1	Capacitor, POSCAP, xx µF, xx V, 20%	7343 (D)	Sanyo	Optional
−	C10	Capacitor, ceramic, xx µF, 6.3 V, X5R, 20%	805	std	std
2	C2, C9	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 20%	805	std	std
1	C3	Capacitor, 0.047 µF, 25 V, X7R	402	std	std
1	C4	Capacitor, 0.1 µF, 16 V, X7R	402	std	6TPC100M
−	C5	Capacitor, xx µF, 16 V, X7R	402	std	std
1	C6	Capacitor, 1000 pF, 25 V, X7R	402	std	std
1	C7	Capacitor, 47 pF, 50 V, X7R	402	std	std
1	C8	Capacitor, 560 pF, 50 V, X7R	402	std	std
2	J1, J2	Terminal block, 2 pin, 6 A, 3.5 mm	0.27” x 0.25”	OST	ED1514
1	L1	Inductor, SMT, 1 µH, 2 A, 110 mΩ	0.138 x 0.138	Coilcraft	DO3314−102MX
2	R1, R7	Resistor, chip, 10 kΩ, 1/16 W, 1%	402	std	std
1	R2	Resistor, chip, 14.7 kΩ, 1/16 W, x%	402	std	std
1	R3	Resistor, chip, 1.74 kΩ, 1/16 W, x%	402	std	std
1	R4	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	402	std	std
1	R5	Resistor, chip, 432 Ω, 1/16 W, 1%	402	std	std
1	R6	Resistor, chip, 0 Ω, 1/16 W, 1%	603	std	std
5	TP1, TP3, TP4, TP6, TP8	Test point, red, 1 mm	0.038”	Farnell	240−345
2	TP2, TP7	Test point, black, 1 mm	0.038”	Farnell	240−333
1	TP5	Adaptor, 3,5 mm probe clip (or 131−5031−00)	0.2”	Tektronix	131−4244−00
1	U1	IC, dc/dc converter, adj, 1.5 A	PWP20	TI	TPS54110PWP
1	−−	PCB, 1.3 In x 2.1 In x 0.062 In		Any	HPA044

Notes: 1) These assemblies are ESD sensitive. ESD precautions must be observed.

2) These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.

3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4) Reference designators marked with an asterisk (**) cannot be substituted. All other components can be substituted. All other components can be substituted with equivalent MFG’s components.