

TPS7A6550 Evaluation Module (EVM)

The Texas Instruments TPS7A6550 EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS7A6550 Linear Regulator.

The EVM contains one Linear Regulator (See [Table 1](#)).

Table 1. Device and Package Configurations

REGULATOR	IC	PACKAGE
U1	TPS7A6550QKVUQ1	KVU-3

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1 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the TPS7A6550 EVM.

1.1 Input / Output Connector Descriptions

VBAT is the protected power input for the regulator. The test point provides a power (Vbat) connection and a reverse battery protection diode to allow the user to power the EVM.

GND is the ground return for the regulator. The EVM provides three GND test points to allow the user to power the EVM, connect the load and attach an oscilloscope ground lead.

VIN is a power test point. The test point allows the user to measure the input voltage after the reverse battery protection diode. The user can also apply power to the regulator through this test point.

VOOUT is power output for the regulator. The test point provides a connection to attach a load to the EVM.

1.2 Setup

The input voltage range for the converter is 5.3 V to 40 V. The EVM can support up to 300-mA of load current.

1.3 Operation

The TPS7A6550 will power-up after the VBAT voltage has exceeded the Power-On Reset threshold.

The PCB offers footprints for the TPS7A6550QKTTQ1 or the TPS7A6550QKVUQ1 device.

2 Board Layout

Figure 1, Figure 3 and Figure 2 show the board layout for the TPS7A6550 EVM PWB.

The PowerPAD™ package offers an exposed thermal pad to enhance thermal performance. This must be soldered to the copper landing on the PCB for optimal performance. The PCB provides 2-oz copper planes on the top and bottom to dissipate heat.

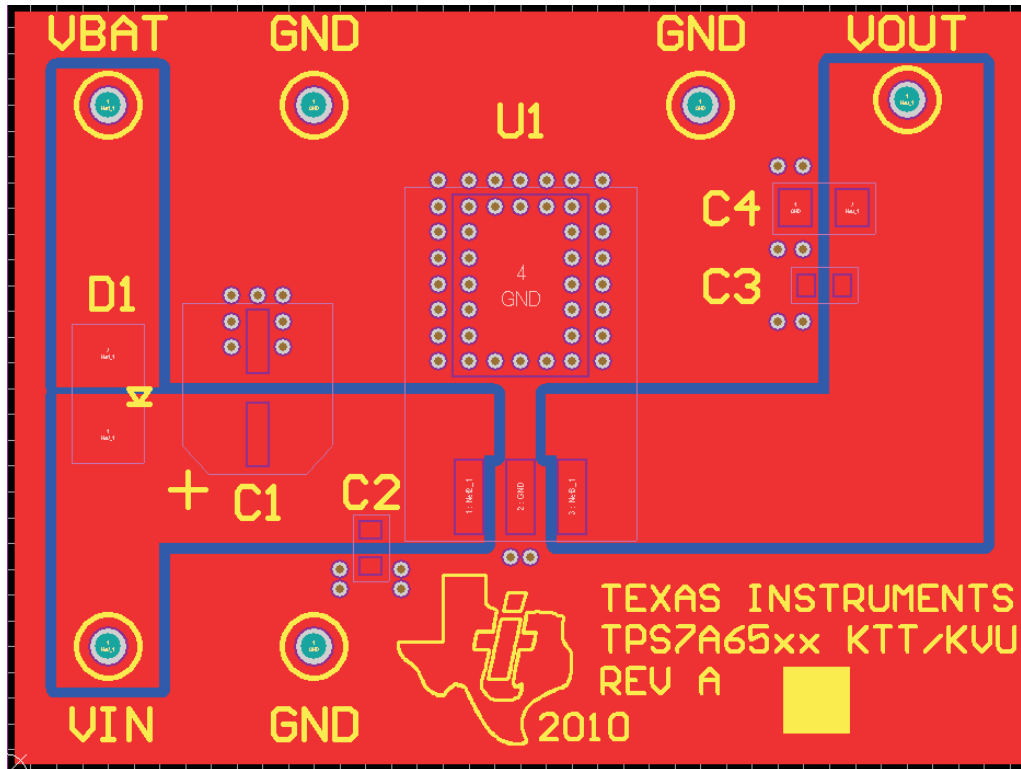


Figure 1. Top Assembly Layer

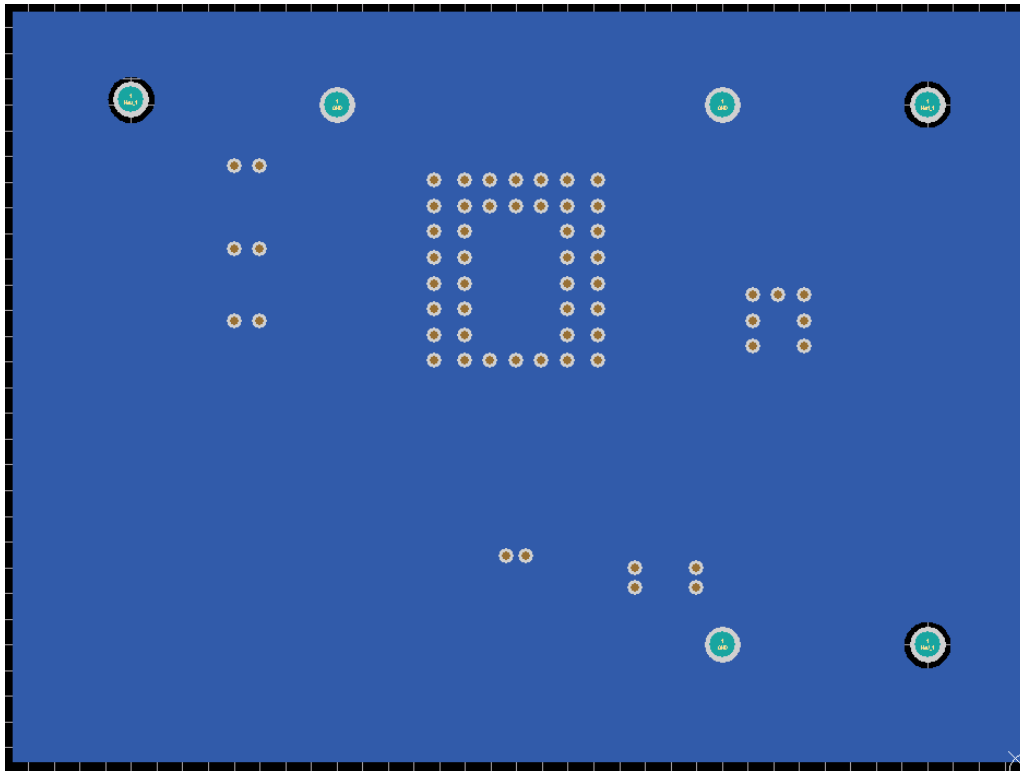


Figure 2. Bottom Layer Routing

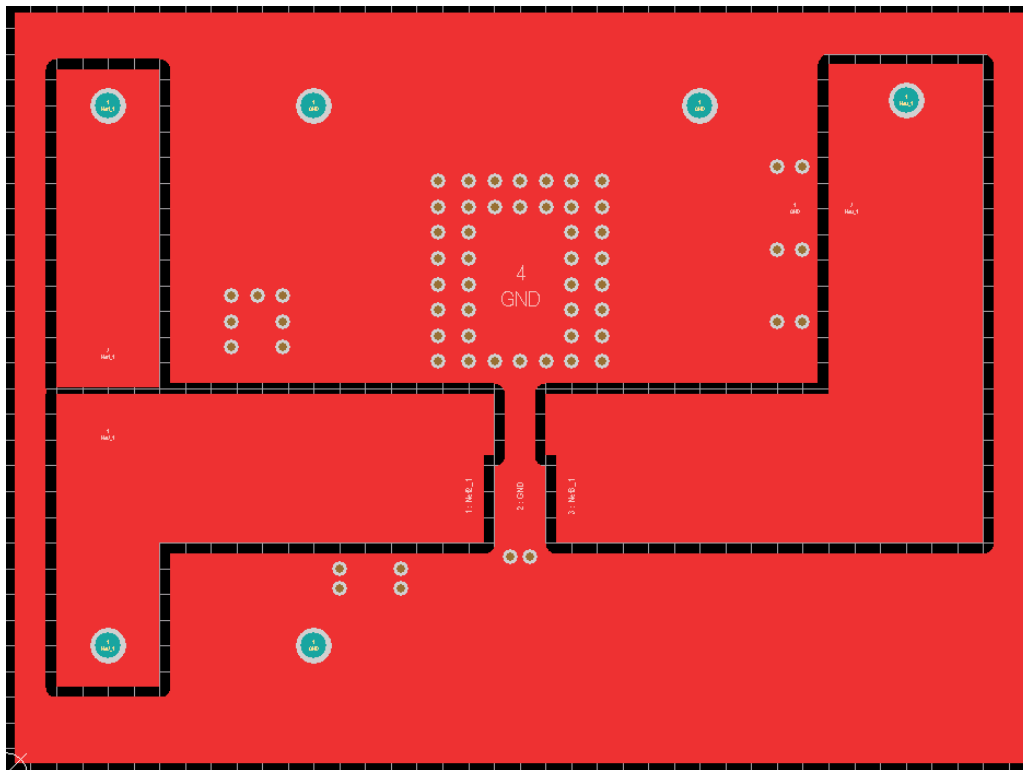


Figure 3. Top Layer Routing

3 Schematic and Bill of Materials

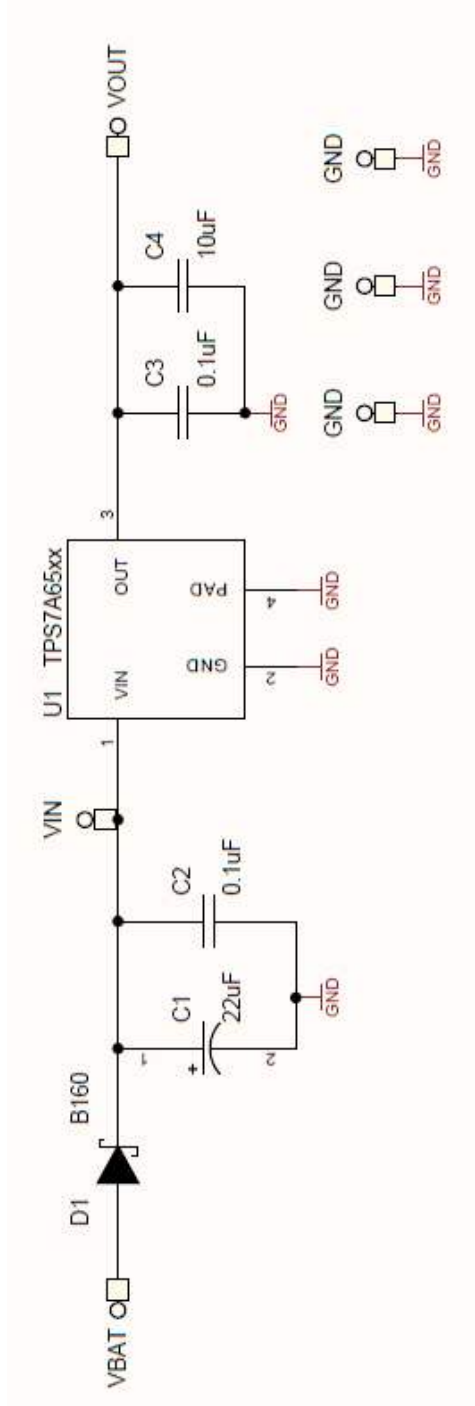


Figure 4. TPS7A6550 EVM Schematic

Table 2. Bill of Materials

Count	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, electrolytic, 22 μ F, 50 V	6.3 mm x 5.8 mm	Panasonic	EEV-FK1H220P
2	C2, C3	Capacitor, ceramic, 0.1 μ F, 50 V, 10%	603	Murata	GCM188R71H104KA57
1	C4	Capacitor, ceramic, 10 μ F, 16 V, 10%	1206	Murata	GRM31CR71C106KAC7
1	D1	Diode, Schottky, 1 A, 60 V	SMA	Diodes	B160-13-F
6	GND (x3), VBAT, VIN, VOUT	Test point, 52-mil	0.052	Kobiconn	151-103-RC
1	U1	IC, TPS7A6550QKVUQ1		TI	TPS7A6550QKVUQ1
	–	PCB, 2 inch x 1.5 inch x 0.062		Any	TPS7A65xx, REV A

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 5.3 V to 40 V and the output voltage range of 5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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