

# SN54F350, SN74F350 4-BIT SHIFTER WITH 3-STATE OUTPUTS

SDFS073 - D2932, MARCH 1987 - REVISED JANUARY 1989

- Shifts 4-Bits of Data to 0, 1, 2 or 3 Places Under Control of Two Select Lines
- Three-State Outputs for Bus Organized Systems
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

## description

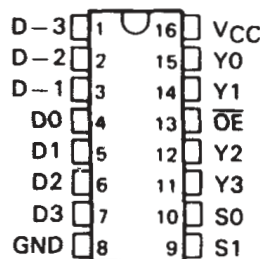
This device is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes shifts of the data word. This makes it possible to perform shifts of 0, 1, 2, or 3 places on words of any length, with suitable interconnection.

A 7-bit data word is introduced at the D inputs and is shifted according to the code applied to the select inputs S0 and S1. Y0 through Y3 are 3-state outputs controlled by an output enable,  $\overline{OE}$ . When  $\overline{OE}$  is low, the outputs follow the selected data inputs; when  $\overline{OE}$  is high, the outputs are in a high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical with zeroes pulled in at either or both ends of the shifting field, arithmetic with the sign bit repeated during a shift down, or end-around with the data word forming a continuous loop.

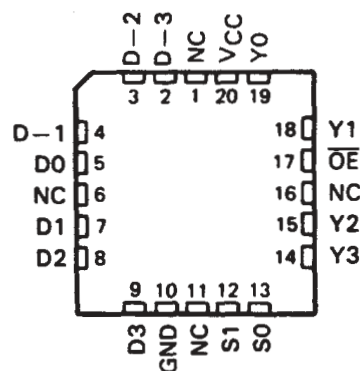
FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{OE}$	S1	S0	Y0	Y1	Y2	Y3
H	X	X	Z	Z	Z	Z
L	L	L	D0	D1	D2	D3
L	L	H	D-1	D0	D1	D2
L	H	L	D-2	D-1	D0	D1
L	H	H	D-3	D-2	D-1	D0

SN54F350 . . . J PACKAGE  
SN74F350 . . . D OR N PACKAGE  
(TOP VIEW)



SN54F350 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

## logic equations

$$Y_0 = \overline{S_0} \overline{S_1} D_0 + S_0 \overline{S_1} D_{-1} + \overline{S_0} S_1 D_{-2} + S_0 S_1 D_{-3}$$

$$Y_1 = \overline{S_0} \overline{S_1} D_1 + S_0 \overline{S_1} D_0 + \overline{S_0} S_1 D_{-1} + S_0 S_1 D_{-2}$$

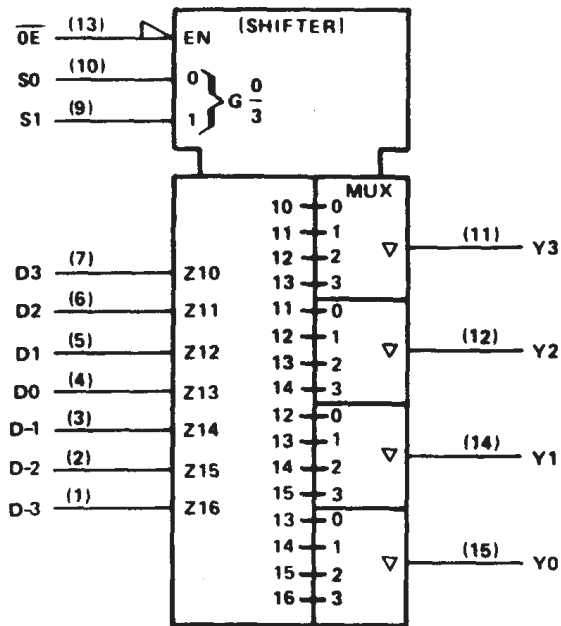
$$Y_2 = \overline{S_0} \overline{S_1} D_2 + S_0 \overline{S_1} D_1 + \overline{S_0} S_1 D_0 + S_0 S_1 D_{-1}$$

$$Y_3 = \overline{S_0} \overline{S_1} D_3 + S_0 \overline{S_1} D_2 + \overline{S_0} S_1 D_1 + S_0 S_1 D_0$$

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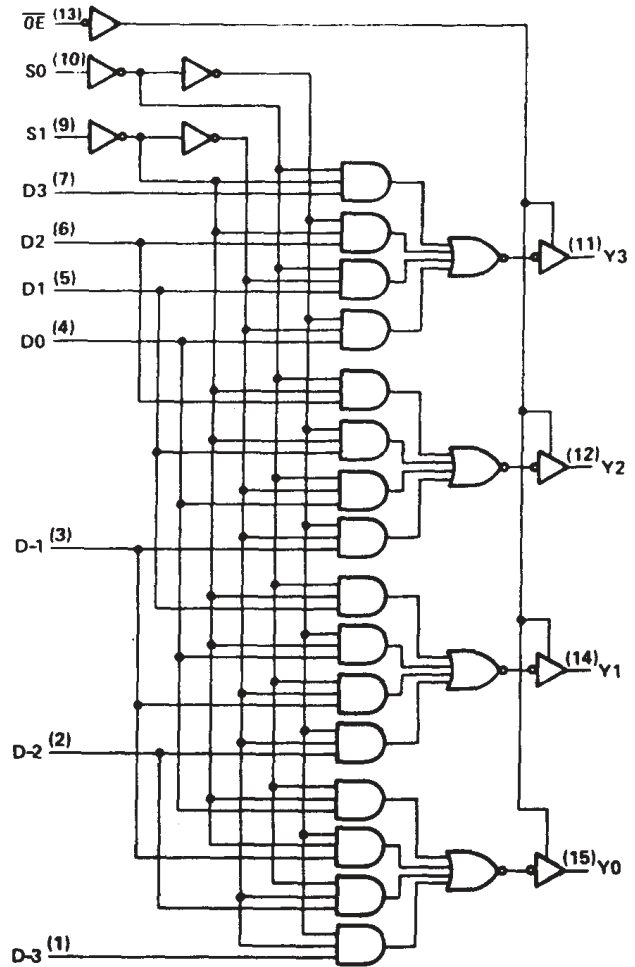
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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC .....	-0.5 V to 7 V
Input voltage‡ .....	-1.2 V to 7 V
Input current .....	-30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state .....	-0.5 V to 5.5 V
Voltage applied to any output in the high state .....	-0.5 V to VCC
Current into any output in the low state: SN54F350 .....	40 mA
SN74F350 .....	48 mA
Operating free-air temperature range: SN54F350 .....	-55°C to 125°C
SN74F350 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

# SN54F350, SN74F350 4-BIT SHIFTER WITH 3-STATE OUTPUTS

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## recommended operating conditions

		SN54F350			SN74F350			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>IK</sub>	Input clamp current			-18			-18	mA
I <sub>OH</sub>	High-level output current			-3			-3	mA
I <sub>OL</sub>	Low-level output current			20			20	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F350			SN74F350			UNIT	
			MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2			-1.2	V	
V <sub>OH</sub>	Any output	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1 mA	2.5	3.4		2.5	3.4		V	
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.4	3.3		2.4	3.3			
V <sub>OL</sub>	Any output	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -1 mA to -3 mA				2.7			V	
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA	0.30	0.5		0.35	0.5			
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50			50	μA	
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50			-50	μA	
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1			0.1	mA	
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			20			20	μA	
I <sub>IL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V			-1.2			-1.2	mA	
I <sub>OS</sub> <sup>‡</sup>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0	-60		-150	-60		-150	mA	
I <sub>CCH</sub>	Any output	V <sub>CC</sub> = 5.5 V	Outputs high		22	35	22		35	mA
I <sub>CCL</sub>			Outputs low		27	41	27		41	
I <sub>CCZ</sub>			Outputs off		26	42	26		42	

## switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX <sup>‡</sup>				UNIT
			'F350			SN54F350		SN74F350		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Data	Any Y	2.2	4.1	6	3	7.5	2.2	7	ns
t <sub>PHL</sub>	Any D		1.7	3.6	5.5	2.5	7	1.7	6.5	
t <sub>PLH</sub>	S0, S1	Any Y	3.2	7.4	10	4	13	3.2	11	ns
t <sub>PHL</sub>			2.2	6.1	8.5	3	10	2.2	9.5	
t <sub>PZH</sub>	OE	Any Y	1.7	4.6	7	2.5	8.5	1.7	8	ns
t <sub>PZL</sub>			3.2	6.6	9	4	11	3.2	10	
t <sub>PHZ</sub>	OE	Any Y	1.2	3.5	5.5	2	7	1.2	6.5	ns
t <sub>PLZ</sub>			1.2	3.6	5.5	2	8.5	1.2	6.5	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTE 1: Load circuits and waveforms are shown in Section 1.



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