



HCPL4503M High Speed Transistor Optocouplers

Features

- $V_{ISO} = 5kV$ RMS is standard for all devices
- High speed – 1MBit/s
- Superior CMR, $CM_H = 50kV/ms$ (typical); $CM_L = 30kV/ms$ (typical)
- No base connection for improved noise immunity
- CTR guaranteed $0^{\circ}C$ to $70^{\circ}C$
- U.L. recognized (File # E90700, Vol 2)
- VDE approval pending

Applications

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

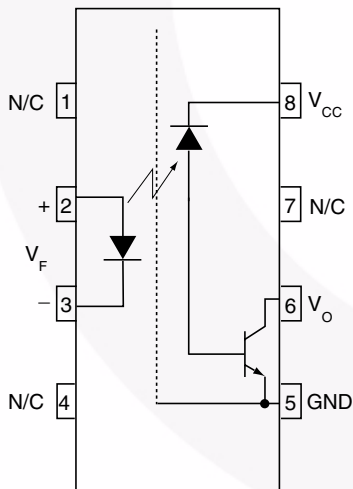
Description

The HCPL4503M optocoupler consists of an AlGaAs LED optically coupled to a high speed photodetector transistor.

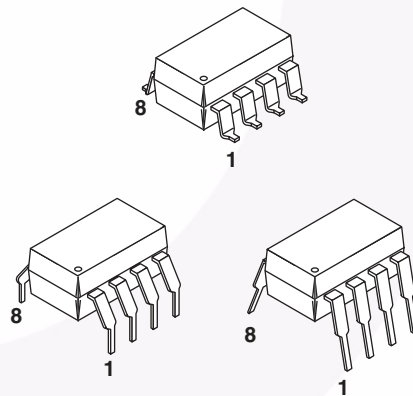
A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor. The base of the phototransistor is not bonded out to a pin for improved noise immunity.

An internal noise shield provides superior common mode rejection of $15kV/\mu s$ minimum.

Schematic



Package Outlines



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	$^\circ\text{C}$
T_{OPR}	Operating Temperature	-40 to +100	$^\circ\text{C}$
T_{SOL}	Lead Solder Temperature	260 for 10 sec	$^\circ\text{C}$
EMITTER			
I_F (avg)	DC/Average Forward Input Current	25	mA
I_F (pk)	Peak Forward Input Current (50% duty cycle, 1ms P.W.)	50	mA
I_F (trans)	Peak Transient Input Current – ($\leq 1\mu\text{s}$ P.W., 300pps)	1.0	A
V_R	Reverse Input Voltage	5	V
P_D	Input Power Dissipation	100	mW
DETECTOR			
I_O (avg)	Average Output Current	8	mA
I_O (pk)	Peak Output Current	16	mA
V_{CC}	Supply Voltage	-0.5 to 30	V
V_O	Output Voltage	-0.5 to 20	V
PD	Output Power Dissipation	100	mW

Electrical Characteristics ($T_A = 0$ to 70°C unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
EMITTER						
V_F	Input Forward Voltage	$I_F = 16\text{mA}$, $T_A = 25^\circ\text{C}$		1.45	1.7	V
		$I_F = 16\text{mA}$			1.8	
B_{VR}	Input Reverse Breakdown Voltage	$I_R = 10\mu\text{A}$	5.0			V
$\Delta V_F/\Delta T_A$	Temperature Coefficient of forward voltage	$I_F = 16\text{mA}$		-1.6		mV/ $^\circ\text{C}$
DETECTOR						
I_{OH}	Logic high output current	$I_F = 0\text{mA}$, $V_O = V_{CC} = 5.5\text{V}$, $T_A = 25^\circ\text{C}$		0.001	0.5	μA
		$I_F = 0\text{mA}$, $V_O = V_{CC} = 15\text{V}$, $T_A = 25^\circ\text{C}$		0.005	1	
		$I_F = 0\text{mA}$, $V_O = V_{CC} = 15\text{V}$			50	
I_{CCL}	Logic low supply current	$I_F = 16\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{V}$		120	200	μA
I_{CCH}	Logic high supply current	$I_F = 0\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{V}$, $T_A = 25^\circ\text{C}$			1	μA
		$I_F = 0\text{mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{V}$			2	

*All Typicals at $T_A = 25^\circ\text{C}$

Transfer Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
COUPLED						
CTR	Current Transfer Ratio ⁽⁵⁾	$I_F = 16\text{mA}$, $V_O = 0.4\text{V}$, $V_{CC} = 4.5\text{V}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾	19	27	50	%
		$I_F = 16\text{mA}$, $V_{CC} = 4.5\text{V}$, $V_{OL} = 0.5\text{V}$	15	30		
V_{OL}	Logic low output voltage output voltage	$I_F = 16\text{mA}$, $I_O = 3\text{mA}$, $V_{CC} = 4.5\text{V}$, $T_A = 25^\circ\text{C}$			0.5	V
		$I_F = 16\text{mA}$, $I_O = 2.4\text{mA}$, $V_{CC} = 4.5\text{V}$			0.5	

*All Typicals at $T_A = 25^\circ\text{C}$

Note:

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.

Electrical Characteristics (Continued) ($T_A = 0$ to 70°C unless otherwise specified)

Switching Characteristics ($V_{CC} = 5\text{V}$)

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
T_{PHL}	Propagation Delay Time to Logic Low	$R_L = 1.9\text{k}\Omega$, $I_F = 16\text{mA}^{(2)}$ (Fig. 7) $T_A = 25^\circ\text{C}$		0.45	0.8	μs
		$R_L = 1.9\text{k}\Omega$, $I_F = 16\text{mA}^{(2)}$ (Fig. 7)			1.0	μs
T_{PLH}	Propagation Delay Time to Logic High	$R_L = 1.9\text{k}\Omega$, $I_F = 16\text{mA}^{(2)}$ (Fig. 7) $T_A = 25^\circ\text{C}$		0.3	0.8	μs
		$R_L = 1.9\text{k}\Omega$, $I_F = 16\text{mA}^{(2)}$ (Fig. 7)			1.0	μs
ICM_{HI}	Common Mode Transient Immunity at Logic High	$I_F = 0\text{ mA}$, $V_{CM} = 1,500V_{P-P}$, $T_A = 25^\circ\text{C}$, $R_L = 1.9\text{k}\Omega^{(3)}$ (Fig. 8)	15,000	50,000		$\text{V}/\mu\text{s}$
ICM_{LI}	Common Mode Transient Immunity at Logic Low	$I_F = 16\text{mA}$, $V_{CM} = 1,500V_{P-P}$, $R_L = 1.9\text{k}\Omega^{(3)}$ (Fig. 8)	15,000	30,000		$\text{V}/\mu\text{s}$

*All Typicals at $T_A = 25^\circ\text{C}$

Isolation Characteristics

Symbol	Characteristics	Test Conditions	Min.	Typ.**	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25^\circ\text{C}$, $t = 5\text{s}$, $V_{I-O} = 3000\text{VDC}^{(4)}$			1.0	μA
V_{ISO}	Withstand Insulation Test Voltage	$RH \leq 50\%$, $T_A = 25^\circ\text{C}$, $I_{I-O} \leq 2\mu\text{A}$, $t = 1\text{ min.}^{(4)}$	5,000			V_{RMS}
R_{I-O}	Resistance (input to output)	$V_{I-O} = 500\text{VDC}$		10^{12}		Ω
C_{I-O}	Capacitance (input to output)	$f = 1\text{MHz}^{(4)}$		0.6		pF

Notes:

- The $1.9\text{k}\Omega$ load represents 1 TTL unit load of 1.6mA and $5.6\text{k}\Omega$ pull-up resistor.
- Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{V}$).
Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8\text{V}$).
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.

Typical Performance Curves

Fig. 1 Normalized CTR vs. Forward Current

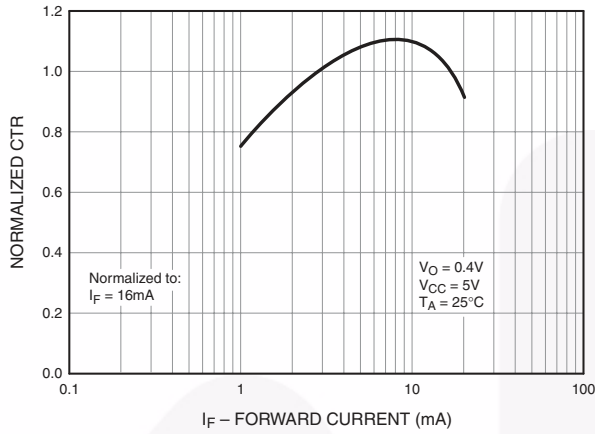


Fig. 2 Normalized CTR vs. Temperature

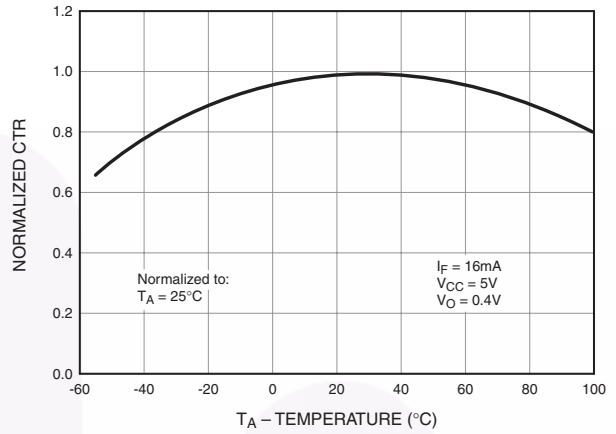


Fig. 3 Output Current vs. Output Voltage

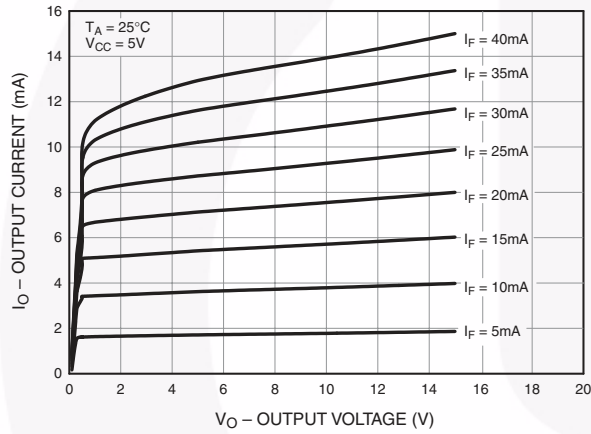


Fig. 4 Logic High Output Current vs. Temperature

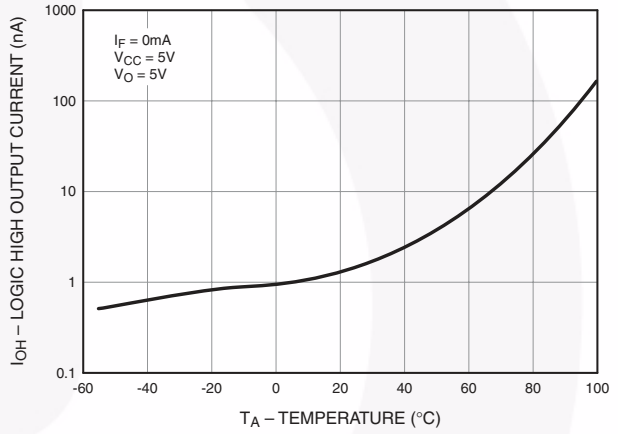


Fig. 5 Propagation Delay vs. Temperature

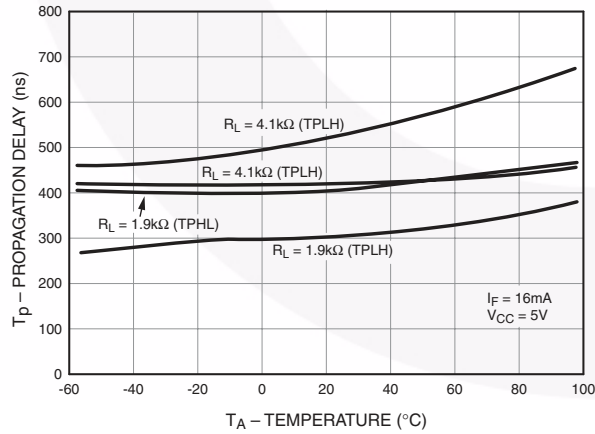
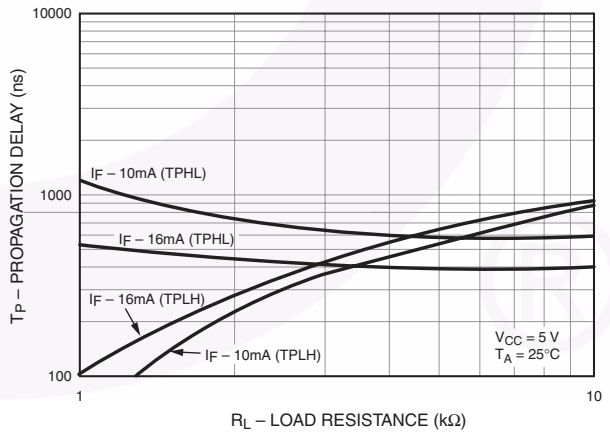


Fig. 6 Propagation Delay vs. Load Resistance



Test Circuits

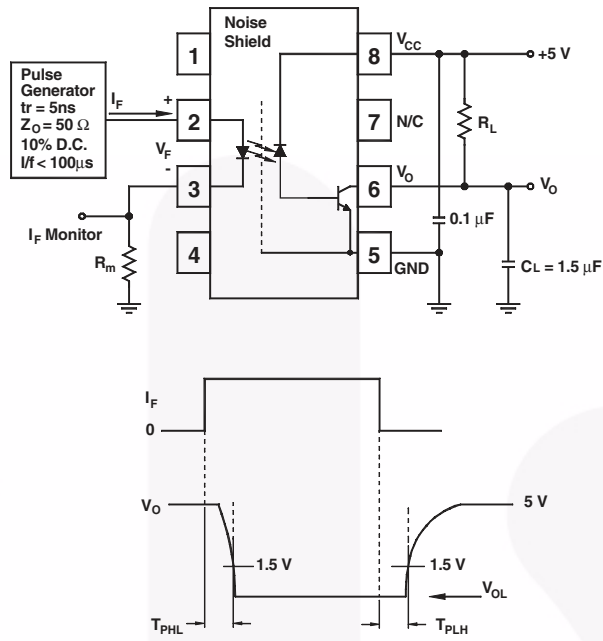


Fig. 7 Switching Time Test Circuit

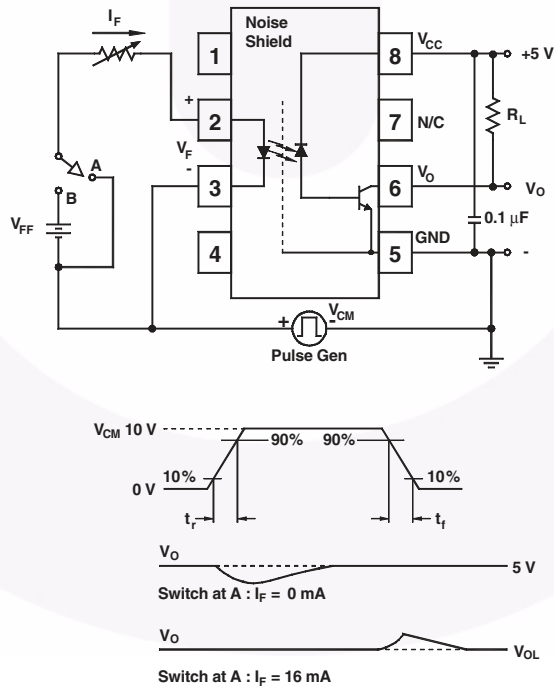
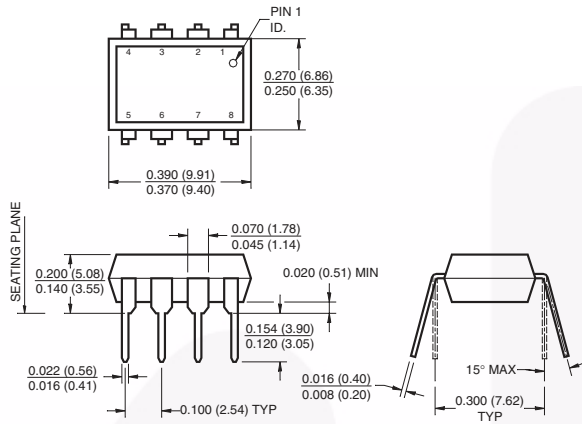


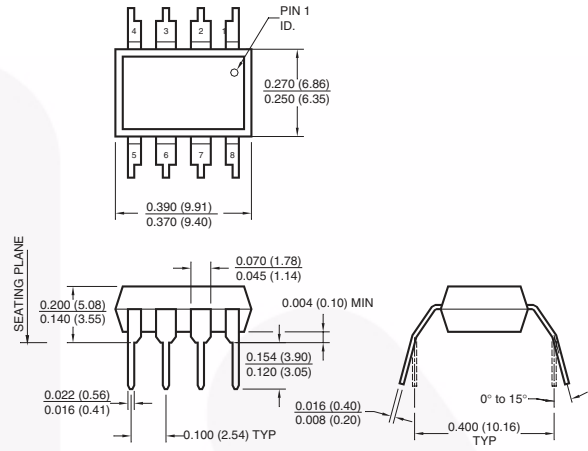
Fig. 8 Common Mode Immunity Test Circuit

Package Dimensions

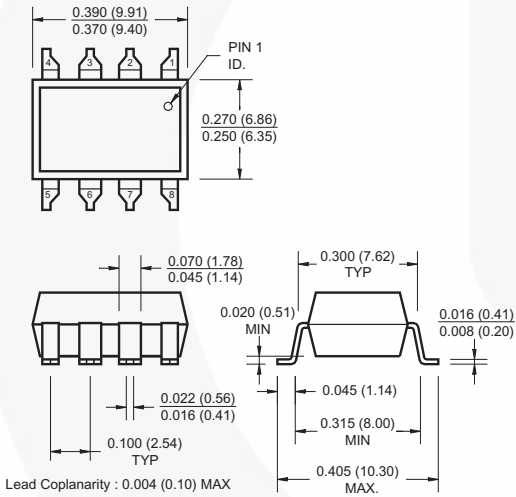
Through Hole



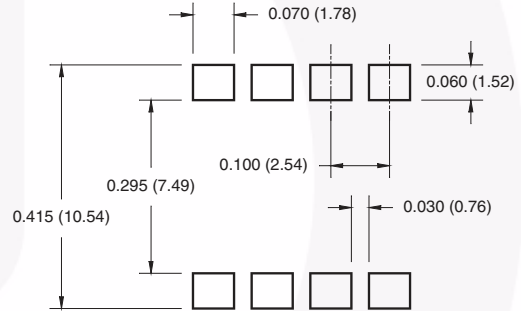
0.4" Lead Spacing



Surface Mount



8-Pin DIP – Land Pattern



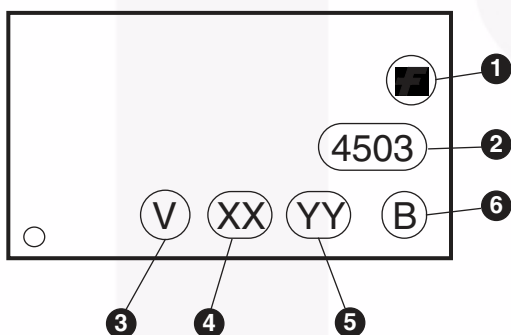
Note:

All dimensions are in inches (millimeters)

Ordering Information

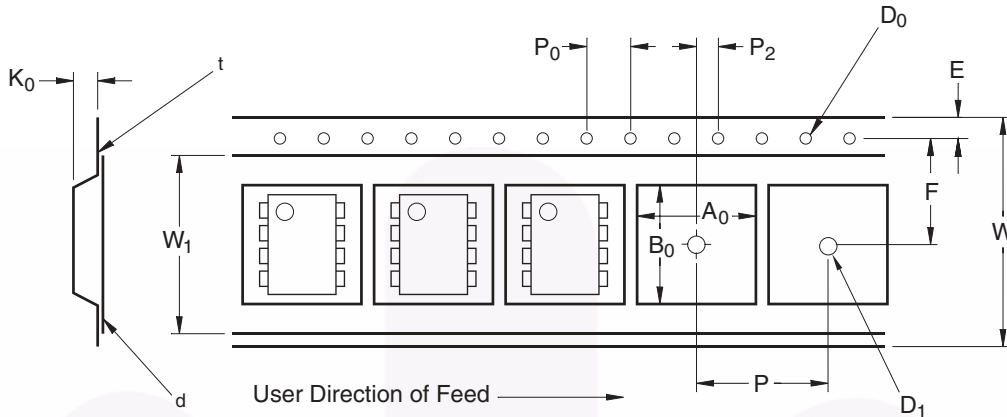
Option	Example Part Number	Description
No Option	HCPL4503M	Standard Through Hole
S	HCPL4503SM	Surface Mount Lead Bend
SD	HCPL4503SDM	Surface Mount; Tape and Reel
T	HCPL4503TM	0.4" Lead Spacing
V	HCPL4503VM	VDE0884
TV	HCPL4503TVM	VDE0884; 0.4" Lead Spacing
SV	HCPL4503SVM	VDE0884; Surface Mount
SDV	HCPL4503SDVM	VDE0884; Surface Mount; Tape and Reel

Marking Information



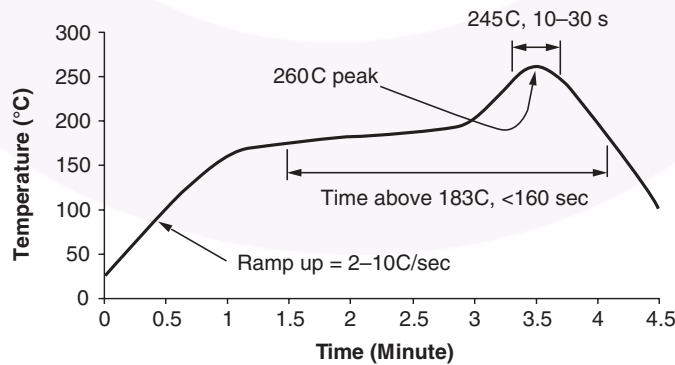
Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., '03'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Carrier Tape Specifications



Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P ₀	Sprocket Hole Pitch	4.0 ± 0.1
D ₀	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P ₂		4.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A ₀	Pocket Dimensions	10.30 ± 0.20
B ₀		10.30 ± 0.20
K ₀		4.90 ± 0.20
W ₁	Cover Tape Width	1.6 ± 0.1
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

Reflow Profile



- Peak reflow temperature: 260C (package surface temperature)
- Time of temperature higher than 183C for 160 seconds or less
- One time soldering reflow is recommended



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Current Transfer Logic™	Green FPS™ e-Series™	QS™	TinyLogic®
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