SN74AHCT14Q-Q1 Automotive Hex Schmitt-Trigger Inverter

1 Features

- Qualified for automotive applications
- EPIC™ (Enhanced-Performance Implanted CMOS) process
- Inputs are TTL-Voltage compatible
- Latch-Up performance exceeds 250 mA per JESD 17

2 Applications

- Synchronize invterted clock inputs
- Debounce a switch
- Invert a digital signal

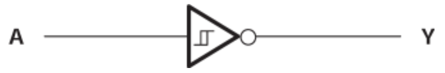
3 Description

The SN74AHCT14Q-Q1 contains six independent inverters. This device performs the Boolean function Y = $\overline{A}$.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN74AHCT14Q-Q1	D (SOIC, 14)	8.65 mm × 6 mm	8.65 mm × 3.9 mm
	PW (TSSOP, 14)	5 mm × 6.4 mm	5 mm × 4.4 mm
	BQA (WQFN, 14)	3 mm × 2.5 mm	3 mm × 2.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Inverter (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2023) to Revision C (June 2023)	Page
• Added the *Applications* section	1
• Updated the *Package Information* table to include package leads and body size	1
• Added the *BQA* package	1

Changes from Revision A (April 2008) to Revision B (May 2023)	Page
• Added *Package Information* table, *Pin Functions* table, and *Thermal Information* table	1

5 Pin Configuration and Functions

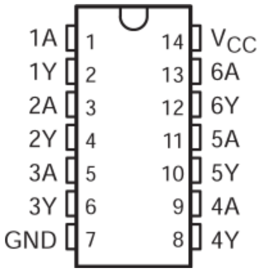

1A 1
1Y 2
2A 3
2Y 4
3A 5
3Y 6
GND 7
14 VCC
13 6A
12 6Y
11 5A
10 5Y
9 4A
8 4Y

Figure 5-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

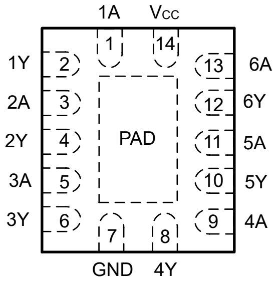

1A
VCC
1
14
1Y 2
2A 3
2Y 4
3A 5
3Y 6
PAD
13 6A
12 6Y
11 5A
10 5Y
9 4A
7
8
GND
4Y

Figure 5-2. BQA Package, 14-Pin WQFN (Top View)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A	1	I	Input 1A
1Y	2	O	Output 1Y
2A	3	I	Input 2A
2Y	4	O	Output 2Y
3A	5	I	Input 3A
3Y	6	O	Output 3Y
4Y	8	O	Output 4Y
4A	9	I	Input 4A
5Y	10	O	Output 5Y
5A	11	I	Input 5A
6Y	12	O	Output 6Y
6A	13	I	Input 6A
GND	7	—	Ground Pin
NC	—	—	No Connection
V_{CC}	14	—	Power Pin
Thermal Pad[1]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) For BQA package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I [1]	Input voltage range		−0.5	7	V
V_O [1]	Output voltage range		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	($V_I < 0$)		−20	mA
I_{OK}	Output clamp current	($V_O < 0$ or $V_O > V_{CC}$)		±20	mA
I_O	Continuous output current	($V_O = 0$ to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	MIL-STD-883, Method 3015(1)	±2000	V
		Machine Model (C = 200 pF, R = 0)(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see Note 1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−8	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AHCT14Q-Q1			UNIT
		D	PW	BQA	
		14 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	113	88.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{T+} Positive-going input threshold voltage		4.5 V	0.9		1.9	0.9	1.9	V
		5.5 V	1		2.1	1	2.1	
V_{T-} Negative-going input threshold voltage		4.5 V	0.5		1.5	0.5	1.5	V
		5.5 V	0.6		1.7	0.6	1.7	
ΔV_T Hysteresis (V_{T+} - V_{T-})		4.5 V	0.4		1.4	0.4	1.4	V
		5.5 V	0.4		1.5	0.4	1.5	
V_{OH}	I_{OH} = -50 µA	4.5 V	4.4	4.5		4.4		V
	I_{OH} = -8 mA	4.5 V	3.94			3.8		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1	v
	I_{OL} = 8 mA	4.5 V			0.36		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20	µA
ΔI_{CC} [1]	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2	10			pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	C_L= 15 pF		4	7	1	8	ns
t_{PHL}					4	7	1	8	
t_{PLH}	A	Y	C_L = 50 pF		5.5	8	1	9	ns
t_{PHL}					5.5	8	1	9	

6.7 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.9		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.1			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.5	V

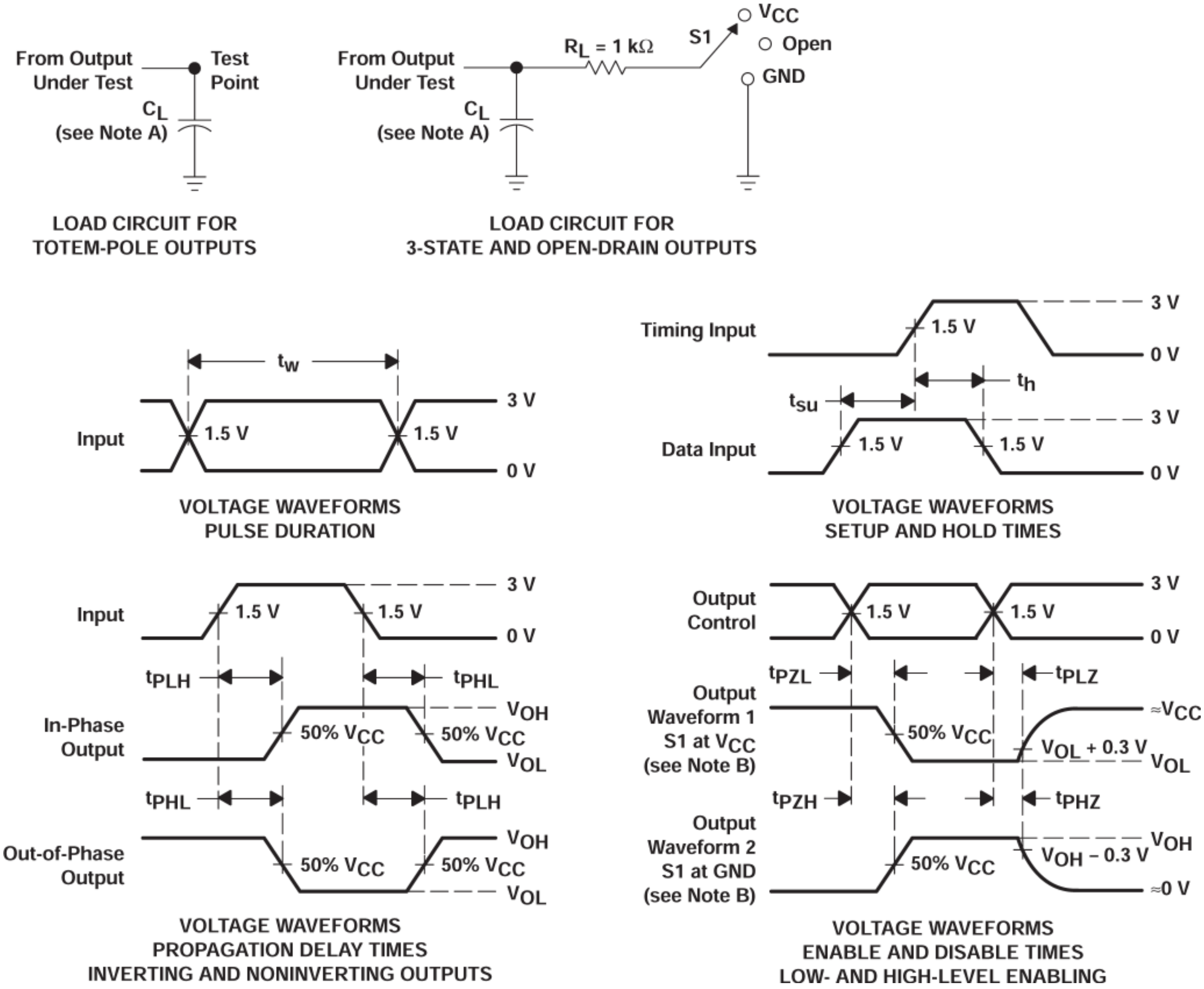
(1) Characteristics are for surface-mount packages only.

6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	12	pF

7 Parameter Measurement Information


From Output Under Test
Test Point
C_L (see Note A)
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS
From Output Under Test
R_L = 1 kΩ
S1
V_{CC}
Open
GND
C_L (see Note A)
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS
t_w
Input
1.5 V
1.5 V
3 V
0 V
VOLTAGE WAVEFORMS PULSE DURATION
Timing Input
1.5 V
3 V
0 V
t_{su}
t_h
Data Input
1.5 V
1.5 V
3 V
0 V
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES
Input
1.5 V
1.5 V
3 V
0 V
t_{PLH}
t_{PHL}
In-Phase Output
50% V_{CC}
50% V_{CC}
V_{OH}
V_{OL}
t_{PHL}
t_{PLH}
Out-of-Phase Output
50% V_{CC}
50% V_{CC}
V_{OH}
V_{OL}
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS
Output Control
1.5 V
1.5 V
3 V
0 V
t_{PZL}
t_{PLZ}
Output Waveform 1 S1 at V_{CC} (see Note B)
50% V_{CC}
≈V_{CC}
V_{OL} + 0.3 V
V_{OL}
t_{PZH}
t_{PHZ}
Output Waveform 2 S1 at GND (see Note B)
50% V_{CC}
V_{OH} − 0.3 V
V_{OH}
≈0 V
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 7-1. Load Circuit and Voltage Waveforms

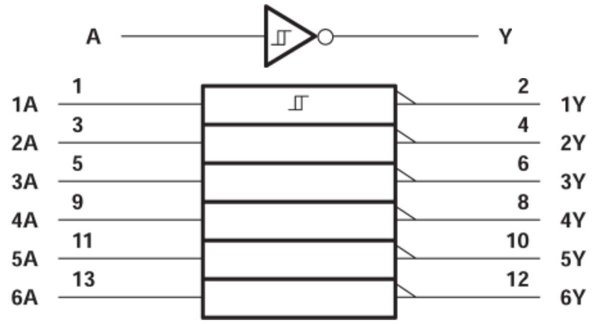
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

8 Detailed Description

8.1 Overview

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

8.2 Functional Block Diagram



The † symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 8-1. Logic Diagram, Each Inverter (Positive Logic)

8.3 Device Functional Modes

Table 8-1. Function Table (Each Inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT14QDRG4Q1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT14Q	Samples
SN74AHCT14QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT14Q	Samples
SN74AHCT14QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB14Q	Samples
SN74AHCT14QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB14Q	Samples
SN74AHCT14QWBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHT14Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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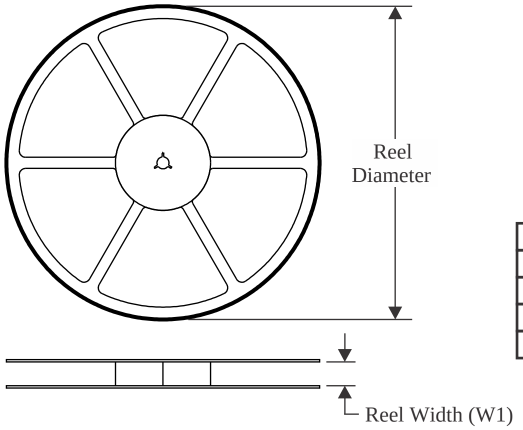
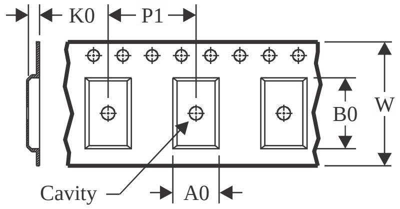
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

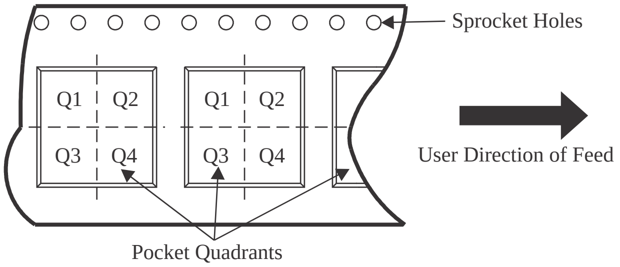

Reel
Diameter
Reel Width (W1)

TAPE DIMENSIONS


K0
P1
B0
W
Cavity
A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

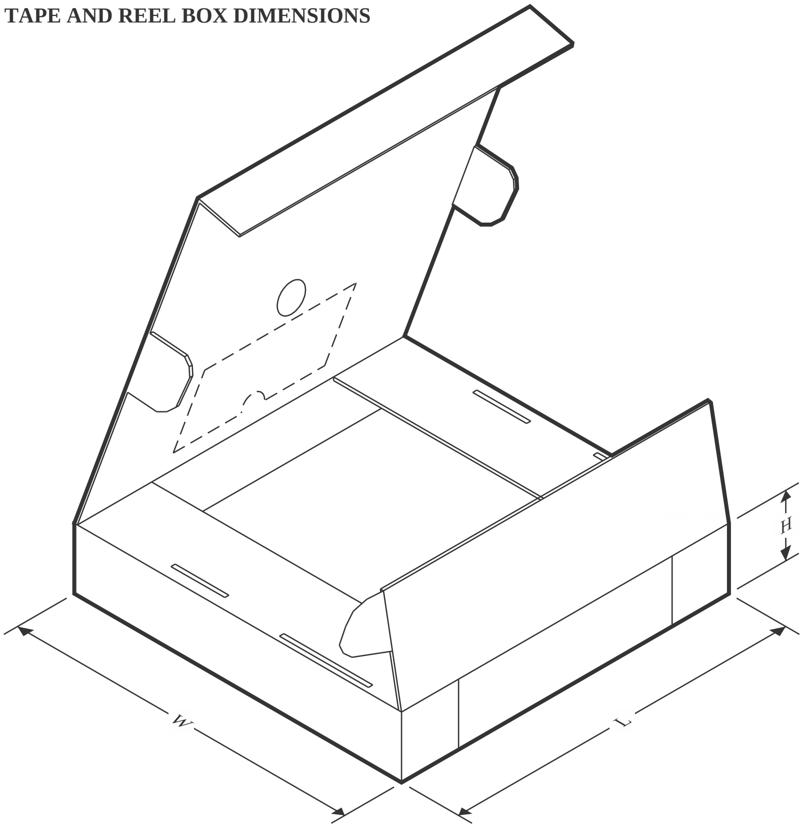
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Sprocket Holes
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
User Direction of Feed
Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT14QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT14QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT14QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT14QPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHCT14QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHCT14QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

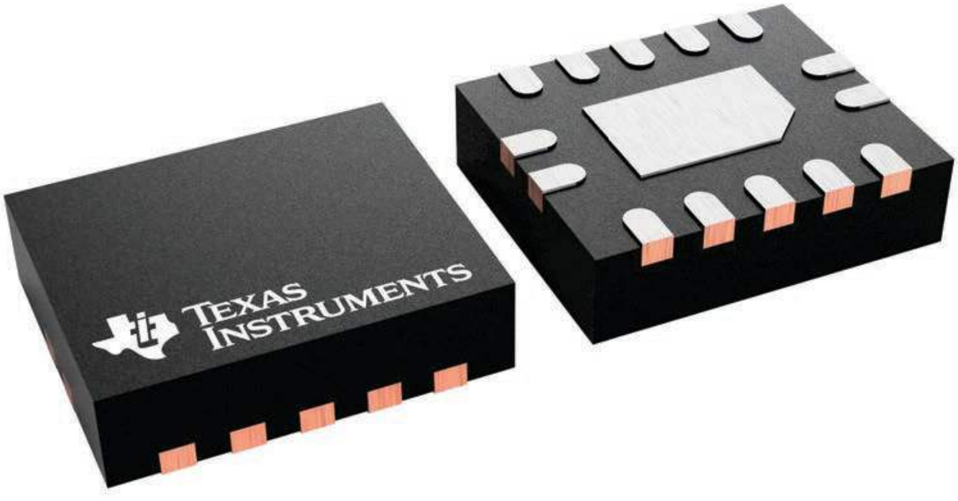
BQA 14

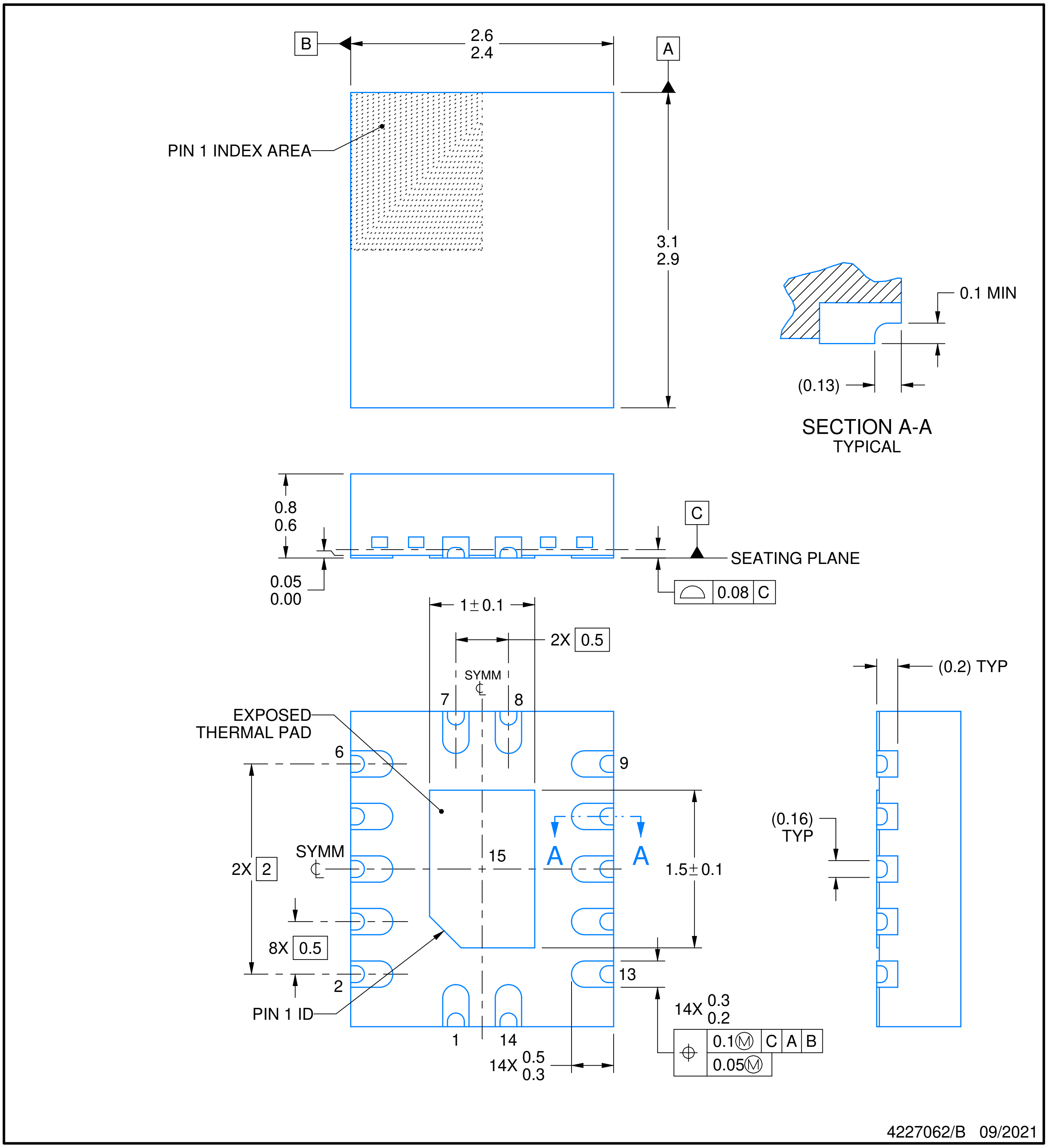
WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

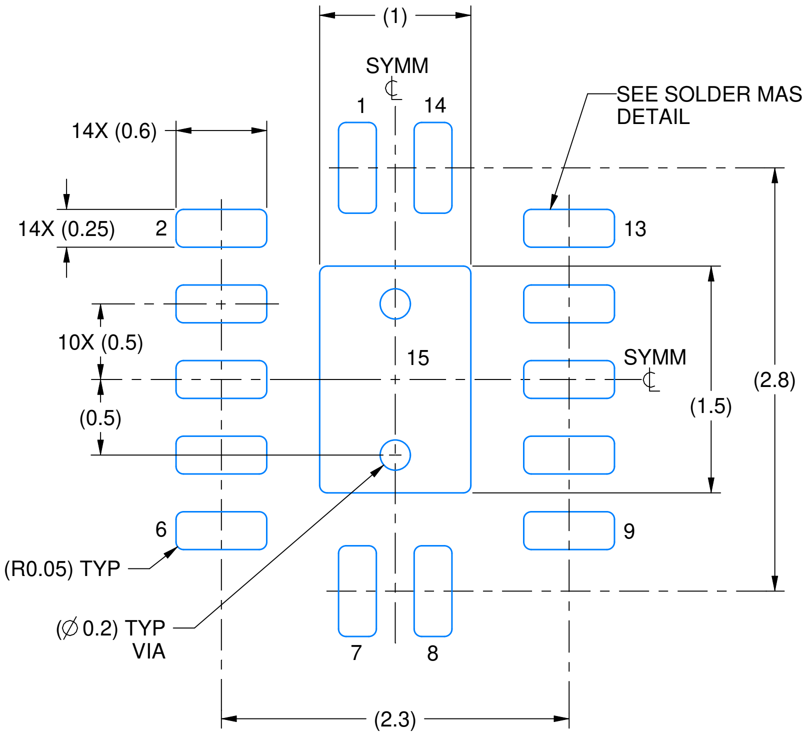
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



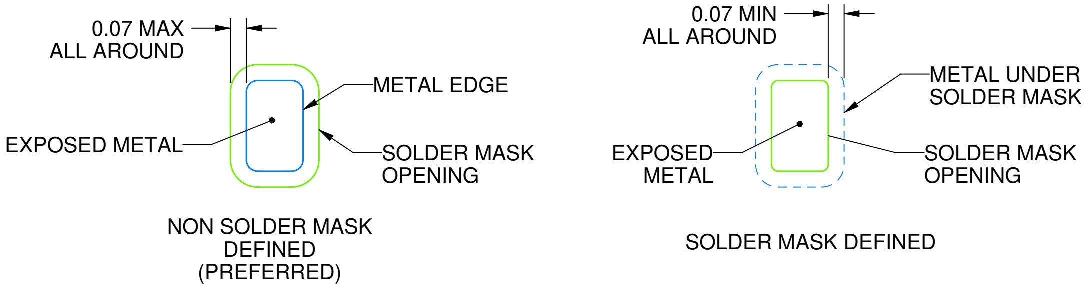

B
2.6
2.4
A
PIN 1 INDEX AREA
3.1
2.9
0.1 MIN
(0.13)
SECTION A-A
TYPICAL
0.8
0.6
C
SEATING PLANE
0.05
0.00
0.08 C
1±0.1
2X 0.5
(0.2) TYP
SYMM
7
8
EXPOSED THERMAL PAD
6
9
15
A
A
1.5±0.1
(0.16) TYP
2X 2
SYMM
8X 0.5
2
13
PIN 1 ID
14X 0.3 0.2
0.1Ⓜ C A B
0.05Ⓜ
1
14
14X 0.5 0.3
4227062/B 09/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.


(1)
SYMM
℄
1
14
SEE SOLDER MASK DETAIL
14X (0.6)
14X (0.25)
2
13
10X (0.5)
15
SYMM
℄
(2.8)
(1.5)
(0.5)
6
9
(R0.05) TYP
(∅0.2) TYP
VIA
7
8
(2.3)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X


0.07 MAX
ALL AROUND
METAL EDGE
EXPOSED METAL
SOLDER MASK OPENING
NON SOLDER MASK DEFINED (PREFERRED)
0.07 MIN
ALL AROUND
METAL UNDER SOLDER MASK
EXPOSED METAL
SOLDER MASK OPENING
SOLDER MASK DEFINED

SOLDER MASK DETAILS

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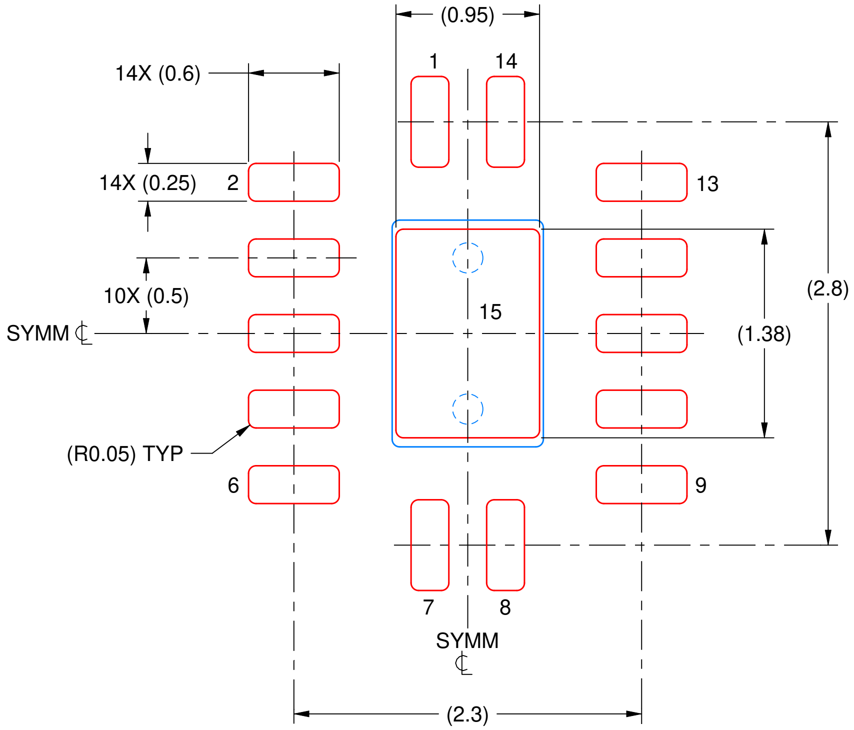
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



(0.95)
14X (0.6)
1
14
14X (0.25)
2
13
10X (0.5)
SYMM ℄
15
(2.8)
(1.38)
(R0.05) TYP
6
9
7
8
SYMM
℄
(2.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

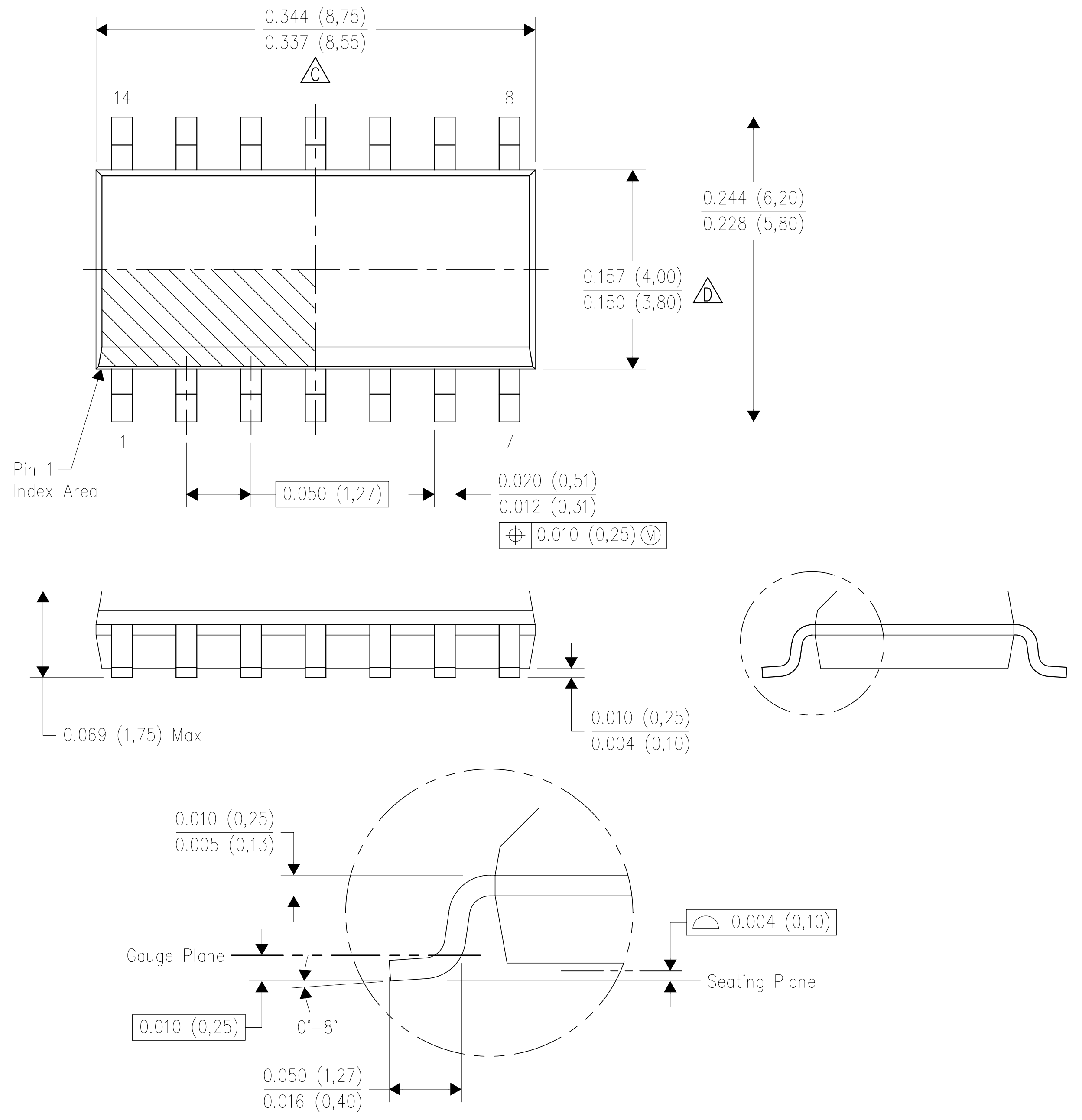
EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

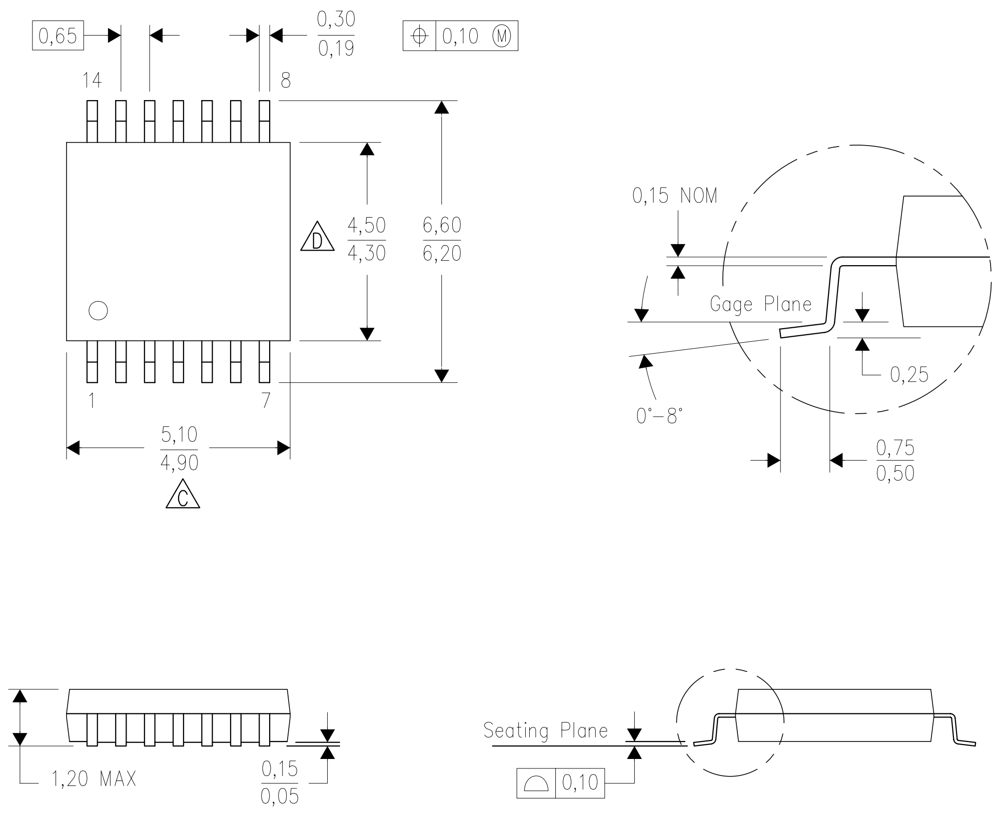
D (R–PDSO–G14) PLASTIC SMALL OUTLINE


0.344 (8,75)
0.337 (8,55)
C
14
8
1
7
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
D
Pin 1
Index Area
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
⌖ 0.010 (0,25) Ⓜ
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
⌓ 0.004 (0,10)
Seating Plane
0.010 (0,25)
0°–8°
0.050 (1,27)
0.016 (0,40)

4040047–5/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

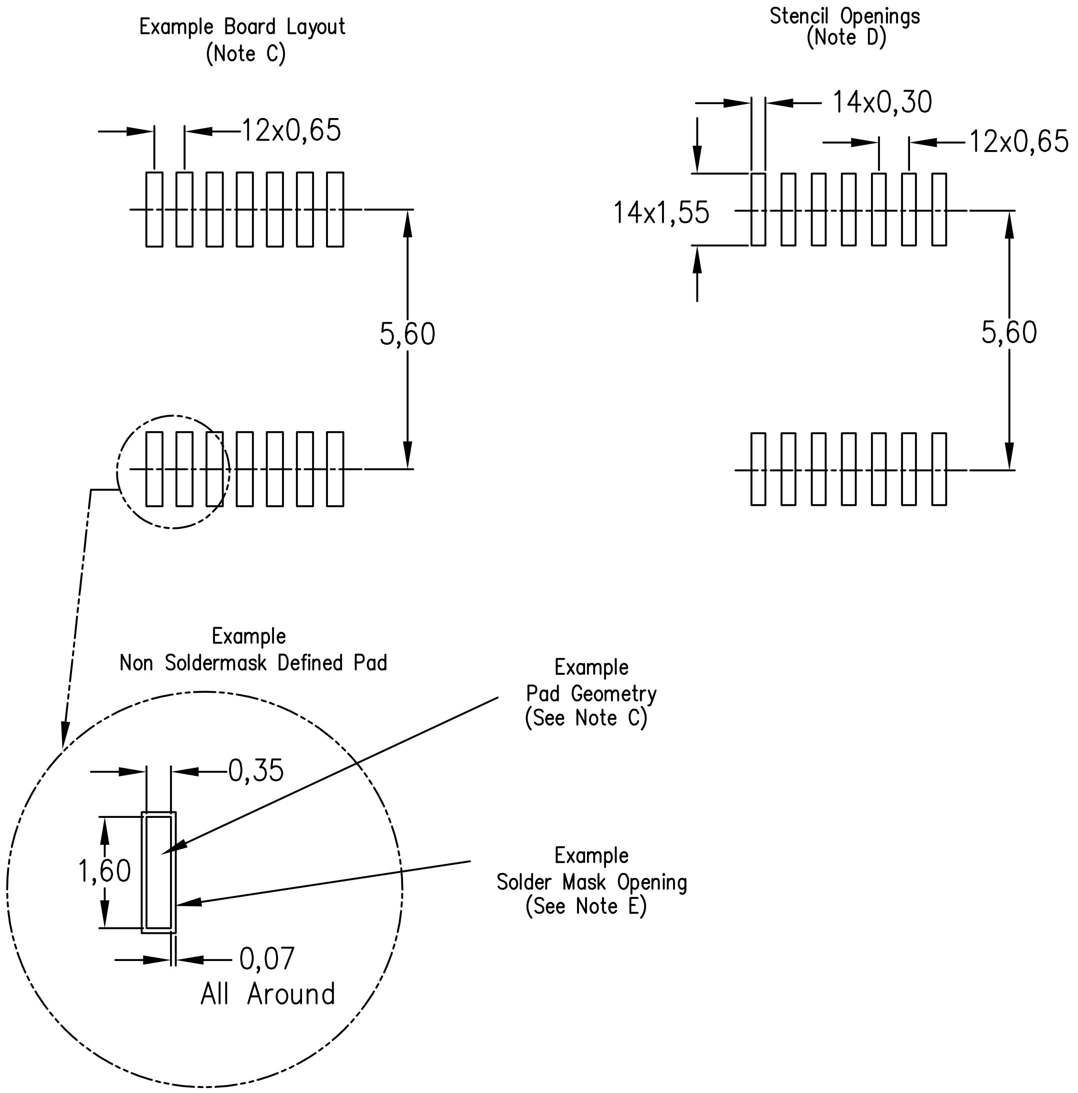
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE


0,65
0,30
0,19
⌖ 0,10 Ⓜ
14
8
1
7
D
4,50
4,30
6,60
6,20
5,10
4,90
C
0,15 NOM
Gage Plane
0,25
0°–8°
0,75
0,50
1,20 MAX
0,15
0,05
Seating Plane
⌓ 0,10

4040064–3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE


Example Board Layout
(Note C)
12x0,65
5,60
Stencil Openings
(Note D)
14x0,30
12x0,65
14x1,55
5,60
Example
Non Soldermask Defined Pad
Example
Pad Geometry
(See Note C)
0,35
1,60
Example
Solder Mask Opening
(See Note E)
0,07
All Around

4211284–2/G 08/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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