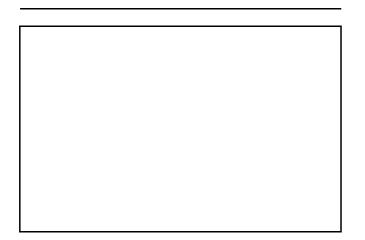
PAGE	1/10
DATE	
NO.	

Messrs.



# SPECIFICATION

## PRODUCT NAME: VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

TYPE:

CSX-750V

FREQUENCY:

MHz

PARTS NO.:

CITIZEN WATCH CO., LTD. 1-12, Honcho 6-chome, Tanashi-shi, Tokyo 188-8511 Japan

Oscillator Technical section Crystal Devices Div. Telephone: 0424-68-4572 Fax : 0424-68-4666

PRODUCTS MARKETING GROUP Telephone: 0424-67-6214 Telex:2822-471/ Fax: 0424-67-8503

APPROVED	CHECKED	PREPARED

JP	
03	

SPECIFICATION	NO.	PAGE
	DATE	2/10

I. SCOPE

This specification relates to the voltage controlled crystal oscillator to be supplied by CITIZEN WATCH CO., LTD. (following as CITIZEN) .

NOTICE

1.If something that is ambiguously defined or undefined in this specification happened, the customer and CITIZEN would discuss and take necessary steps by mutual consent.

- 2. Product test data can't be attached to this specification.
- 3. This product is not authorized for use as critical component in life support devices or systems.

#### II. SPECIFICATION

#### **1. ABSOLUTE MAXIMUM RATING**

Parameter		CSX750VB/CSX750VC
Supply Voltage	Vmax	-0.5V to +7.0V
Storage Temperature	Tstg	-45°C to +90°C
Output Current	lout	10mA Max.
Input Control Voltage	Vc_m	-0.5V to Vdd +0.5V
Solder Heat Resistance	Tsol	Max.240°C x Max.10 seconds x 2times
Of The Outer Lead		Max.200°C x Max. 3 minutes

## 2. OPERATING RANGE

Parameter		CSX750VB	CSX750VC
Supply Voltage	Vdd	3.3V±5%	5.0V±10%
Operating Temperature	Topr	-10°C to 70°C or -40°C to 85°C	
Input Control Voltage	Vc	0.0V to Vdd	
Output Load	CL	30pF Max.	

### 3. FREQUENCY CHARACTERISTICS

Parameter		CSX750VB	CSX750VC
Stability (note1)	dF0	±50ppr	m Max.
Pullability (note2)	Fpull	±90ppm Min.	±100ppm Min.
Linearity	Ldev	±15% Max.	±10% Max.
Modulation Band Width	Fmod	10kHz Min.	

note1) Frequency Stability includes initial tolerance, temperature characteristics, input voltage characteristics, load characteristics, shock, vibration, reflow and 1st year aging. note2) Vc=1.65V±1.65V (CSX750VB) Vc=2.5V±2.0V (CSX750VC)

SPECIFICATION	NO.	PAGE
	DATE	3/10

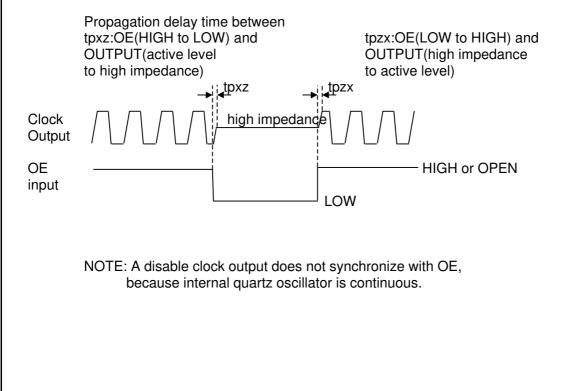
#### 4. ELECTRICAL CHARACTERISTICS (Ta=25°C load=30pF Vc=Vdd/2)

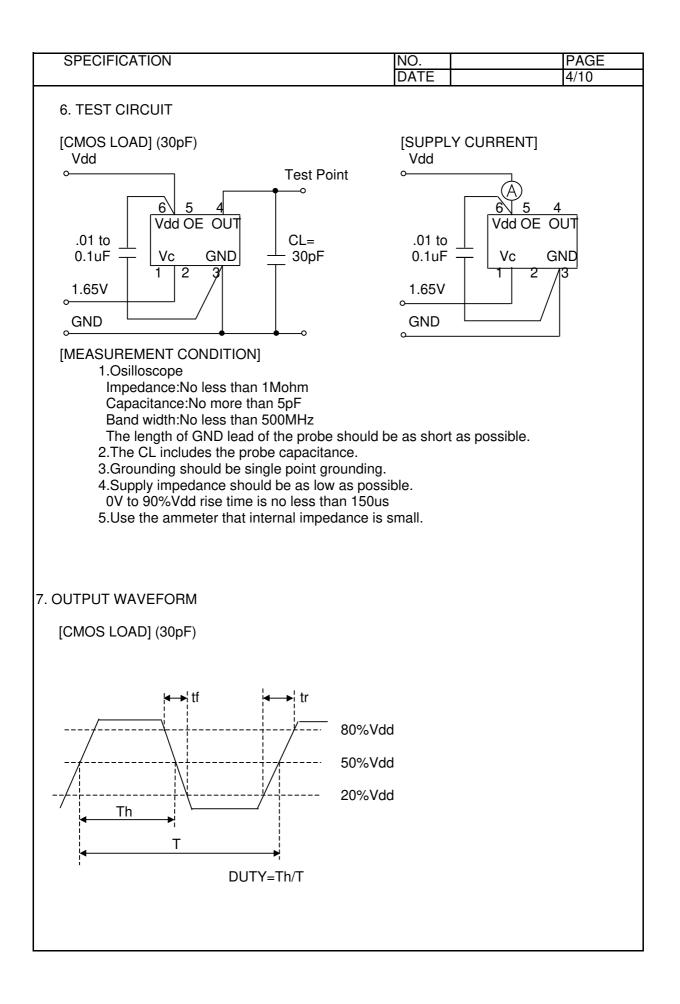
Parameter		Conditions	CSX750VB	CSX750VC
Start Up Time (note)	tosc		4msec Max.	
Power Supply Current	ldd	No Load	11mA Max.	30mA Max.
Disable Current	linh	No Load	5mA Max.	20mA Max.
Rise Time	tr	20% to 80%Vdd	5ns Max.	
Fall Time	tf	80% to 20%Vdd	5ns Max.	
Duty Cycle	duty	50%Vdd	45% to 55%	
Output HIGH Voltage	Voh	loh = -0.8mA	Vdd-0.4V Min.	
Output LOW Voltage	Vol	lol = 3.2mA	0.4V Max.	
OE Input HIGH Voltage	Vih		Vdd x 0.7 Min.	
OE Input LOW Voltage	Vil		Vdd x 0.3 Max.	
Output Disable Time	tpxz	See 5.	100ns Max.	
Output Enable Time	tpzx		100ns Max.	

note) Vc must be kept ground level or left open when starting up.

## 5. THREE STATE OUTPUT OPERATION

OE Input	Clock Output	
HIGH or OPEN	Active	enable
LOW	High impedance	disable

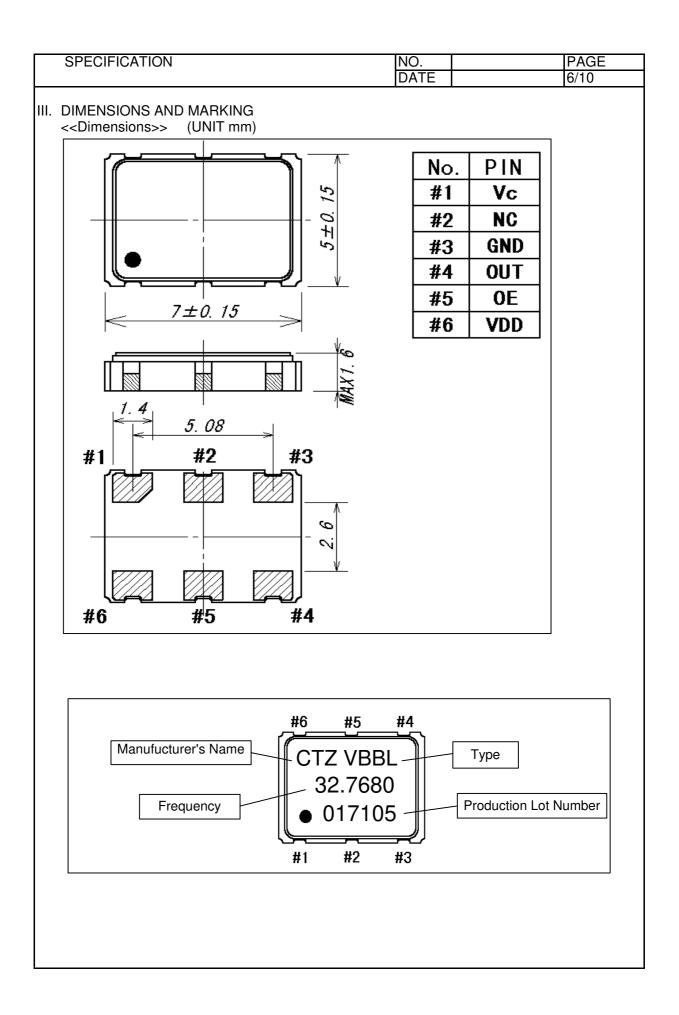


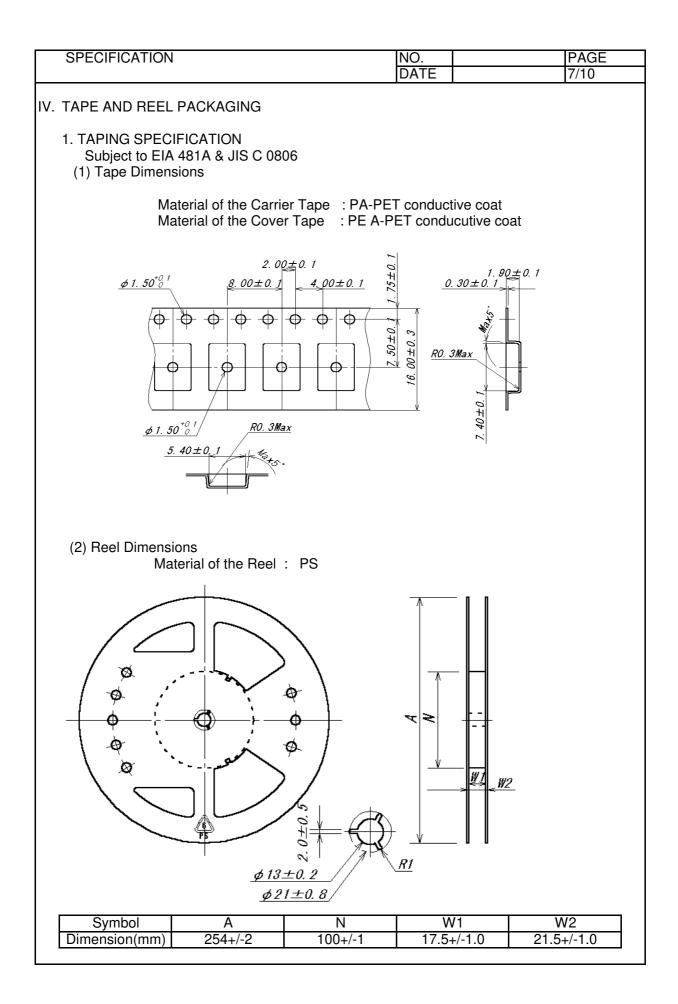


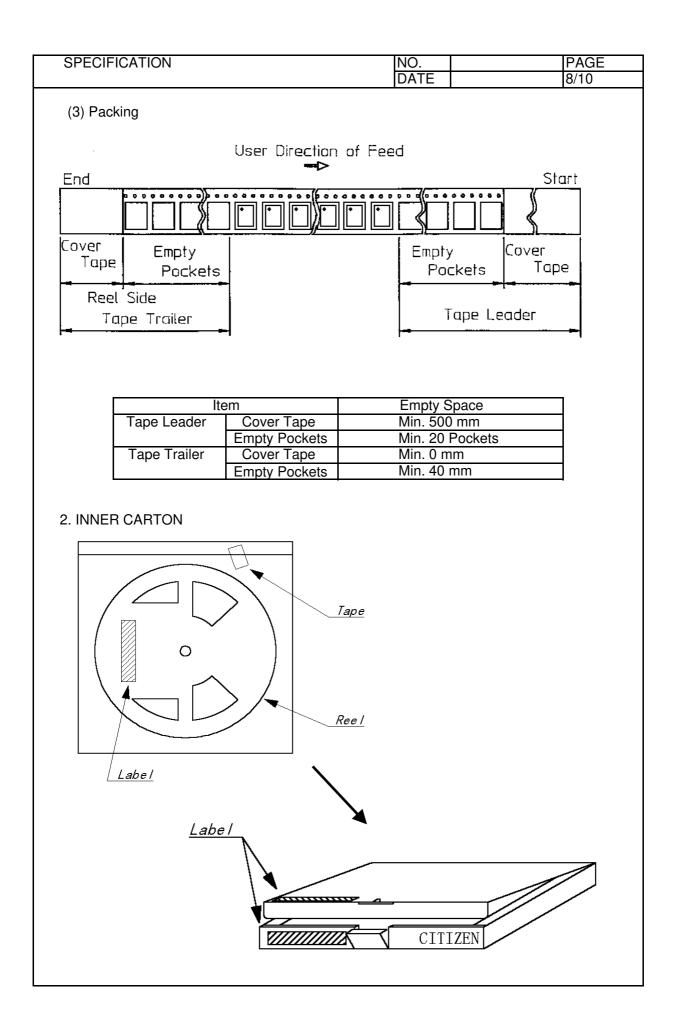
SPECIFICATION	NO.	PAGE
	DATE	5/10

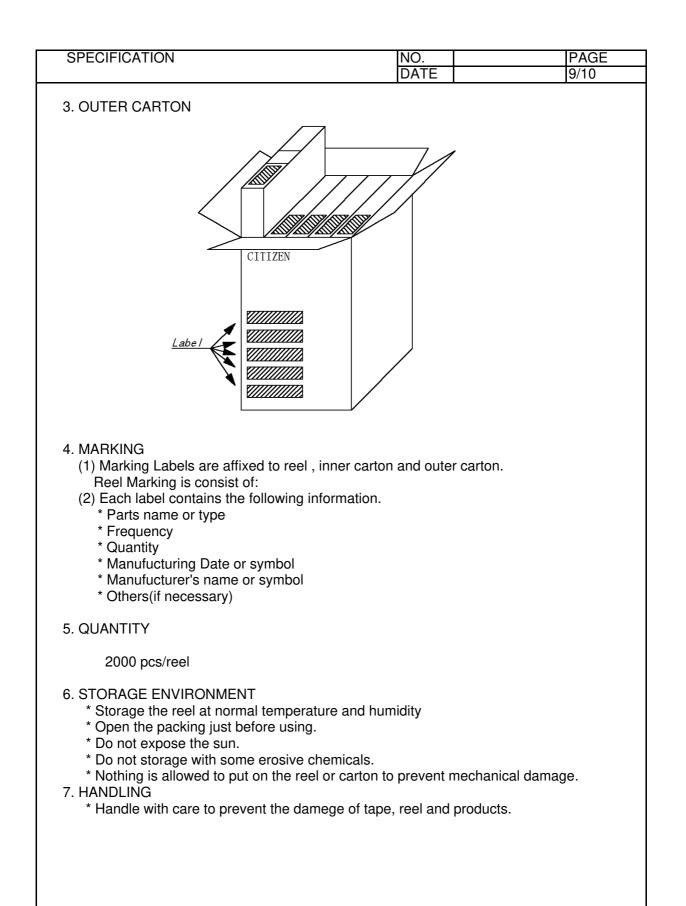
## 8. ENVIRONMENTAL AND MECHANICAL CHARACTERISTICS The following are our reliability test conditions.

Item	Conditions	
Shock	MIL-STD-883E 2002.3B	
Vibration	MIL-STD-883E 2007.2A	
Gross Leak	Leak rate less than 50ppm atm cc /sec of Air	
Fine Leak	Leak rate less than 0.01ppm atm cc /sec of Herium	









3	PECIFICATION	NO.		PAGE
		DATE		10/10
1. (E Ti	DTES HANDLING LECTROSTATIC DISCHARGES) his device is made with CMOS circuitry. Please tak o prevent damage due to electrical static discharge		ions	
(S TI Ai in	HOCK RELIABILITY) his device contains a quartz crystal, so please do n n automatic insersion is available, however, the inte case that too much shock or vibration is given by r pur machine condition in advance.	ot give too ernal quar	tz crystal might be	e damaged
Si to	LEANING) ince, depending on the cleaning conditions,there is the Crystal Osillator,do not fail to test and confirm ompany's cleaning conditions.			
W W CC	EMPERATURE AND HUMIDITY) /e recomend to store and use device under normal /hen this device is used in high humidity application ondensation. s with other IC's, please take precautions to preven	is, there is	s a potential probl	em with
(P W op	CIRCUIT DESIGNS OWER LINES) /e recomend placing a 0.01 to 0.1uF capacitor betw peration and protect against power line ripple . DD and GND pattern should be as wide as possible		and GND to obta	in stable
,	E INPUT LINE) /hen OE pin is not used, please connect it to VDD.			
À	UTPUT LINE) s a long output line may cause irregular output, plea as short as possible, and also keep high level sign			
	TARTING UP) c must be kept ground level or left open when starti	ng up.		