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NCD98010 SAR ADC Evaluation Board User Guide

March, 2020 – Rev. 0

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Introduction

The STR-NCD98010-GEVK SAR ADC evaluation board provides hardware to realize a full analog to digital signal path required to analyze the performance metrics of the NCD98010 ADC. The block diagram below shows the signal path used to capture samples from the ADC for analysis. The user's computer running the Strata Application connects to the board's USB connector for data transfer and power.

Figure 1: NCD98010 Evaluation Board

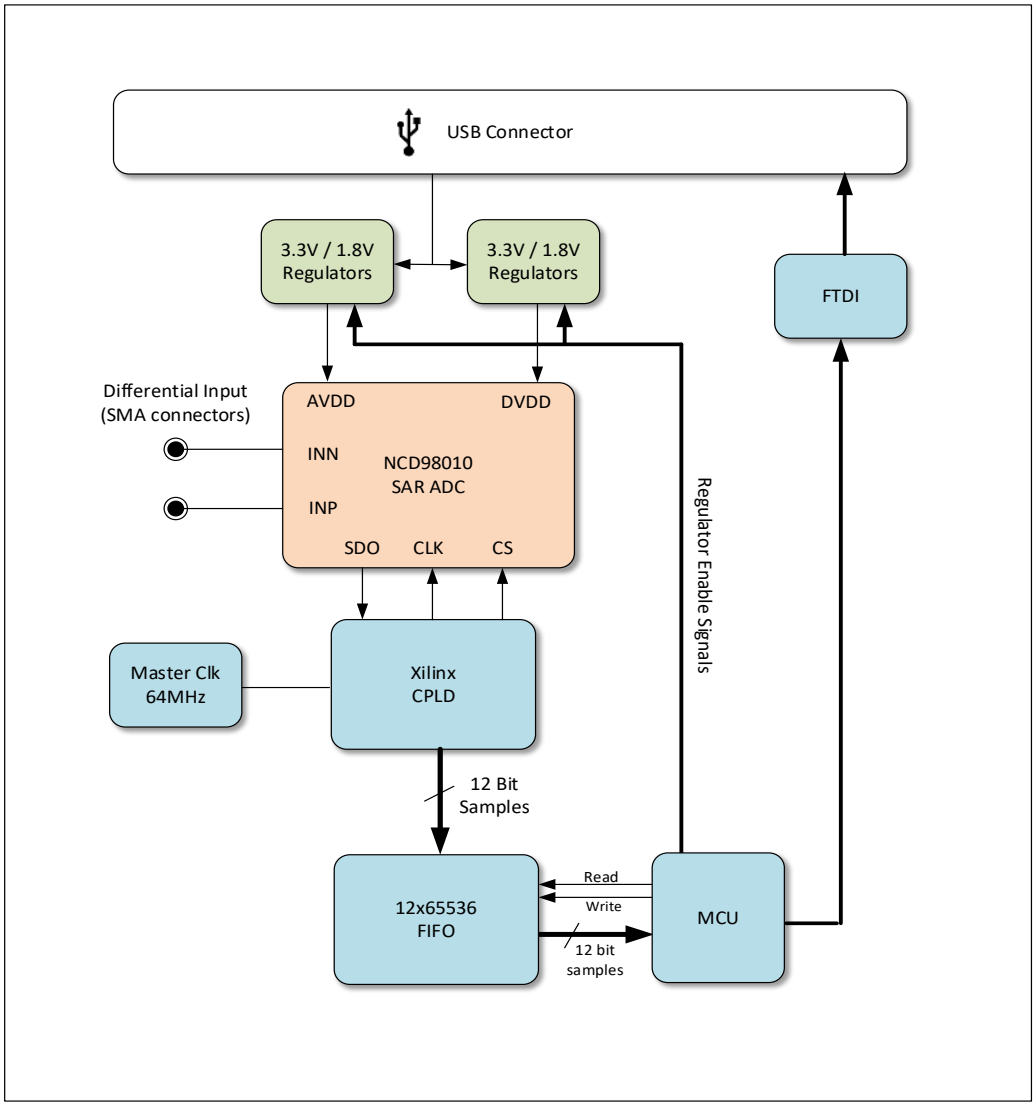

Figure 2: NCD98010 SAR ADC Evaluation Board Block Diagram

Features

12-bit Analog to Digital Conversion	• Fully Differential Input • Low 2pF Input Capacitance
Digital SPI Interface	• Available in Signed and Unsigned Output Formats
Split Analog / Digital Supplies	• Digital and Analog Supplies can be Supplied Separately from 1.65V to 3.6V
Low Power Consumption	• 7uA at 100 kSPS • Analog Current Consumption can to go down to nano-amps with Slower Clock Rates.
Small Package Size	• 1.5 x 1.5 mm 8-pin X2QFN
Pre-Calibrated	•

Applications

Low-Power Data Acquisition	• Battery-Powered Equipment • Level Sensors • Ultrasonic Flow Meters • Motor Controls • Wearable Fitness Devices • Portable Medical Equipment • Glucose Meters

Startup Procedure

1. Connect computer running the ON Semiconductor Strata Application to the evaluation board using the provided USB cable.

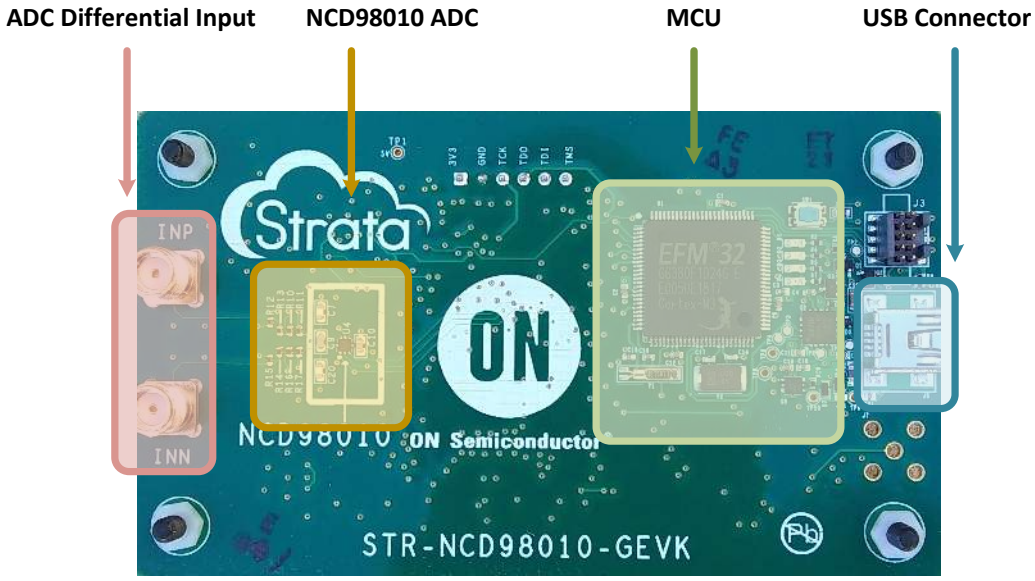

Figure 5: NCD98010 Evaluation Board Front

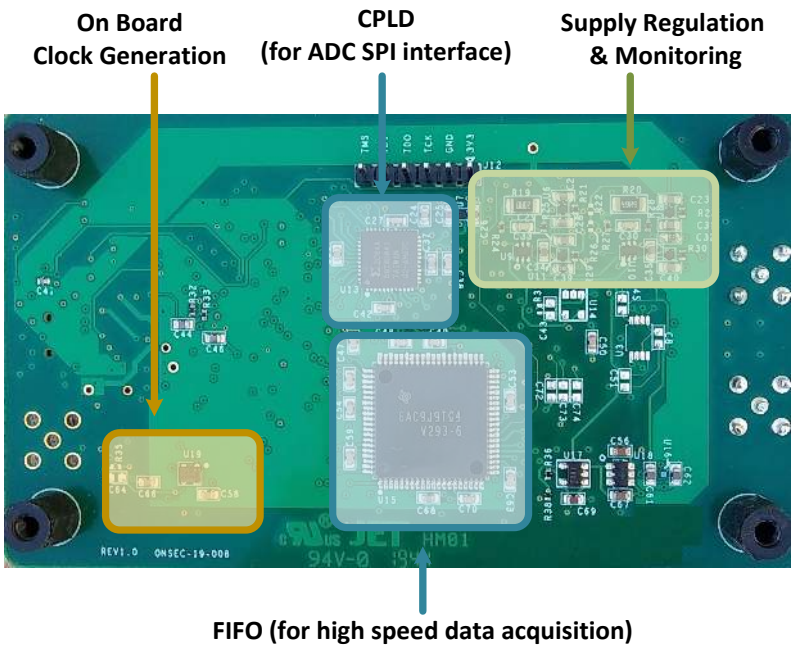

Figure 5: NCD98010 Evaluation Board Back

2. Start the Strata Application found at onsemi.com/strata.
3. Create a login.

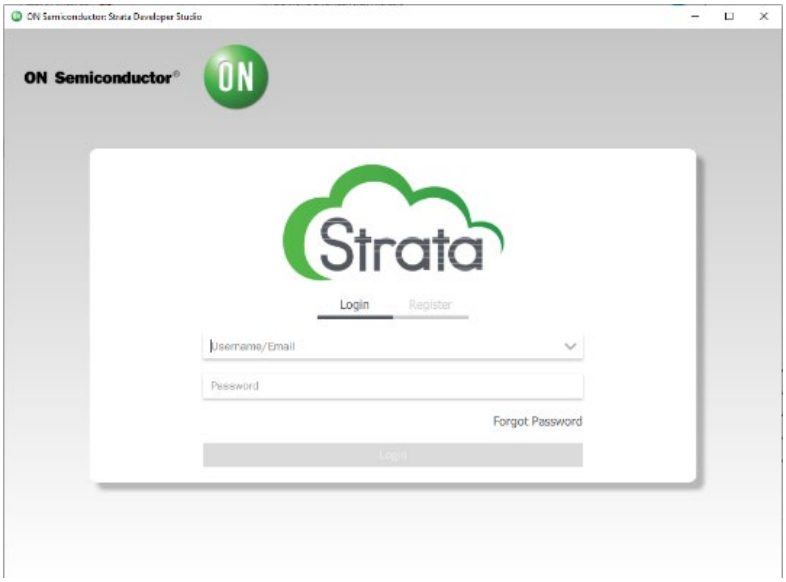

Figure 3: Strata Login Window

The Strata Application will recognize the evaluation board connected via USB and will bring up the evaluation board specific user interface. (The evaluation board can be connected after the Strata App has been launched).

4. The user interface, as shown below, allows the user to change the NCD98010 clock and supply stimuli. The clock pull down menu allows the user to choose between a number of clock rates supported by the evaluation board. 3.3V and 1.8V options are available for both AVDD and DVDD supplies. Every time the supplies or the clock are changed by the user, the power consumption measurements are updated. The power consumption measurements are most accurate when the ADC INN and INP inputs are not active. Input signals may supply AC currents that can add to or subtract from the actual ADC current.

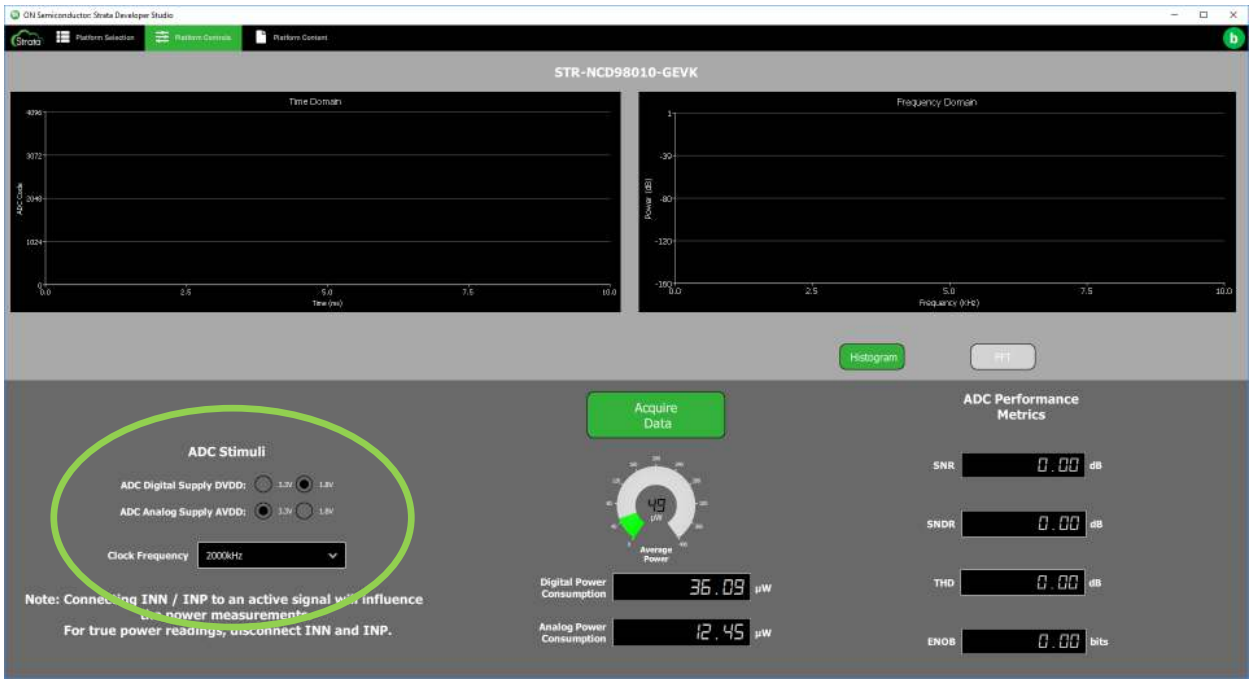

Figure 4: NCD98010 SAR ADC Strata UI Window

5. Connect the INN and INP inputs to the ADC to a signal generator. With the differential inputs active, the setup is ready to acquire data.
6. Click the “Acquire Data” button. 8,192+ samples will be collected from the ADC at the sample rate of clock/16 and loaded into the evaluation board FIFO. The contents of the FIFO will then be communicated to the Strata GUI. During this time there will be a green LED indicating this communication.

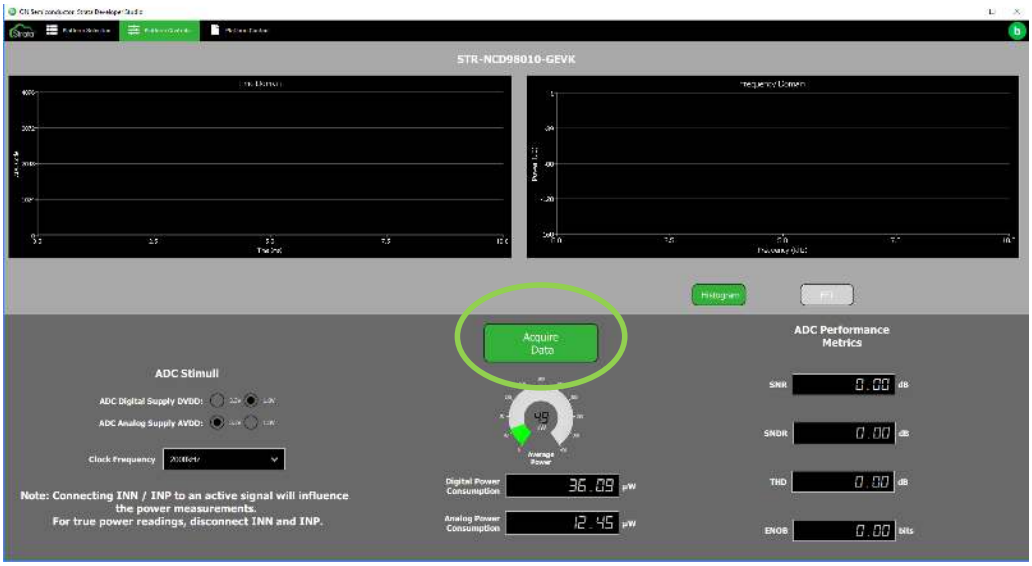

Figure 6: SAR ADC Data Acquisition Button

7. Once the data has been transmitted, the Strata GUI will analyze and plot the data. After some time, the time domain, frequency domain, and histogram plots will be populated.

Figure 7: SAR ADC UI Post Data Acquisition

Performance Considerations

The data from any differential signal connected to the ADC inputs will be shown in the time domain plot. However, the AC metrics shown on the right hand side of the user interface are best demonstrated when the differential signal has the following characteristics:

a. Single frequency, differential signal, where INN and INP inverted from one another and in sync with each other.
b. Differential input signal fundamental is less than 1/2 the Nyquist frequency, where the Nyquist frequency is defined as $F_{NYQUIST}$ = clock/32.
c. Differential input amplitude is very near the analog supply so that nearly the full range of the ADC is utilized. If 3.3V is selected for the analog supply, then the differential input amplitude should be ~3.29V peak to peak.
d. Common mode of the differential input signal should be the center of the ADC range. For a 3.3V analog supply, the common mode should be 1.65V. For a 1.8V analog supply, the common mode should be 900mV. The analog supply (AVDD) is the ADC reference voltage.
e. Input frequency should not be a multiple of the clocking frequency. If the input frequency is a direct multiple of the sampling rate, aliasing may occur, which will negatively affect performance metrics.
f. Differential input must be supplied by a low noise low jitter source. The board's anti-aliasing filter will help to remove frequency content higher than the Nyquist frequency. Any noise less than 2 MHz will pass through the input filtering and will adversely affect the ADC performance metrics.

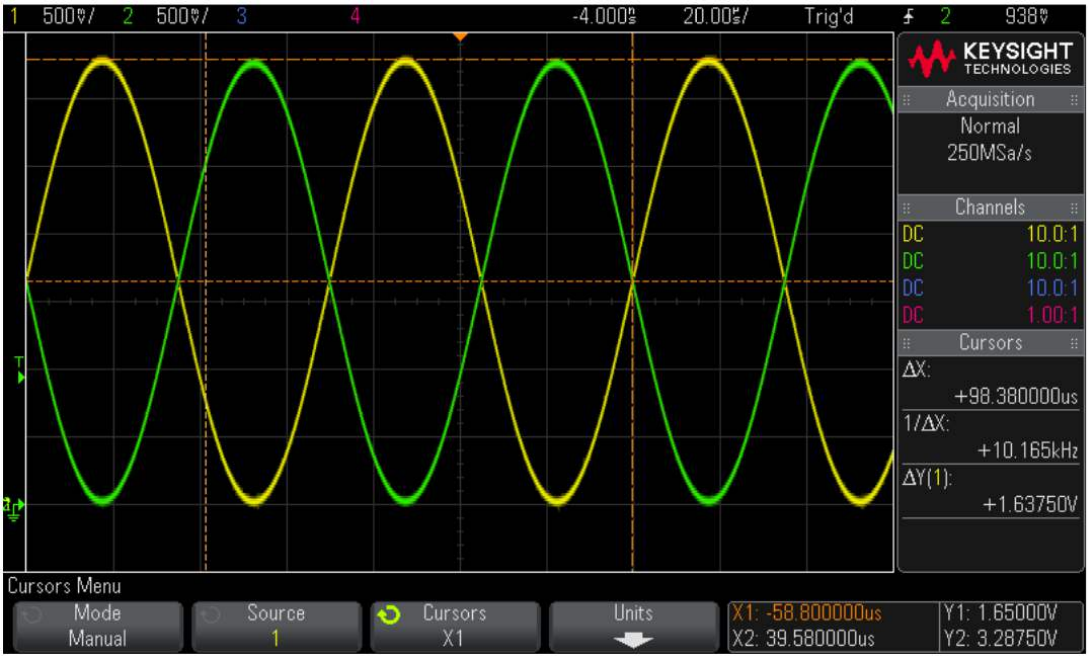

Figure 8: Sinusoidal Differential Input Signal Example

Board Options for Application Specific Development

The NCD98010 evaluation board has additional utility allowing the user to use the board for application development.

Differential Input Filtering

The noise performance of the ADC can never be better than the noise content in the differential input. For this reason, an input anti-aliasing filter is critical for good SNR performance. The evaluation board has a generic common mode filter and low pass filters on INN and INP. The values of the passives for these filters can be altered to improve the ADC performance for clock rates lower than 32 MHz. See the applications section of the NCD98010/1 datasheet for more information regarding input filtering.

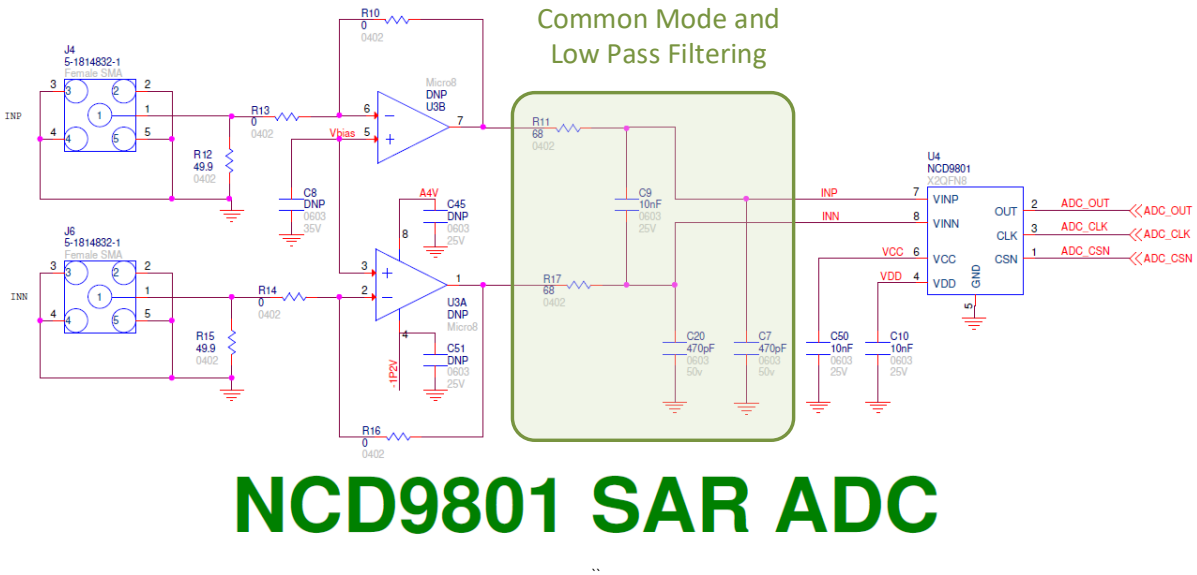

Figure 9: Differential Input Common Mode and Low Pass Filters

Differential Input Buffering

The board provides vacant spots for amplifiers on the INN and INP inputs that can be used for buffering and active filtering. This may be useful if the user is connecting the board to a very high impedance application. The board has 50Ω termination resistors from INN and INP to ground. These can be removed if the differential input source cannot drive 50Ω termination. The input impedance of the NCP98010 is extremely high, with very little input capacitance. This alleviates the need for an input buffer in most cases.

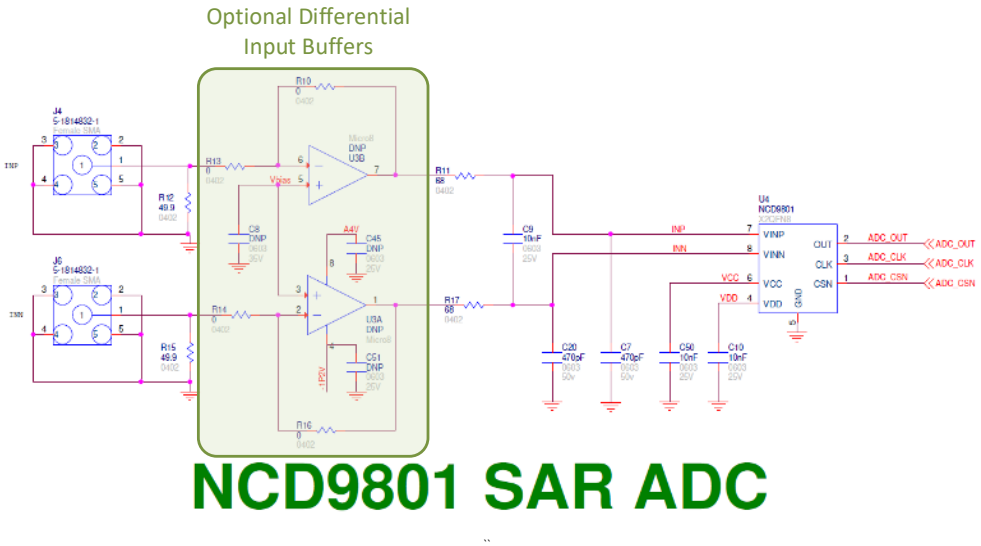

Figure 10: Optional Input Buffering

If the input buffer is populated, a location for additional circuitry for generating a common mode voltage is also provided.

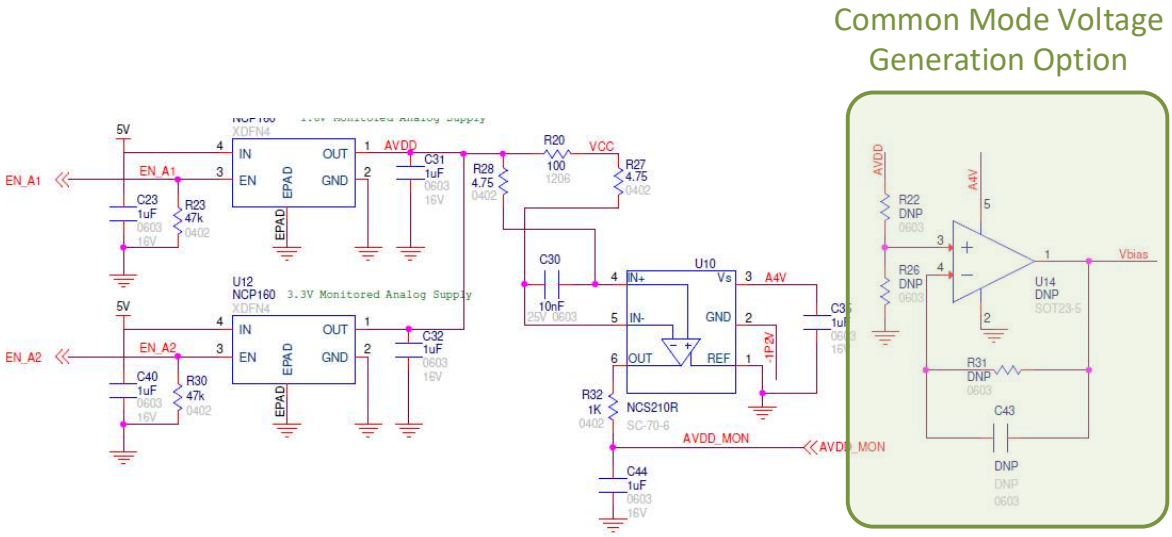

Figure 11: Optional common mode voltage generation for differential input buffers

The differential input buffers and common mode voltage generation circuitry is not populated by default.

Collateral Viewing

Click the “Platform Content” button at the top of Strata to view system content. This content always pulls from the most current documentation and allows the user to access the following documentation all in one place:

- Evaluation Board Schematic
- Evaluation Board Layout
- Evaluation Board BOM
- Test Report
- Evaluation Board Users Guide
- Block Diagram
- Demo Setup
- Part Datasheets
- Fabrication Files
- Cad Design Files

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