

MC74VHC00

Quad 2-Input NAND Gate

The MC74VHC00 is an advanced high speed CMOS 2-input NAND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

Features

- High Speed: $t_{PD} = 3.7 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8 \text{ V}$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 32 FETs or 8 Equivalent Gates
- Pb-Free Packages are Available

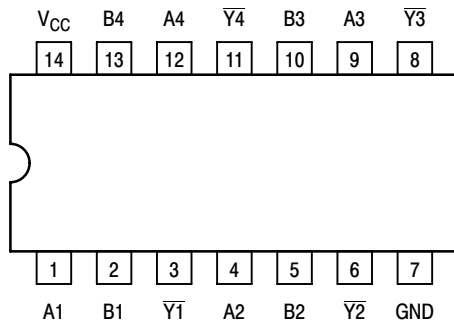


Figure 1. Pinout: 14-Lead Packages (Top View)

FUNCTION TABLE

Inputs		Output
A	B	\bar{Y}
L	L	H
L	H	H
H	L	H
H	H	L



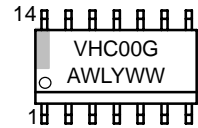
ON Semiconductor®

<http://onsemi.com>

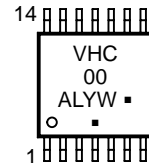
MARKING DIAGRAMS



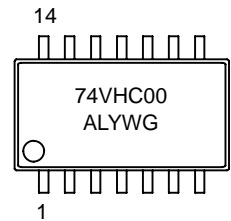
SO-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



EIAJ SO-14
M SUFFIX
CASE 965



- A = Assembly Location
- L, WL = Wafer Lot
- Y = Year
- W, WW = Work Week
- G, ■ = Pb-Free Device

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC00

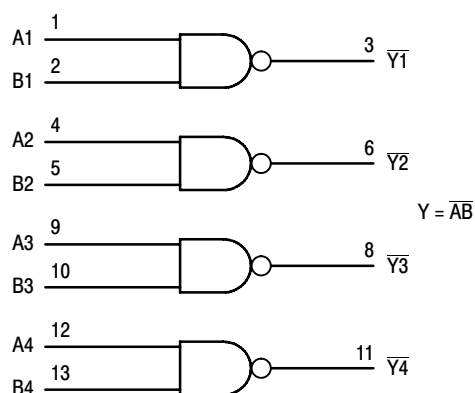


Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V_{CC}	Positive DC Supply Voltage	-0.5 to +7.0	V	
V_{IN}	Digital Input Voltage	-0.5 to +7.0	V	
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V	
I_{IK}	Input Diode Current	-20	mA	
I_{OK}	Output Diode Current	± 20	mA	
I_{OUT}	DC Output Current, per Pin	± 25	mA	
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA	
P_D	Power Dissipation in Still Air	SOIC Package 200 TSSOP 180	mW	
T_{STG}	Storage Temperature Range	-65 to +150	$^{\circ}C$	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) >2000 Machine Model (Note 2) >200 Charged Device Model (Note 3) N/A	V	
$I_{LATCH-UP}$	Latch-Up Performance	Above V_{CC} and Below GND at 125 $^{\circ}C$ (Note 4)	± 300	mA
θ_{JA}	Thermal Resistance, Junction to Ambient	SOIC Package 143 TSSOP 164	$^{\circ}C/W$	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	-55	125	$^{\circ}C$
t_r, t_f	Input Rise or Fall Time	$V_{CC} = 3.3 V \pm 0.3 V$ 0	100	ns/V
		$V_{CC} = 5.0 V \pm 0.5 V$ 0	20	

MC74VHC00

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = -40 to 85°C		T _A = -55 to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7			1.50 V _{CC} × 0.7		1.50 V _{CC} × 0.7		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V _{CC} × 0.3		0.50 V _{CC} × 0.3		0.50 V _{CC} × 0.3	V
V _{OH}	High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{OH} = - 50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{in} = V _{IH} or V _{IL} I _{OH} = - 4 mA I _{OH} = - 8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.40 3.70		
V _{OL}	Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.55 0.55	
I _{in}	Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 2.0	μA
I _{CC}	Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			2.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = -40 to 85°C		T _A = -55 to +125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, A or B to \bar{Y}	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		5.5 8.0	7.9 11.4	1.0 1.0	9.5 13.0	1.0 1.0	10 14.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		3.7 5.2	5.5 7.5	1.0 1.0	6.5 8.5	1.0 1.0	7.0 9.5	
C _{in}	Input Capacitance			4.0 10			10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 5)	Typical @ 25°C, V _{CC} = 5.0 V		pF
		19		

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per gate). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, C_L = 50 pF, V_{CC} = 5.0 V, Measured in SOIC Package)

Symbol	Characteristic	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.3	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	- 0.3	- 0.8	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

MC74VHC00

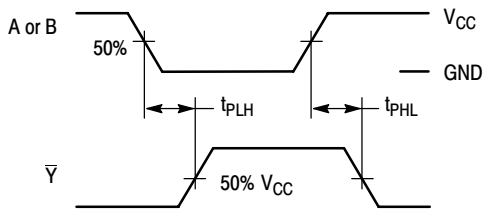
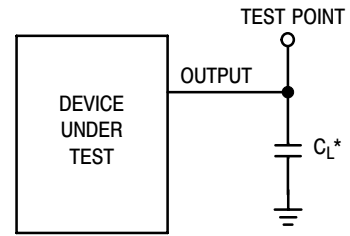


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

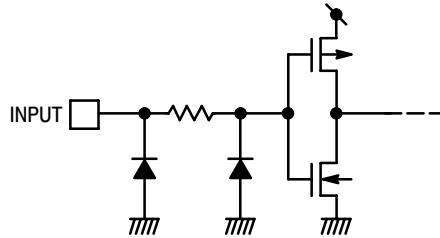


Figure 5. Input Equivalent Circuit

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74VHC00DR2	SOIC-14	2500 / Tape & Reel
MC74VHC00DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHC00DT	TSSOP-14*	96 Units / Rail
MC74VHC00DTG	TSSOP-14* (Pb-Free)	96 Units / Rail
MC74VHC00DTR2	TSSOP-14*	2500 / Tape & Reel
MC74VHC00DTR2G	TSSOP-14* (Pb-Free)	2500 / Tape & Reel
MC74VHC00MEL	SOEIAJ-14	2000 / Tape & Reel
MC74VHC00MELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel

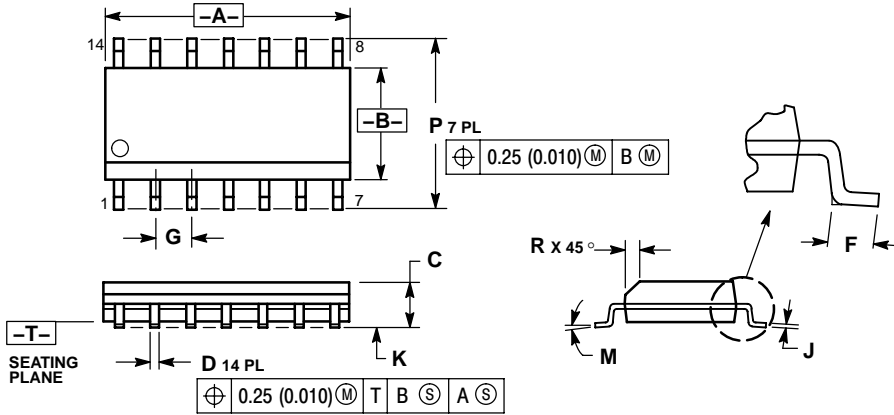
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74VHC00

PACKAGE DIMENSIONS

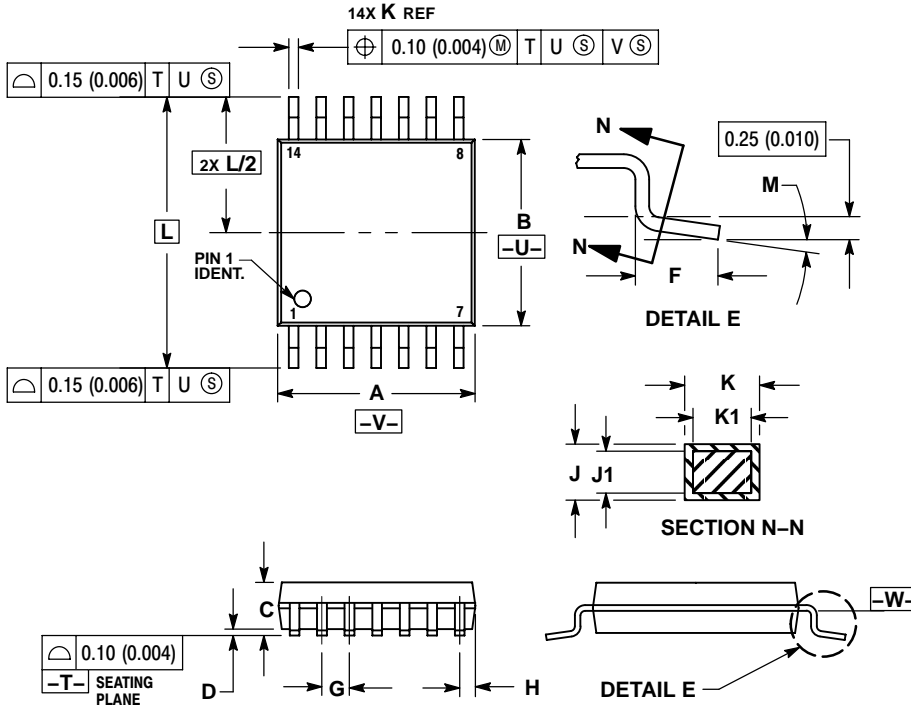
SOIC-14
CASE 751A-03
ISSUE G



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE A



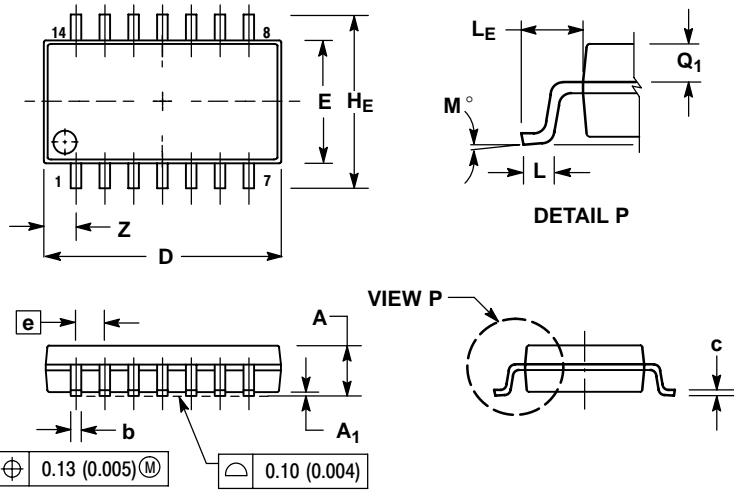
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74VHC00

PACKAGE DIMENSIONS

SO-14
M SUFFIX
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.