90 W PFC evaluation board for the IRS2505L

IRuPFC2

About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and user guide for the IRuPFC2 90 W PFC evaluation board based on the IRS2505L control IC. The scope applies to all technical aspects that concerned with the design process including calculation of external component values, MOSFET selection, PCB layout optimization as well as additional circuitry. Comprehensive test measurements and waveforms are also provided.

Intended audience

Power supply and lighting ballast design engineers, applications engineers and students.

Disclaimer

Attention: For clarity purposes, this Disclaimer must be read together with "Important Notice" and "Warnings" given on last page 36 of the document.

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It is the responsibility of the Customer to ensure that each evaluation board will be handled in a way which is compliant with all relevant requirements and standards in the country in which it is operated.

The evaluation board is only intended for use by qualified and skilled technical staff for laboratory usage and shall be used and managed according to the terms and conditions detailed in the related documentation provided with the Evaluation Board.

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The Customer agrees to indemnify and hold Infineon harmless from any third party claims in connection with or arising out of the use and/or handling of their use of Infineon evaluation boards.

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1 Introduction and specification

The IRuPFC2 demo board is a 90 W wide input range power factor correction Boost converter based on the IRS2505L controller IC. The IRS2505L is a critical conduction mode (CrCM) PFC controller IC primarily intended for front end PFC pre-regulators typically used in power supply and lighting applications up to 150 W. It may also be used in other SMPS topologies such as Buck, Buck-Boost and Flyback, which are not covered here. The IRS2505L based PFC circuit is able to meet the requirements of EN61000-3-2, including class C limits for lighting applications.

The design procedure for a PFC stage based on the IRS2505L differs slightly from the procedure used for industry standard 8 pin CrCM PFC control ICs and will be explained in detail here. In order for the circuit to produce optimum performance care must be taken to select the correct component values and ratings. The PCB must also be designed according to the correct practices for SMPS design to avoid noise susceptibility for which guidelines are provided.

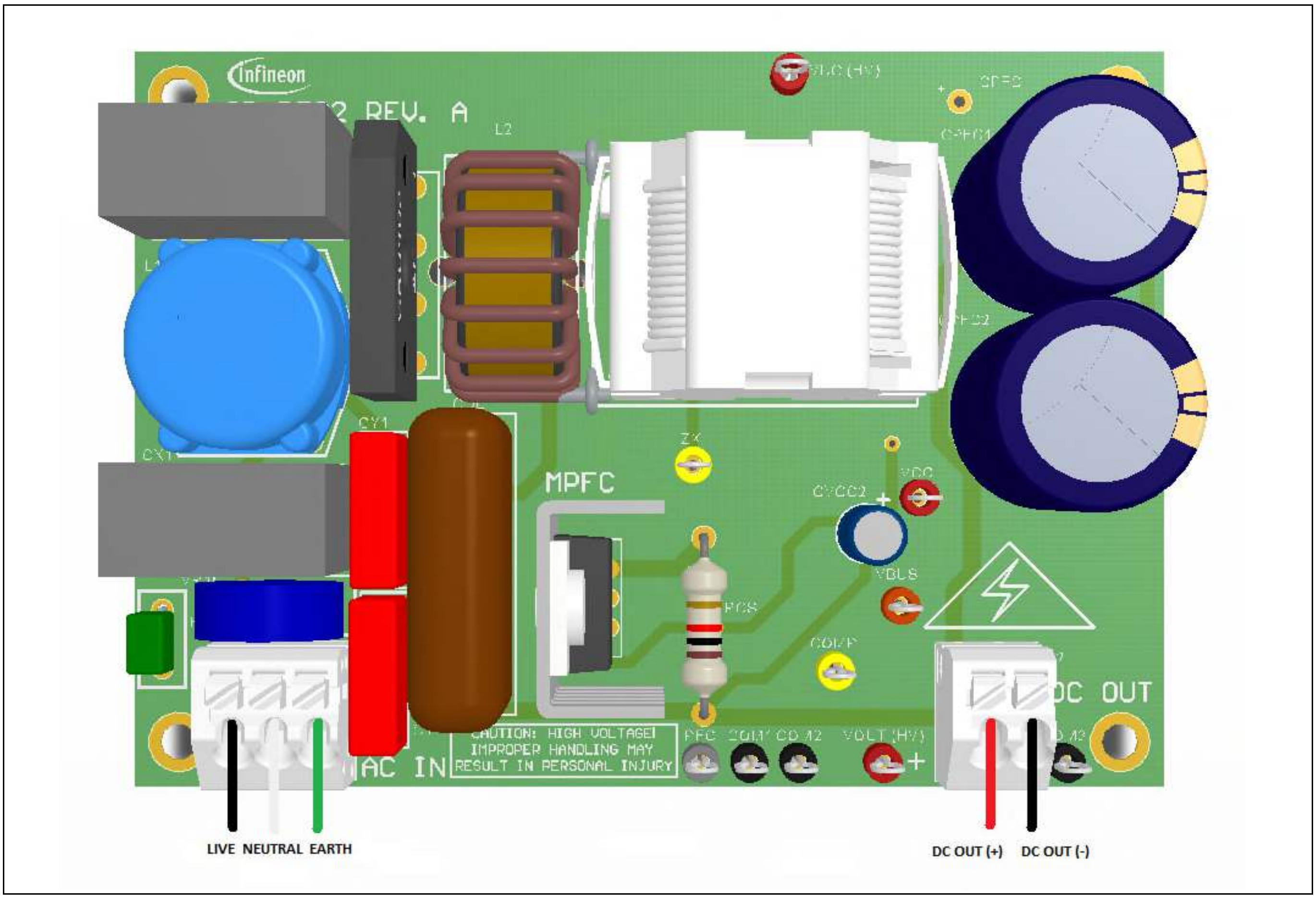
In order to save design time a simple design tool in the form of a spreadsheet is available, which calculates all of the component values based on user inputs as well as providing a simple means for designing the inductor.

Table 1 Specifications

Parameter	Description	Value	Units
VAC, min	Minimum RMS Input Voltage	90	[VAC]
VAC, nom	Nominal RMS Input Voltage	230	[VAC]
VAC, max	Maximum RMS Input Voltage	265[1]	[VAC]
VBUS	Nominal Bus Voltage	420[2]	[VDC]
POUT	Max Output Power	90	[W]
PF	Power Factor	>0.9	
THDi	Total Harmonic Distortion, Current	<10	[%]
η	Power Efficiency (at full load)	>93	[%]
Dimensions	3.5” (89 mm) x 2.5” (64 mm) x 1.1” (28 mm) maximum		

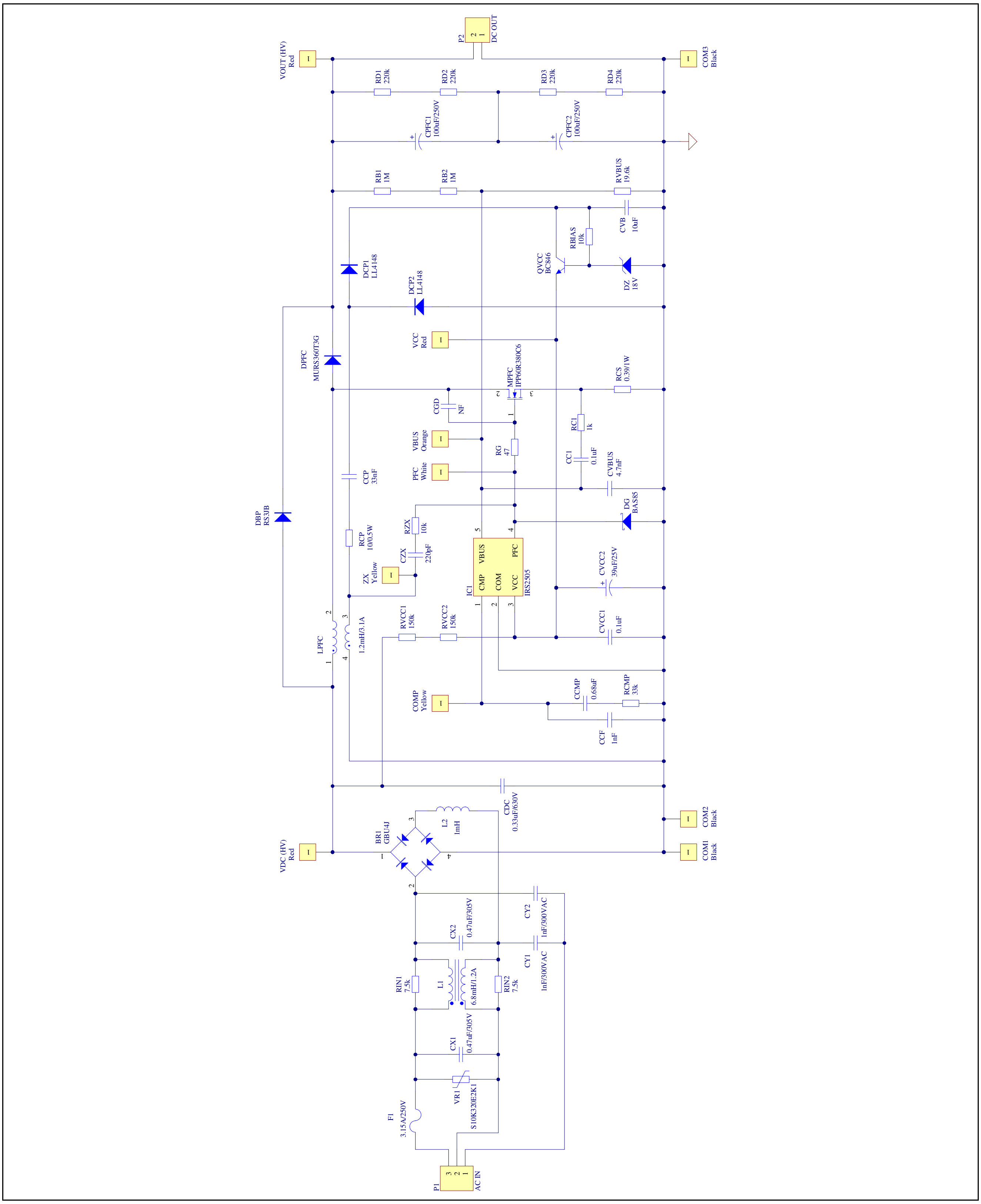
[1] The IRuPFC2 evaluation board is designed to withstand input voltage up to 305 VAC and output up to 500 VDC. However, it is necessary to set the output voltage to 475 V to use this board with input voltage above 265 VAC.
WARNING – The evaluation board will not function correctly and may become damaged if the difference between the input *peak* voltage and the output voltage is less than 40 V.

[2] The output voltage may be adjusted by changing the value of one resistor (RVBUS), please refer to section 3.3 for instructions on how to determine the value for the desired output voltage.



Board connections

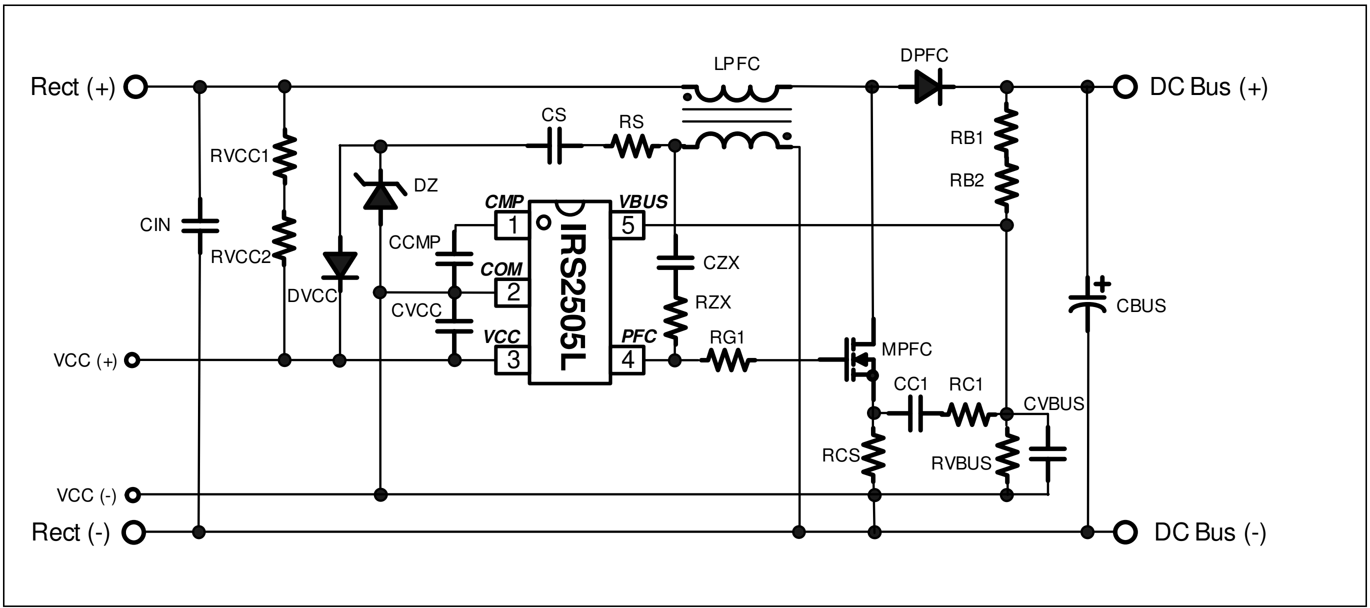
2 Circuit schematic



IRuPFC2 circuit schematic

3 Dimensioning

The main components in the schematic are shown in the following figure:



IRS2505 Boost PFC pre-regulator key components

3.1 VCC supply

The VCC supply for the IRS2505L is initially derived from the rectified voltage at the input bridge rectifier positive terminal (VRECT+) through two series resistors, RVCC1 and RVCC2. Two resistors are needed in order to properly withstand the high voltage between the bridge rectifier output and VCC.

An auxiliary winding on the PFC inductor (LPFC) is used in conjunction with the charge pump circuit made up of RS, CS, DZ and DVCC, to supply VCC during circuit operation. The auxiliary supply takes over supplying VCC when the converter starts switching.

The start up resistor values are selected based on a tradeoff between lowest dissipation at maximum AC line input voltage and minimum start up time at minimum AC line voltage. The maximum power dissipation in each resistor during normal running (not startup) is given by:

$$P_{RVCC1} = P_{RVCC2} = \frac{\left(VAC_{MAX(RMS)} - VCC\right)^2}{2 \cdot (R_{VCC1} + R_{VCC2})} \quad \text{[W]} \qquad [1]$$

In this example RVCC1 and RVCC2 are 150 k giving a power dissipation of 107 mW.

Before calculating the start up time the value of the VCC hold up capacitor (CVCC2) must be known. CVCC2 must be sufficiently large to supply the PFC circuit long enough for the auxiliary supply to take over before VCC discharges below VCCUV-. A value of 39 µF is used in this example. The start up time is then calculated according to:

$$t_{START} = \frac{c_{VCC} \cdot VCCUV^{+}}{\left(\frac{\sqrt{2} \cdot VAC_{MIN(RMS)} - \frac{VCCUV^{+}}{2}}{RVCC1 + RVCC2}\right) - \frac{IQCCUV}{2}} \quad [s] \quad [2]$$

Equation 2 accounts for the effect of CIN and CBUS, which means that before startup VRECT+ will be a smoothed DC voltage of √2 times VACMIN(RMS), which becomes full wave rectified only after the converter has started switching. The values of VCCUV+ and IQCCUV can be obtained from the IRS2505L datasheet.

$$\frac{39 \cdot 10^{-6} \cdot 11.1}{\left(\frac{\sqrt{2} \cdot 90 - \frac{11.1}{2}}{150 \cdot 10^{3} + 150 \cdot 10^{3}}\right) - \frac{60 \cdot 10^{-6}}{2}} \approx 1.2\ s$$

After startup VCC is supplied through the auxiliary winding by means of a charge pump consisting of PCP, CCP, DCP1 and DCP2 which charge CVB. The charge pump circuit has been used rather than a single diode in either polarity because this maintains a stable voltage at CVB, which varies very little with line and load. A basic linear regulator consisting of QVCC, DZ and RBIAS has been included to prevent VCC from exceeding 18V, which avoids possible over stress of the IRS2505L.

3.2 Inductor calculation

The PFC inductor is calculated to produce an off time of 15 µs at the peak of the AC line at nominal line input voltage, which has been selected as 230 VAC. This provides optimum THD reduction where it is most needed in the 220-230 VAC range. The IRS2505L introduces on time modulation to compensate for cross over distortion when the off time falls below 7 µs. This means that with the correct value of LPFC the on time modulation will begin to take effect as the line voltage drops from the peak and approaches the zero crossing. The on time is thereby increased as needed to compensate for the cross-over distortion which causes THD degradation at high line in PFC circuits. The desired inductance is calculated from the following formula:

$$LPFC = \frac{15 \cdot 10^{-6} \cdot \left(VBUS - \sqrt{2} \cdot VAC_{NOM(RMS)}\right) \cdot VAC_{NOM(RMS)} \cdot \eta}{2\sqrt{2} \cdot POUT} \quad [H] \quad [3]$$

$$\frac{15 \cdot 10^{-6} \cdot \left(420 - \sqrt{2} \cdot 230\right) \cdot 230 \cdot 0.95}{2\sqrt{2} \cdot 90} = 1.2\ mH$$

The peak inductor current is then calculated from:

$$IPFC_{MAX} = \frac{2\sqrt{2} \cdot POUT}{VAC_{MIN} \cdot \eta} \quad [A] \quad [4]$$

$$IPFC_{MAX} = \frac{2\sqrt{2} \cdot 90}{90 \cdot 0.95} = 2.98\ A$$

The current sense resistor (RCS) is then calculated:

$$RCS = \frac{2 \cdot V_{BUSOC}}{IPFC_{MAX}} \quad [\Omega] \quad [6]$$

$$RCS = \frac{2 \cdot 0.56\ V}{2.98\ A} = 0.38\ \Omega$$

The closest preferred value of 0.39 Ω has been used.

3.3 Voltage feedback and loop compensation

The DC output bus voltage is regulated using a resistor divider to provide feedback to the error amplifier through the VBUS input. The cycle by cycle current sense signal is also superimposed onto this DC voltage however this can be ignored for the purposes of calculating the voltage divider. The internal reference for the error amplifier VBUSREG is nominally 4.1 V in the IRS2505L. The resistor divider values are calculated as follows where two equal series resistors RB1 and RB2, are used for the upper branch of the divider:

RB1 and RB2 are selected as 1 MΩ for minimal power dissipation:

$$P_{RB1} = P_{RB2} \approx \frac{V_{BUS}^2}{2 \cdot (R_{B1} + R_{B2})} \quad [W] \quad [7]$$

$$P_{RB1} = P_{RB2} \approx \frac{420^2}{2 \cdot (1 \cdot 10^6 + 1 \cdot 10^6)} \approx 44\ mW$$

Therefore:

$$R_{VBUS} = \frac{VBUSREG \cdot (R_{B1} + R_{B2})}{VBUS - VBUSREG} \quad [\Omega] \quad [8]$$

$$R_{VBUS} = \frac{4.1 \cdot (1 \cdot 10^6 + 1 \cdot 10^6)}{420 - 4.1} = 19.7\ k\Omega$$

Important Note – For higher input voltage requirement:

Some applications require a higher input voltage input. The IRuPFC2 evaluation board is designed to accept input voltage up to 305 VAC, however the output voltage must be set to a higher level. For 305 VAC maximum input, the output (VBUS) should be set to 475 V, RVBUS then becomes 17.4 kΩ.

In order for the converter to provide high power factor and low THD the loop response must be slow enough that the on time remains effectively constant (except for on time modulation) throughout each line frequency half cycle. Since the AC line frequency is 50-60 Hz the error amplifier gain has to roll off at a lower frequency. The recommended value for this cut off frequency (or bandwidth) is 20 Hz to give the acceptable loop response without degrading the power factor. The loop speed is determined by the compensation capacitor CCMP whose value is calculated from the transconductance of the error amplifier g_m (approximately 100 $\mu\Omega^{-1}$) as follows:

$$C_{CMP} = \frac{g_m}{2\pi \cdot f_c} = \frac{100}{2\pi \cdot 20} = 0.796 \qquad [\mu F] \qquad [9]$$

A CCMP value of 0.68 µF is used in the IRuPFC2 evaluation board combined with a 33 k series resistor (RCMP) and a 1 nF (CCF) capacitor parallel to both. The series resistor enables VCOMP to jump almost instantly to approximately 1 V when VCC first crosses VCCUV+, which reduces the time required for CCMP to charge above VCMPON to enable the gate drive. This reduces the time during which VCC is supplied through CVCC before the auxiliary winding can provide current as discussed in section 3.1.

The compensation network discussed changes the frequency response of the error amplifier introducing a zero at 7.1 Hz and a pole at 4.8 kHz, while maintaining a gain of approximately 10 dB between these two frequencies. This has the effect of reducing settling time at start up or after a change in line or load.

3.4 Output capacitor calculation

The output bulk capacitor (CBUS) can be a single capacitor rated at 450 V for nominal output voltages up to 410 V, or two 250 V rated capacitors in series for higher output voltages. This ensures that under startup and transient conditions the output voltage will not exceed the maximum voltage ratings. If two series capacitors are used each must have approximately twice the calculated value of CBUS. This value can be calculated according to:

$$C_{BUS} = \frac{P_{OUT}}{2 \cdot \pi \cdot f_{IN(MIN)} \cdot \Delta_{RIPPLE} \cdot V_{BUS}^2} \qquad [F] \qquad [13]$$

Where $f_{IN(MIN)}$ is the minimum line input frequency (set at 50 Hz in the spreadsheet) and Δ_{RIPPLE} is the fraction of VBUS acceptable as peak to peak ripple amplitude. This should not exceed 16 % to avoid false triggering of the over voltage protection. In this case a value of 0.036 is used corresponding to 15 Vpp.

$$\frac{90}{2 \cdot \pi \cdot 50 \cdot 0.036 \cdot 420^2} = 45\ \mu F$$

In this design the output voltage is 420 V therefore two series output capacitors of 100 µF rated at 250 V have been used to provide 50 µF, alternatively a single 47 µF, 450 V rated capacitor could be used.

3.4 ZX triggering

The IRPuPFC2 nominal output voltage is 420 V and the maximum line input voltage is 265 Vrms with a peak value of 375 V. This leaves a headroom of 45 V, which is not sufficient to guarantee ZX triggering at high line. For this reason a series resistor and capacitor (RZX and CZX) have been added from the auxiliary winding to the gate drive output to inject some additional current to pull the gate voltage down below the ZX trigger threshold VPFCZX- under all conditions. The values of RZX and CZX have been determined empirically by bench testing.

The IRuPFC2 evaluation board test results shown in the following sections meet all specified parameters, providing a high power factor and very low THD of the line current over a wide range of input voltage.

The design tool produces the outputs shown in tables 3 and 4, based on the following inputs:

Table 2 Design tool inputs

Parameter	User Input Value	Units	Description
VAC_nom	230	Vrms	Nominal r.m.s. input voltage
VAC_min	90	Vrms	Minimum r.m.s. input voltage
VAC_max	265	Vrms	Maximum r.m.s. input voltage
VBUS	420	VDC	DC bus voltage (RED indicates insufficient headroom without additional ZX trigger network)
Max pp Ripple	15	Vpp	Pk-Pk output voltage ripple (RED indicates too high)
POUT	90	W	Output power

Table 3 Boost circuit calculations

Parameter	Calculated Value	Units	Description
I_LPFC_max	3.0	Apk	Maximum peak inductor current at VAC_min
LPFC	1.2	mH	PFC inductance value
f_min(nom)	52	kHz	Minimum switching frequency at VAC_nom
f_min(min)	24	kHz	Minimum switching frequency at VAC_min
Cout	45.5	uF	Output capacitor

Table 4 IRS2505L VCC supply

Parameter	Calculated Value	Units	Description
CVCC2	0.1	µF	VCC filter capacitor value (fixed)
CVCC1 MIN	39.1	µF	VCC capacitor minimum value to startup
CVCC1	39	µF	VCC capacitor value (user input value) (RED indicates value too small!)
RVCC1	150	kΩ	VCC start-up resistor no. 1 (user input)
RVCC2	150	kΩ	VCC start-up resistor no. 2 (user input)
PRVCC	0.105	W	VCC start resistor highest dissipation

Parameter	Calculated Value	Units	Description
t_startup	1.25	s	VCC start-up time at VAC_min

A CVCC1 value of 39 µF was selected since this only very slightly less than the calculated minimum value to minimize switch on delay.

Table 5 Inductor design

Inductor Parameter	Value	Unit	Comments
Core Selected:	QP2520		Core specs can be found in the manufacturer's datasheet
Effective area (Ae)	118	mm2	
Effective length (le)	50.2	mm	
Core factor Σ(l/A)	0.425	mm-1	
Fill Factor	0.4		Typically 0.7, varies between 0.3-0.7 depending on core
Air Gap	1.5	mm	Select an airgap that gives BMAX between 0.25-0.30
BMAX	0.28	T	Bmax <= 0.3T -- OK
Primary Turns (Np)	112		

Table 6

This gives a good first approximation, however the values here will not exactly match the values given by the real inductor since fringing effects around the gap are not taken into account.

4 Bill of materials

Designator	Part Number	Quantity	Value/Rating	Manufacturer
BR1	GBU4J-E3/51	1	600 V/4 A	Vishay
CC1, CVCC1	C2012X7R1H104K085AA	2	0.1 uF/50 V/0805/10%	TDK
CCF	C2012X7R2E102K085AA	1	1 nF/250 V/0805/10%	TDK
CVBUS	C2012X7R2E472K085AA	1	4.7 nF/250 V/0805/10%	TDK
CCMP	C2012X7R1E684K125AB	1	0.68 uF/25 V/0805/10%	TDK
CCP	C3216CH1H333K085AA	1	33 nF/50 V/1206/10%	TDK
CDC	ECQ-E6334JF	1	0.33 uF/630 V/5%	Panasonic
CGD		N/F	<TBD>pF/500 V/1206/10%	TDK
COM1, COM2, COM3	5001	3	0.04" dia black	Keystone
COMP, ZX	5004	2	0.04" dia yellow	Keystone
CPFC1, CPFC2	UCY2E101MHD1TN	2	100 uF/250 V/20%	Nichicon
CVB	C3216X5R1H106K160AB	1	10 uF/50 V/1206/10%	TDK
CVCC2	EEU-FC1E390	1	39 uF/25 V	Panasonic
CX1, CX2	B32922C3474M	2	0.47 uF/305 VAC/X2	Epcos
CY1, CY2	VY2102M29Y5US63V7	2	1 nF/300 VAC/Y	Vishay
CZX	CGA4C2C0G2A221J060A A	1	220 pF/100 V/0805/5%	TDK
DBP	RS3JB-13-F	1	600 V/3 A/SMB	Diodes Inc
DCP1, DCP2	LL4148-13	2	75 V/0.15 A/MINIMELF	Diodes Inc
DG	BAS85-GS08	1	Schottky/30 V/200 mA /SOD80	Vishay
DPFC	MURS360T3G	1	600 V/3 A Fast Recovery Diode	ON Semi
DZ	BZV55C18-TP	1	18 V/0.5 W/MINIMELF	Micro Commercial Co
F1	0698Q3150-02	1	350 VAC/3.15 A	Bel Fuse Inc
IC1	IRS2505L	1	PFC Control IC	Infineon
L1	B82721A2122N20	1	6.8 mH/1.2 A/Horiz	Epcos
L2	2124-V-RC	1	1 mH/1.3 A	Bourns
LPFC		1	1.2 mH/3.1 A/QP2520H 120:10	Yujing
MPFC	IPP60R380C6	1	600 V/10.6 A/TO-220	Infineon
P1	1985205	1	3 Position 3.5 mm Green	Phoenix Contact
P2	1985195	1	2 Position 3.5 mm Green	Phoenix Contact
PFC	5002	1	0.04" dia white	Keystone
QVCC	BC846B	1	65 V/0.1 A/NPN/SOT-23	Micro

Designator	Part Number	Quantity	Value/Rating	Manufacturer
				Commercial Co
RB1, RB2	ERJ-8GEYJ105V	2	1 M/0.25 W/1206/5 %	Panasonic
RBIAS, RZX	ERJ-6GEYJ103V	2	10 k/0.125 W/0805/5 %	Panasonic
RC1	ERJ-6GEYJ102V	1	1 k/0.125 W/0805/5 %	Panasonic
RCMP	ERJ-6GEYJ333V	1	33 k/0.125 W/0805/5 %	Panasonic
RCP	ERJ-14YJ100U	1	10/0.5 W/1210/5 %	Panasonic
RCS	KNP100JR-73-0R39	1	0.39/1 W/5 %/AXIAL	Yageo
RD1, RD2, RD3, RD4	ERJ-8GEYJ224V	4	220 k/0.25 W/1206/5 %	Panasonic
RG	ERJ-8GEYJ470V	1	47/0.25 W/1206/5 %	Panasonic
RIN1, RIN2	ERJ-8GEYJ752V	2	7.5 k/0.25 W/1206/5 %	Panasonic
RVBUS	ERJ-8ENF-1962V	1	19.6 k/0.25 W/1206/1 %	Panasonic
RVCC1, RVCC2	ERJ-8GEYJ154V	2	150 k/0.25 W/1206/5 %	Panasonic
VBUS	5003	1	0.04" dia orange	Keystone
VCC, VDC (HV), VOUT (HV)	5000	3	0.04" dia red	Keystone
VR1	S10K320E2K1	1	510 V/3.5 kA/10 mm	Epcos
Z1	1902F	1	Standoff, Hex 0.65"L 4-40THR Nylon	Keystone
Z2	NY PMS 440 0025 PH	1	Screw, Philips 4-40 x 1/4 Nylon	B & F Fastner
Z3	591202B00000G	1	Heatsink, TO-220	Aavid Thermalloy

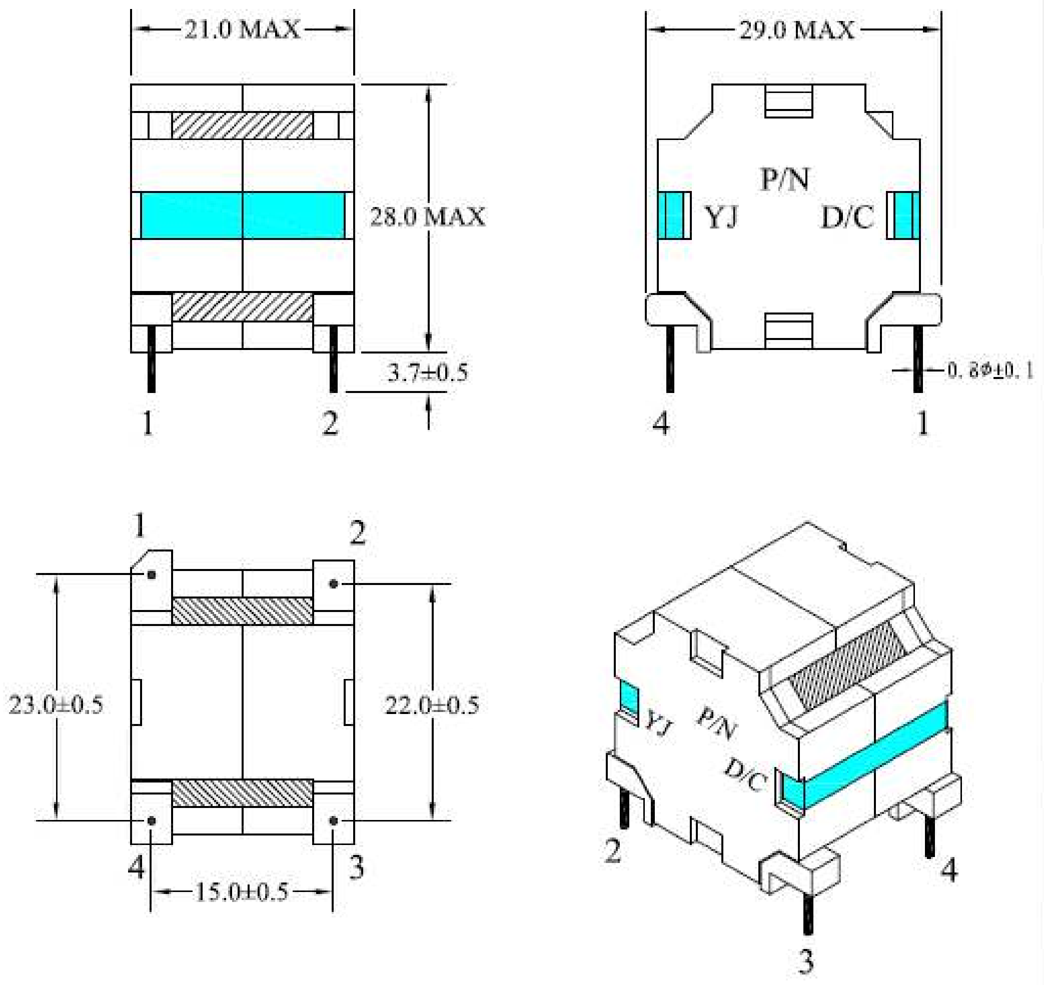
5 Inductor specification

YUJING

SPECIFICATION

CUSTOMER	I. R	PART NO.		DESCRIPTION		QP-2520H (4P)	
MODEL NO.		DATE	2015-09-02	REV.	1.0	SHEET	2 OF 4

1.MACHENIC DIMENSION (UNIT:mm)



NOTE:
1.CLIP PIN CUT OFF.
2.CORE需GAP.
3.CORE中柱點膠.
4.CORE兩端用2PCS CLIP固定, CLIP位置必須端正.
5.成品含浸.
6.繞線時PIN1朝機臺內.

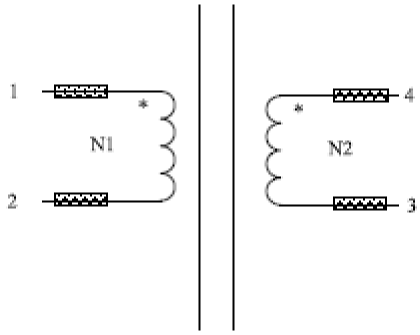
MYLAR TAPE
CLIP
SOLDER

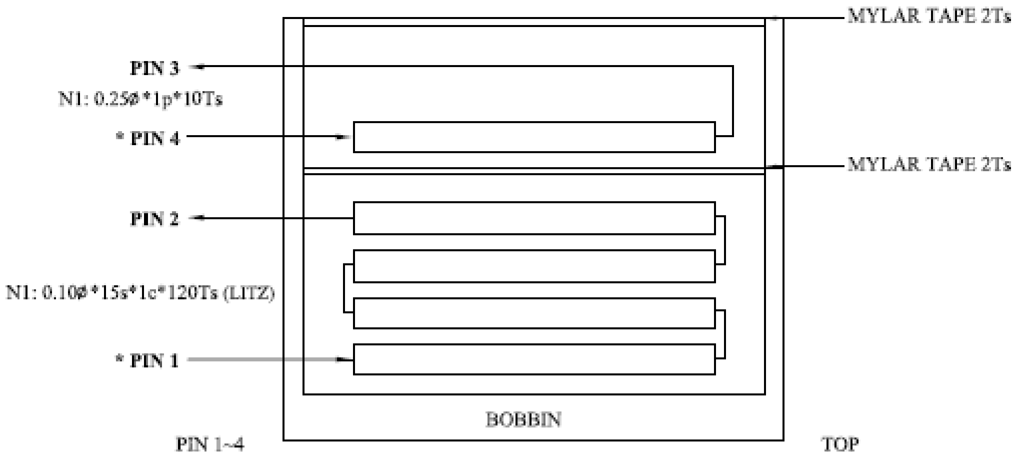
YUJING

SPECIFICATION

CUSTOMER	I. R	PART NO.		DESCRIPTION		QP-2520H (4P)	
MODEL NO.		DATE	2015-09-02	REV.	1.0	SHEET	3 OF 4

2.WINDING ORDER





NOTE:
出入線須加TEFLON TUBE.

透明 TUBE

YUJING

SPECIFICATION

CUSTOMER	I. R	PART NO.		DESCRIPTION	QP-2520H (4P)		
MODEL NO.		DATE	2015-09-02	REV.	1.0	SHEET	4 OF 4

3.ELECTRICAL SPECIFICATION

HP: 4284A ZENTECH:WK5235, 502A , F = 10KHz V =1V AT 25°C

NO.	START	FINISH	WIRE	COLOR	TURNS	INDUCTANCE	DCR (mΩ)
L1	1	2	0.10ø*15s*1c(LITZ)	Y	120±0.5	1.2 mH±10%	1250 Max
L2	4	3	0.25ø*1c	Y	10±0.5		

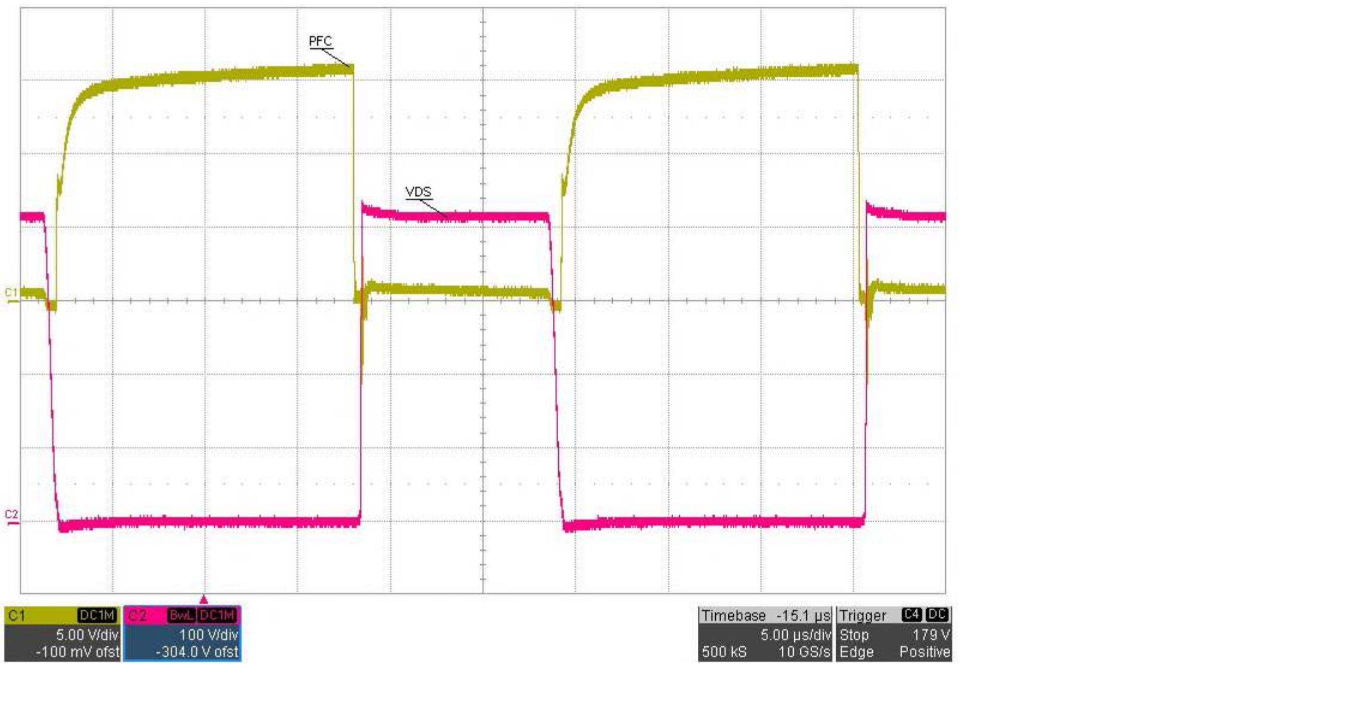
4.DIELECTRIC STRENGTH

WITHSTANDING VOLTAGE: 1.0KV/3SEC/AC/ 3 mA , WINDING TO CORE
1.0KV/3SEC/AC/ 3 mA , WINDING TO WINDING

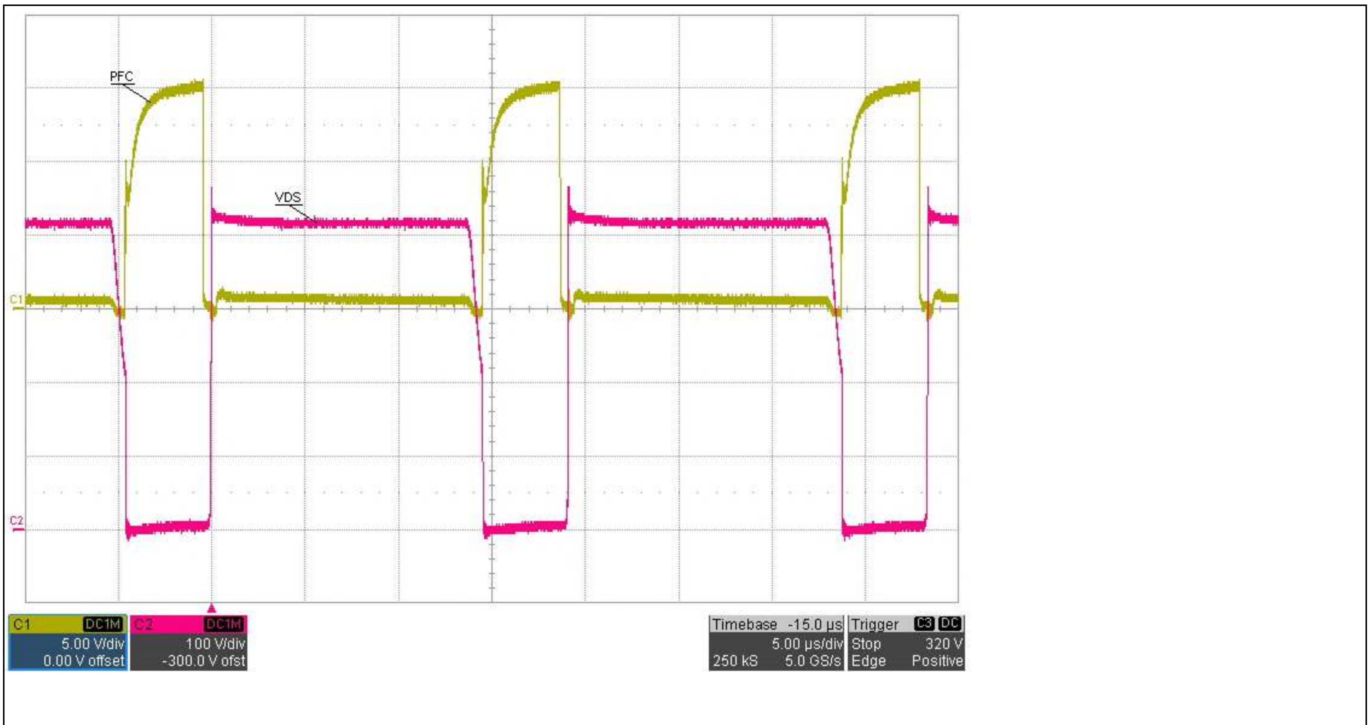
5.MATERIAL LIST

NO.	ITEM	TYPE	SUPPLIER	UL FILE NO.
1	BOBBIN	PM-9820/PM-9630	SUMITOMO BAKELITE CO., LTD.	E41429
2	CORE	QP25 3C94	FERROXCUBE	
		QP25 MB4	JFE	
3	WIRE	MW 75-C/UEW-4@	JUNG SHING WIIRE CO., LTD.	E174837
		MW 75-C/UEW/U@	PACIFIC ELECTRIC WIRE &CABLE (SHENZHEN) CO.,LTD	E201757
		MW 75-C/xUEW	FENG CHING METAL CORPORATION	E172395
4	WINDING TAPE	1350F-1	3M COMPANY	E17385
5	TUBE	TFL	GREAT HOLDING INDUSTRIAL CO.,LTD.	E156256
		TFL	FLUOTECH INDUSTRIAL CO.,LTD.	E175982(S)
		TFL	CHANG YUAN ELECTRONIC(SHENZHEN) CO., LTD.	E180908
6	ADHESIVE	ES2044P	CANADA SILICONE INC.	E223694
		3300ZH	EATTO ELECTRONIC MATERIAL CO., LTD.	E218090
7	VARNISH	WP-2952F-2G	HITACHI CHEMICAL CO., LTD.	E72979
8	CLIP	SK7	SHANGHAI DIAN QIANG PRODUCTS SUPPLYING CO.,LTD	

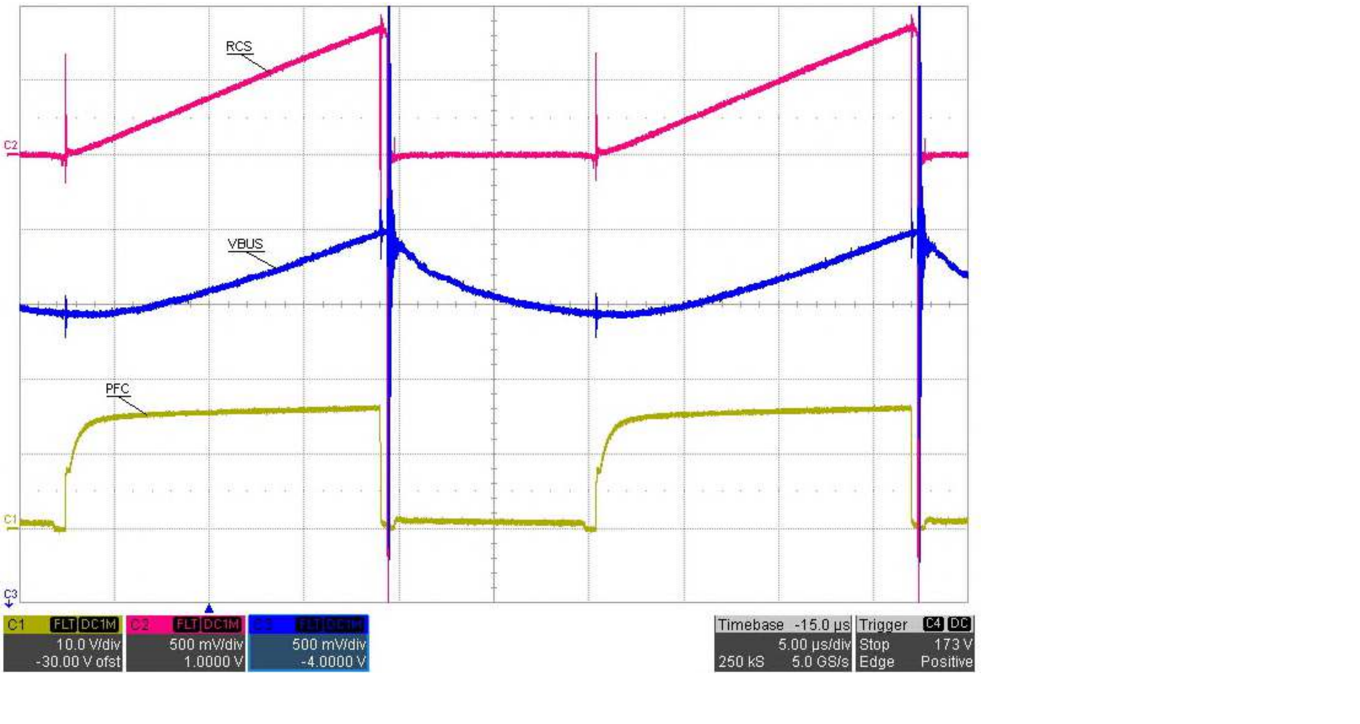
6 Operating waveforms



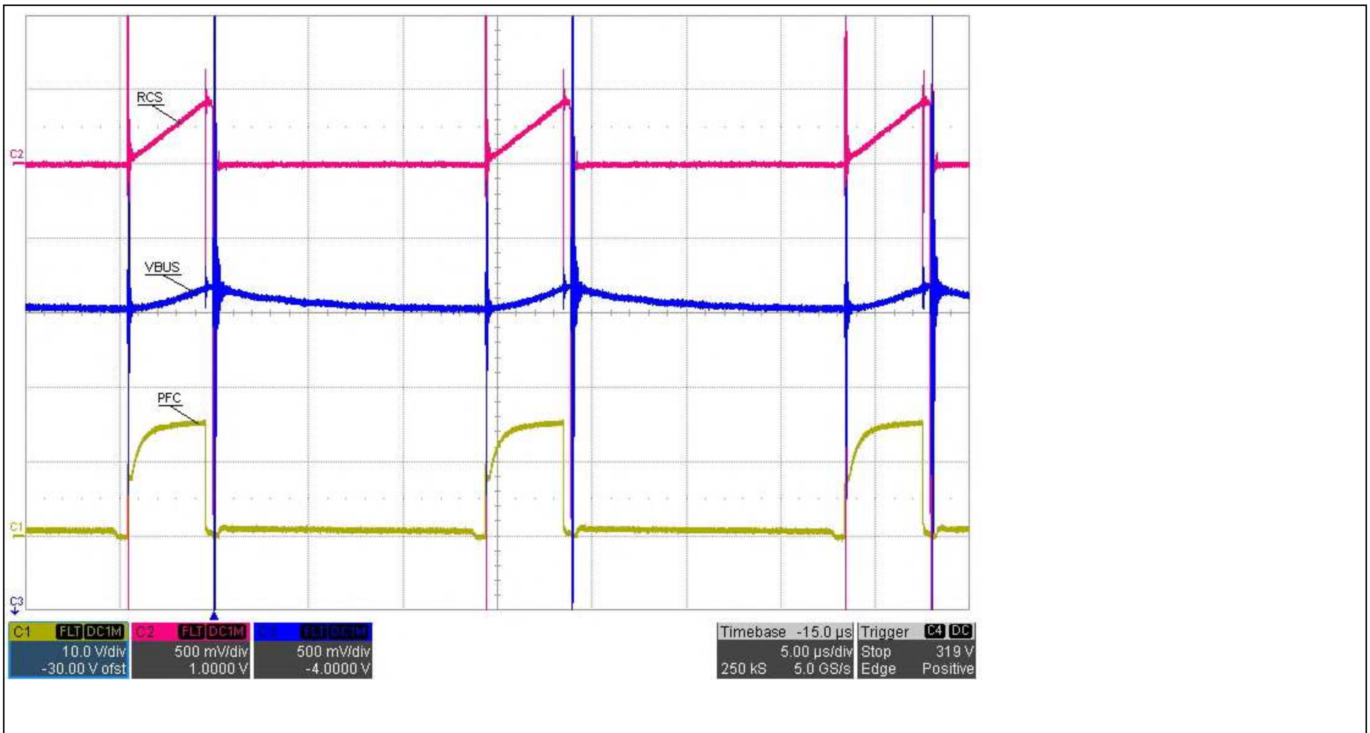
Gate (yellow) and drain (red) waveforms at line peak at 90 W/120 VAC input



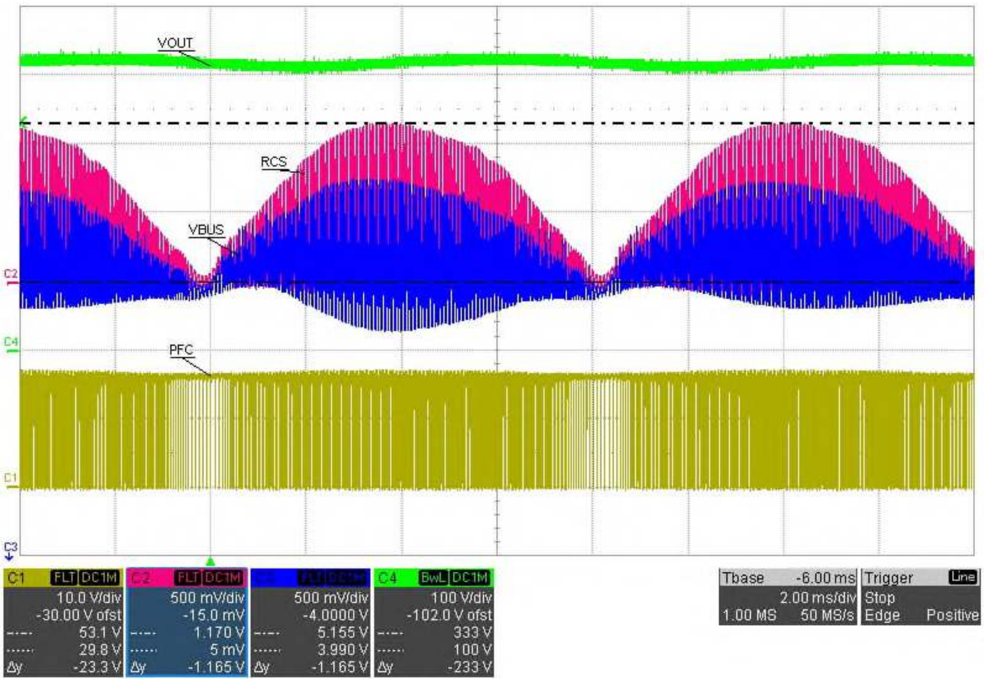
Gate (yellow) and drain (red) waveforms at line peak at 90 W/230 VAC input



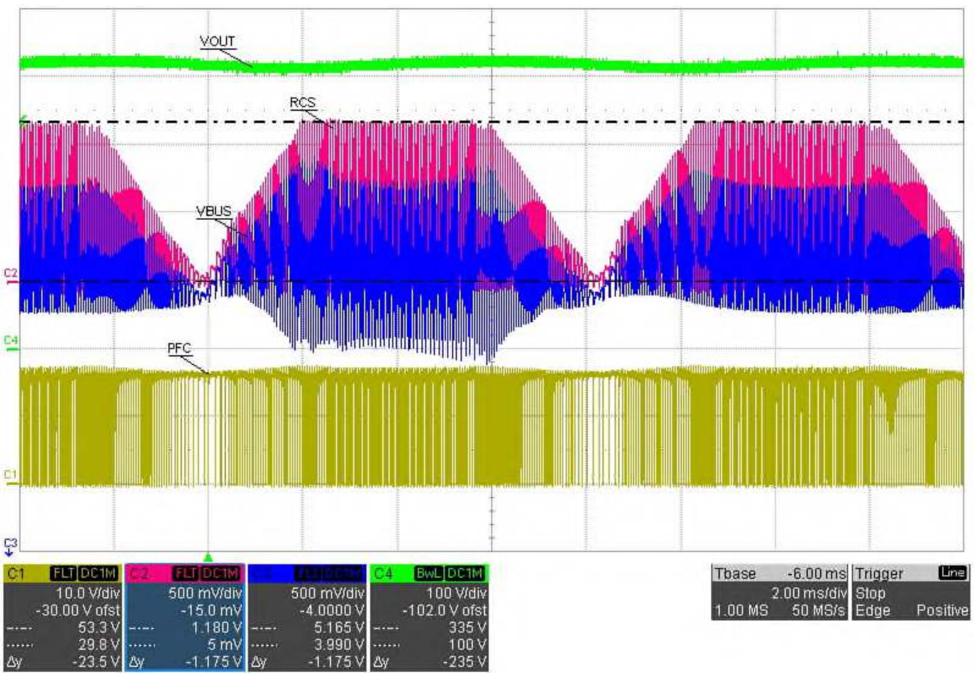
Current sense (red), VBUS input (blue) and gate drive (yellow) at line peak at 90 W/120 VAC



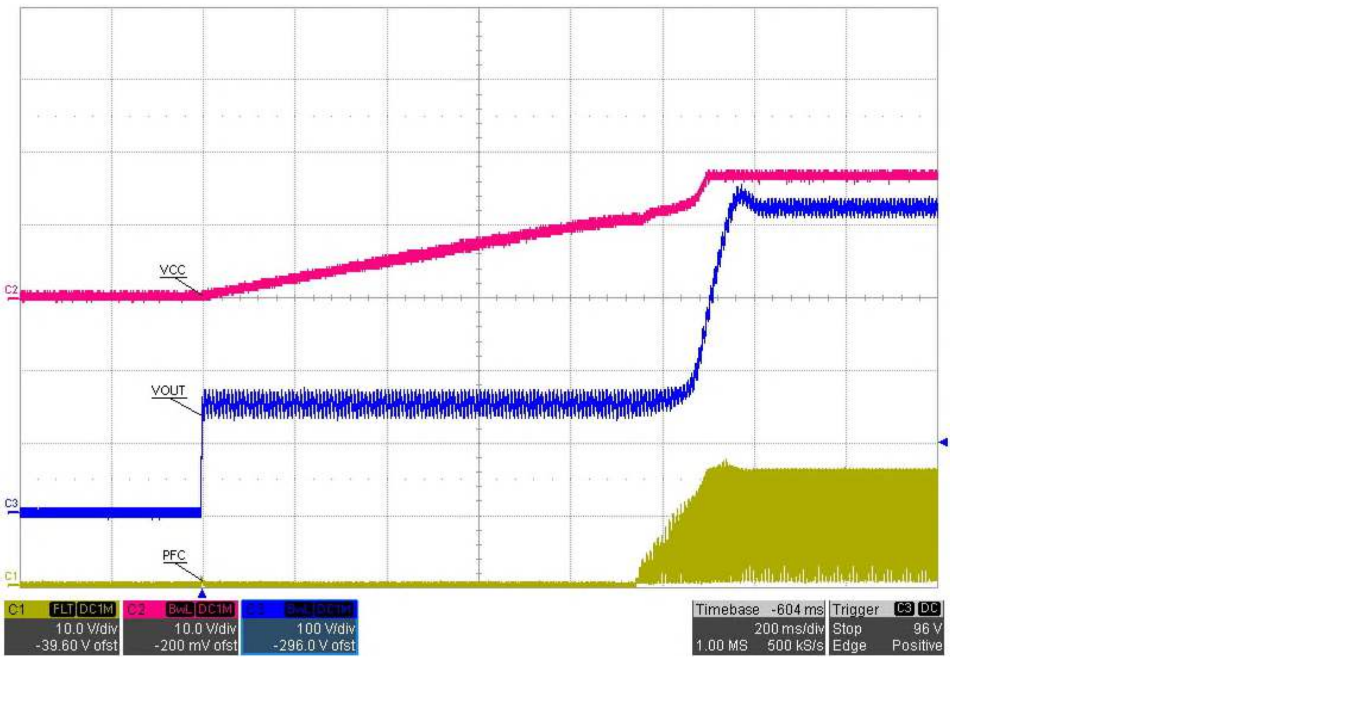
Current sense (red), VBUS input (blue) and gate drive (yellow) at line peak at 90 W/230 VAC



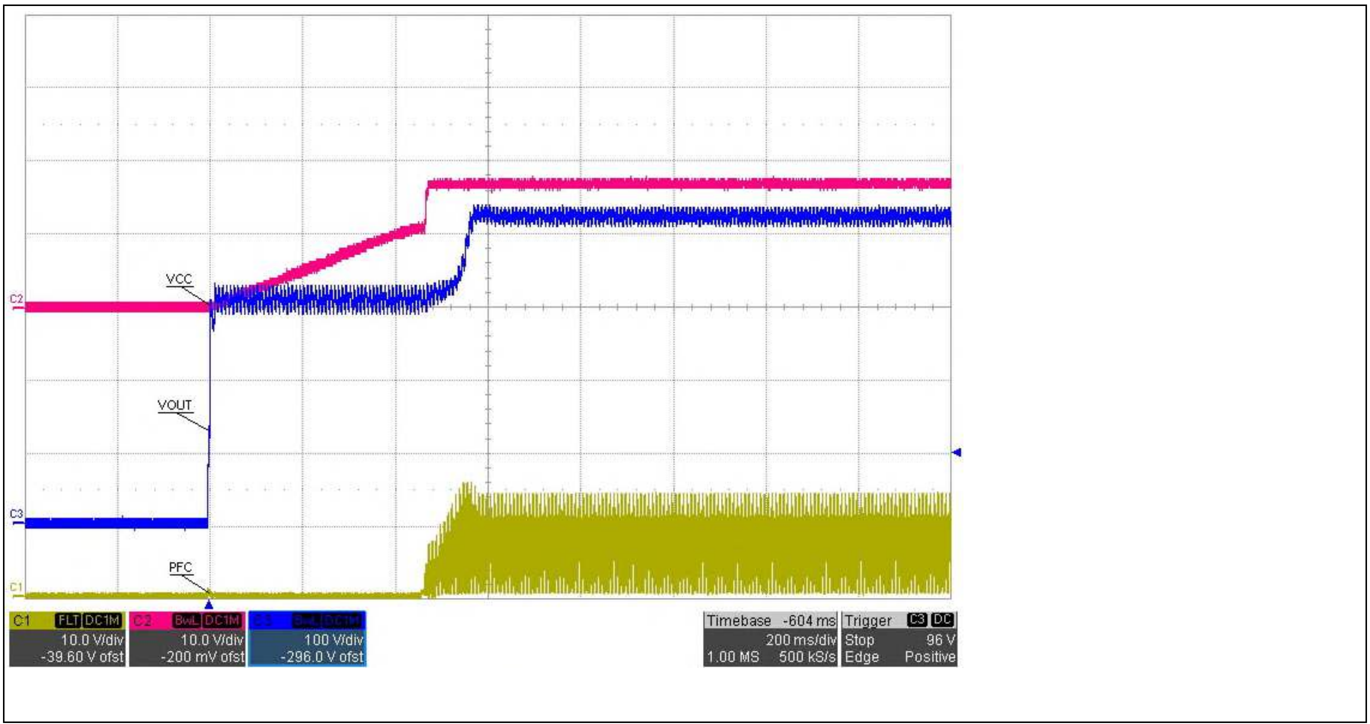
Current sense (red), VBUS (blue), VOUT (green) and gate drive (yellow) at 90 W/90 VAC (no current limit)



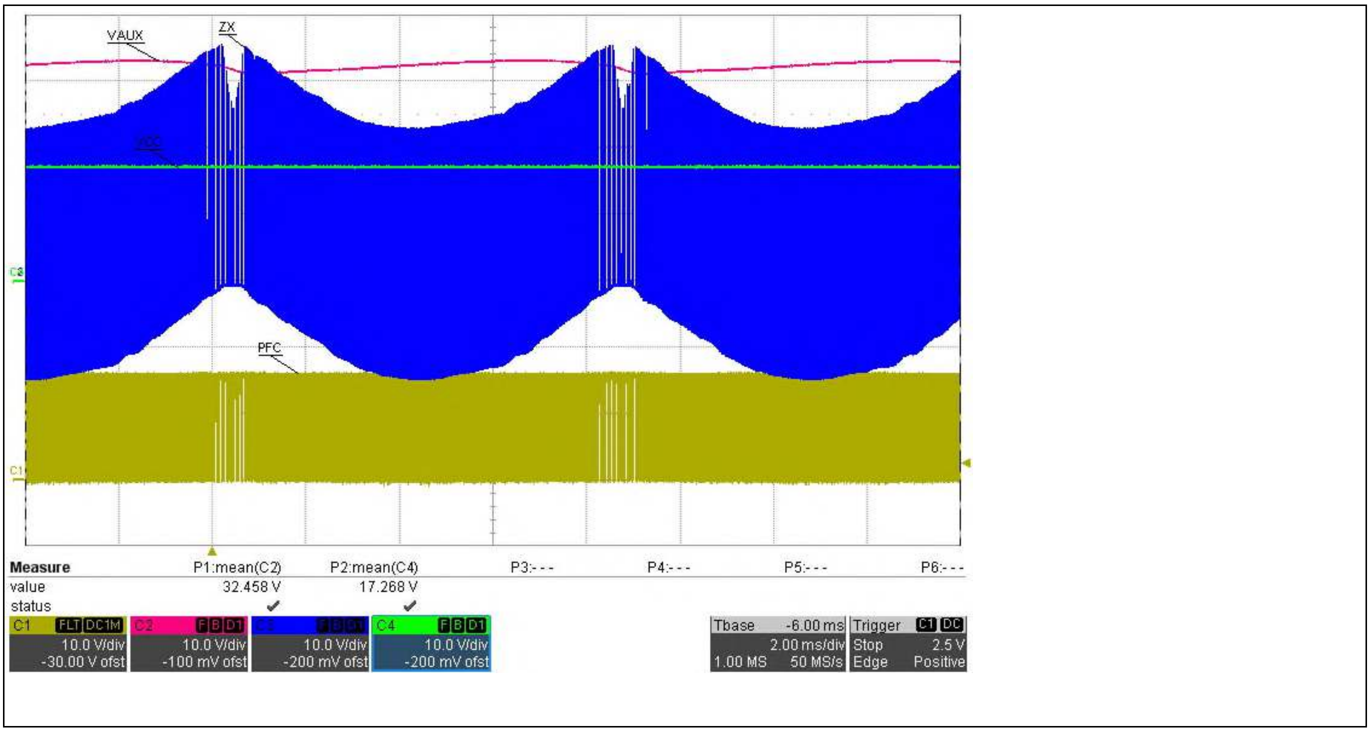
Current sense (red), VBUS (blue), VOUT (green) and gate drive (yellow) at 90 W/75 VAC (current limiting)



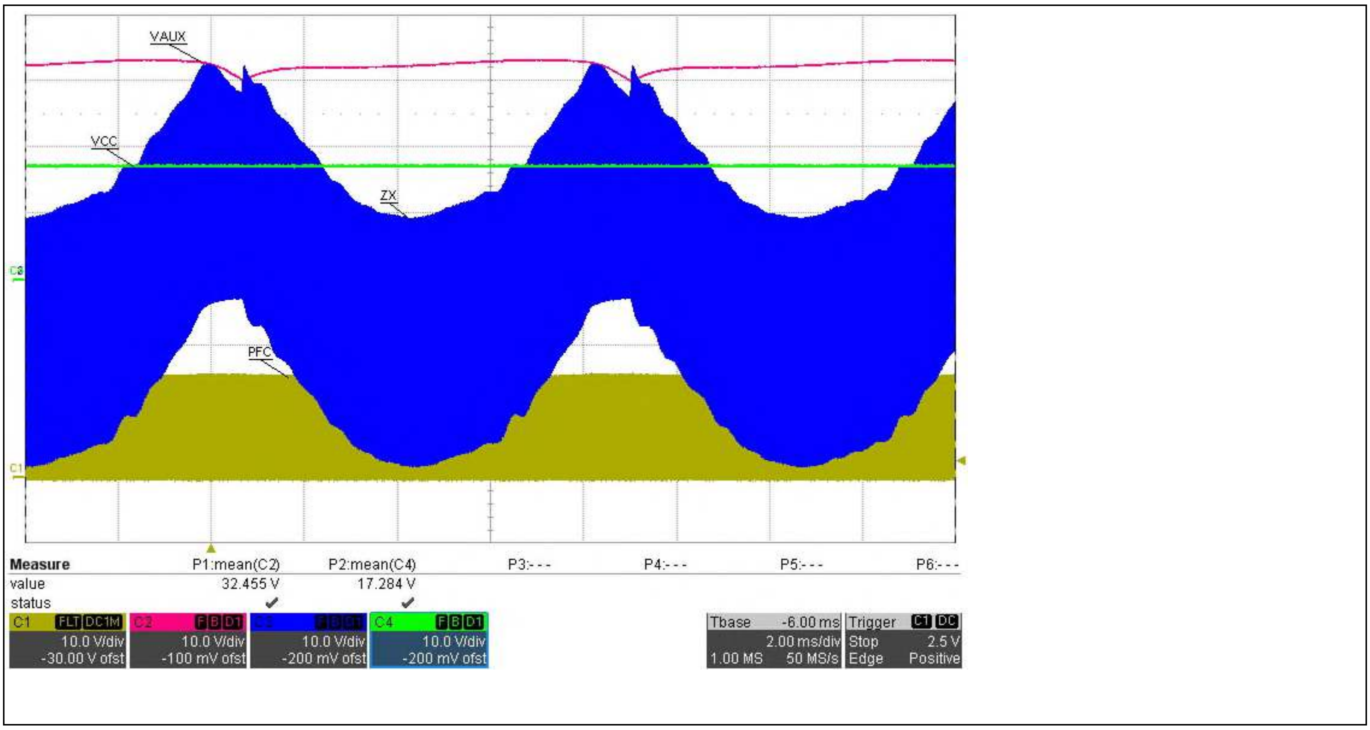
VCC (red), VOUT (blue) and gate drive (yellow) during startup at 90 W/120 VAC



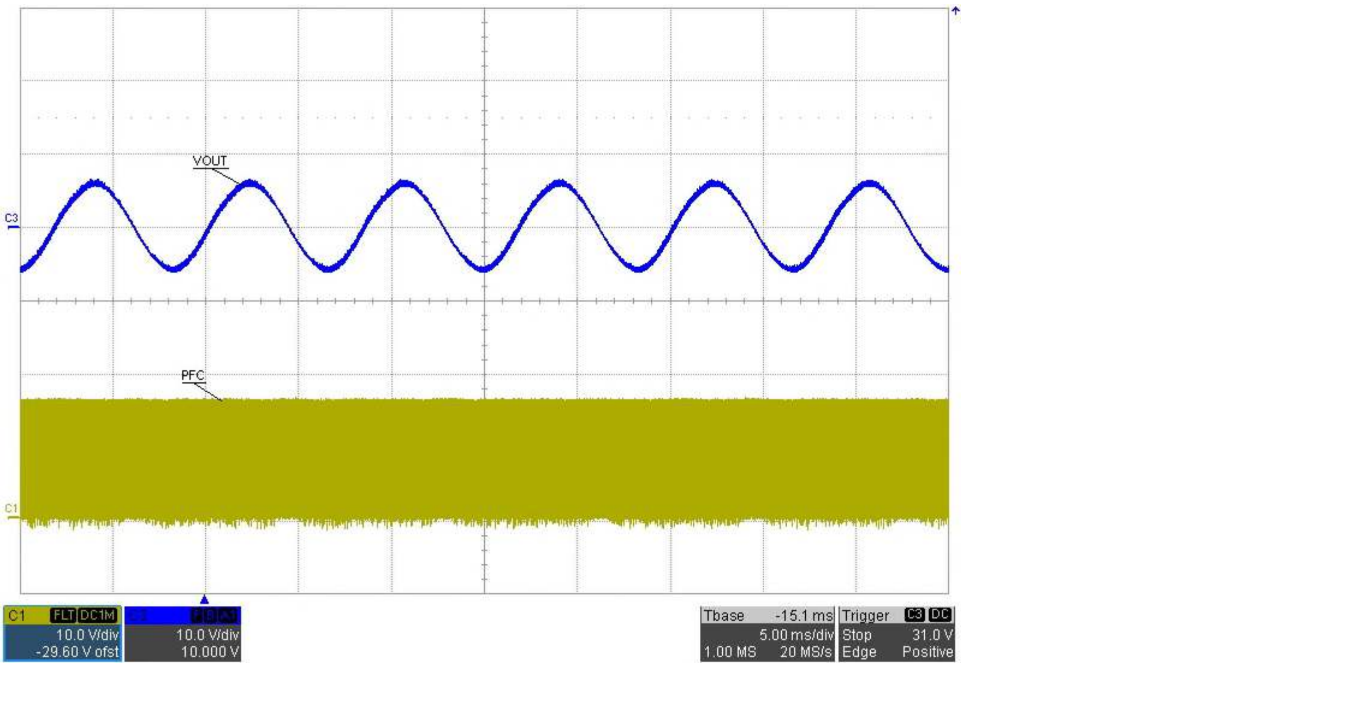
VCC (red), VOUT (blue) and gate drive (yellow) during startup at 90 W/230 VAC



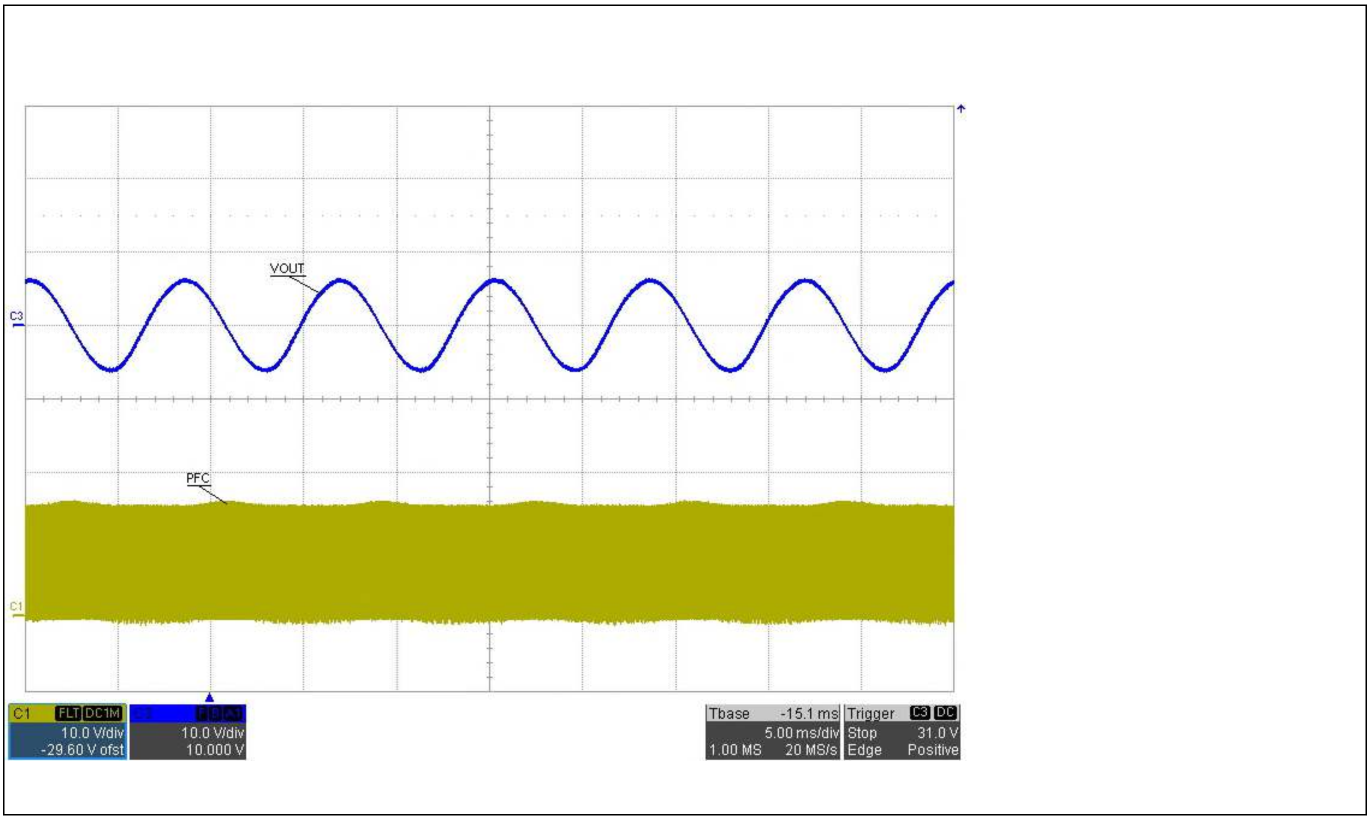
VCC (green), VAUX (red), VZX (blue) and gate drive (yellow) at 90 W/120V AC



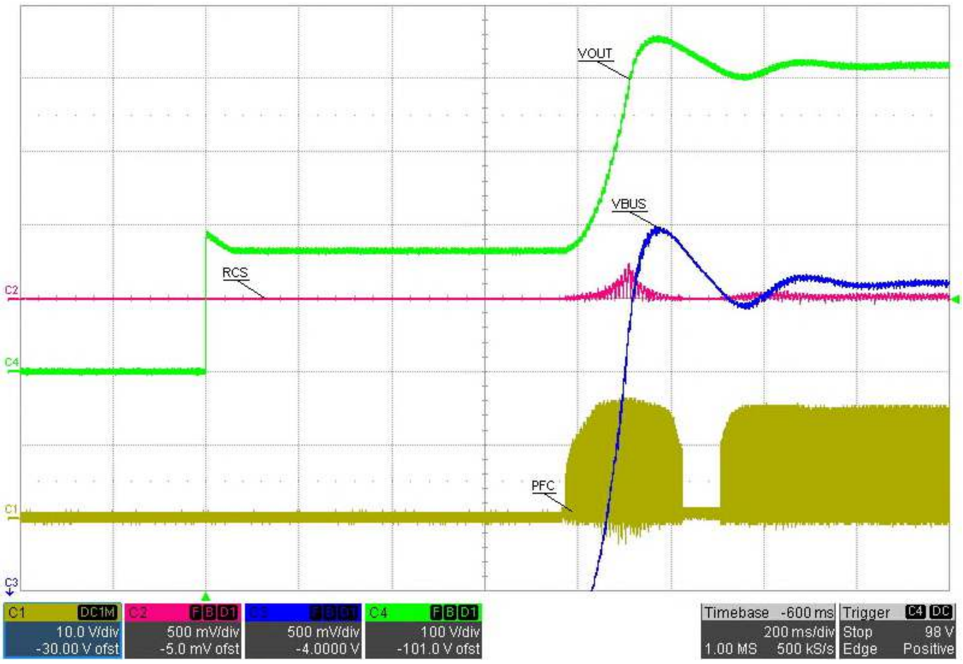
VCC (green), VAUX (red), VZX (blue) and gate drive (yellow) at 90 W/230 VAC



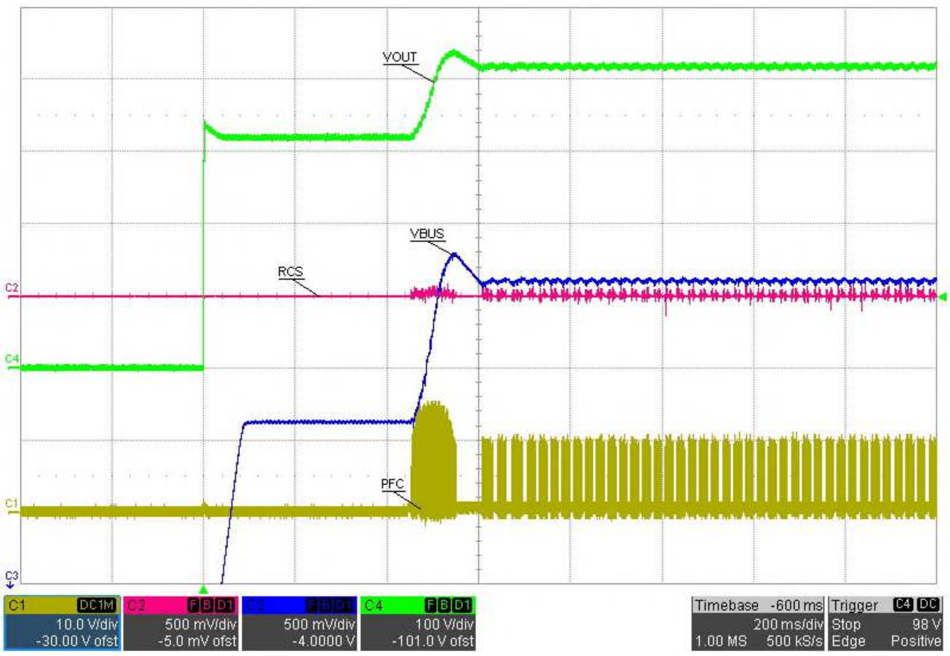
VOUT ripple (blue), gate drive (yellow) at 90 W/120 VAC



VOUT ripple (blue), gate drive (yellow) at 90 W/230 VAC



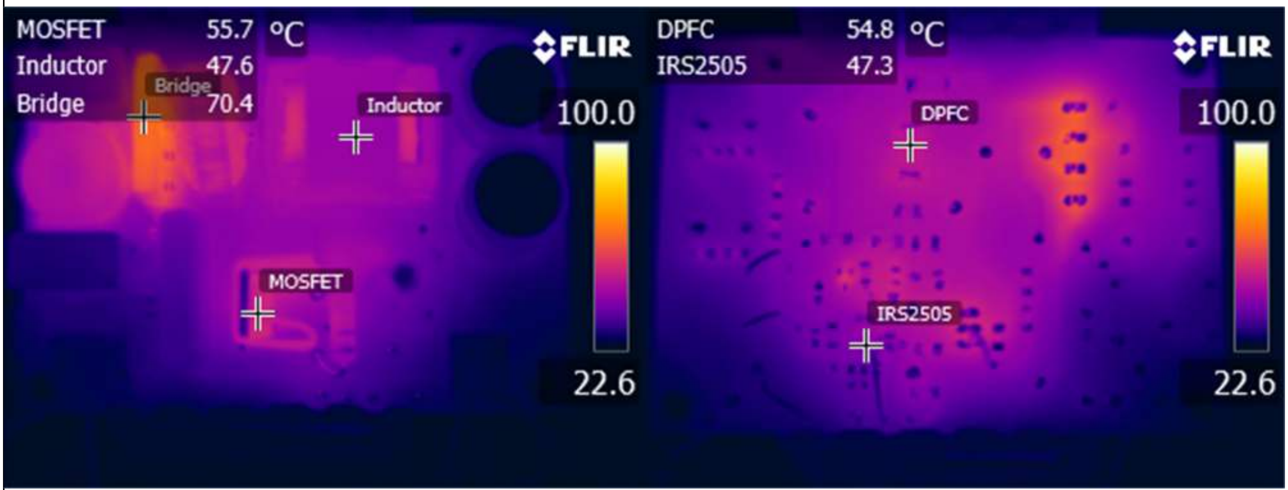
Current sense (red), VBUS (blue), VOUT (green) and gate drive (yellow) startup at 18 W/120 VAC showing over-voltage protection



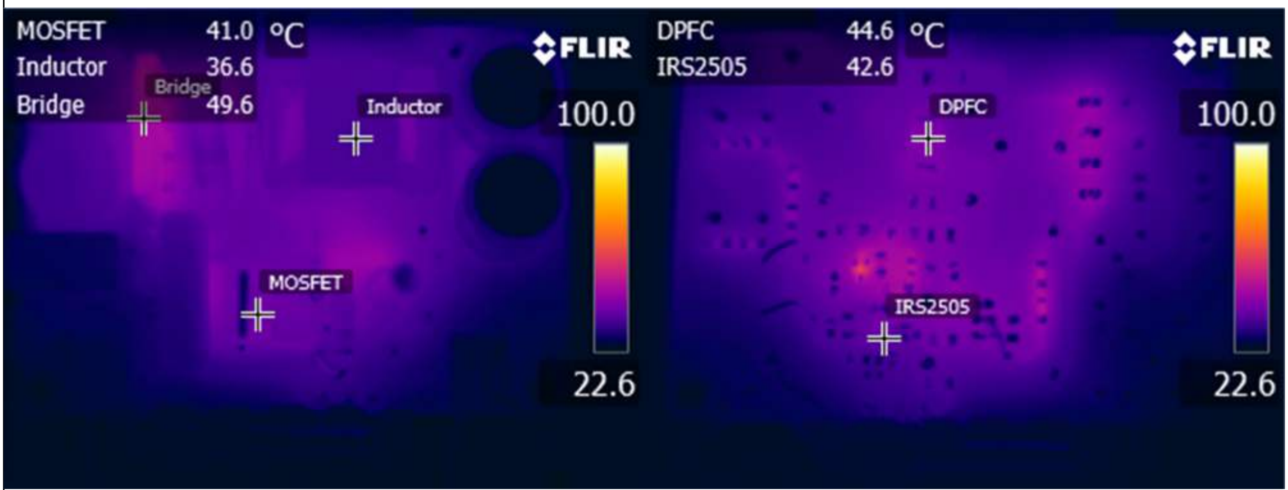
Current sense (red), VBUS (blue), VOUT (green) and gate drive (yellow) startup at 18 W/230 VAC showing over-voltage protection

7 Thermal images

Thermal images of the top and bottom of the board in open air at room temperature of 25°C measured after 15 minutes operation:

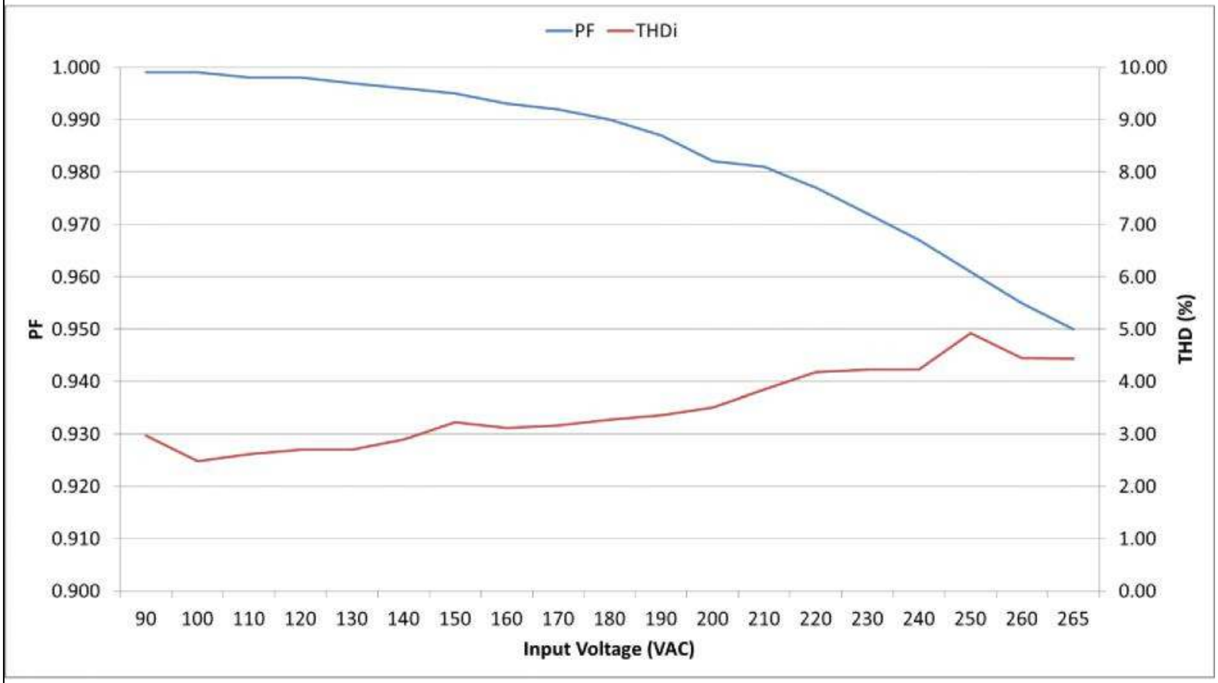


Thermal images for 120 VAC , full load (90 W)

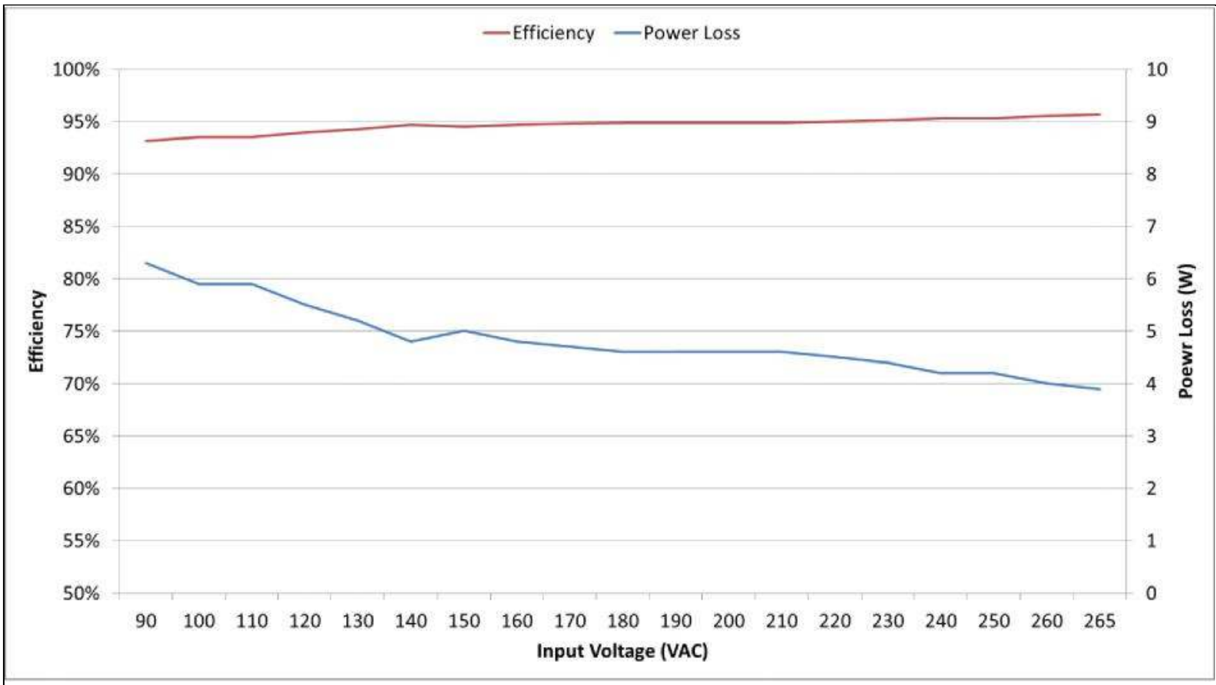


Thermal images for 230 VAC , full load (90 W)

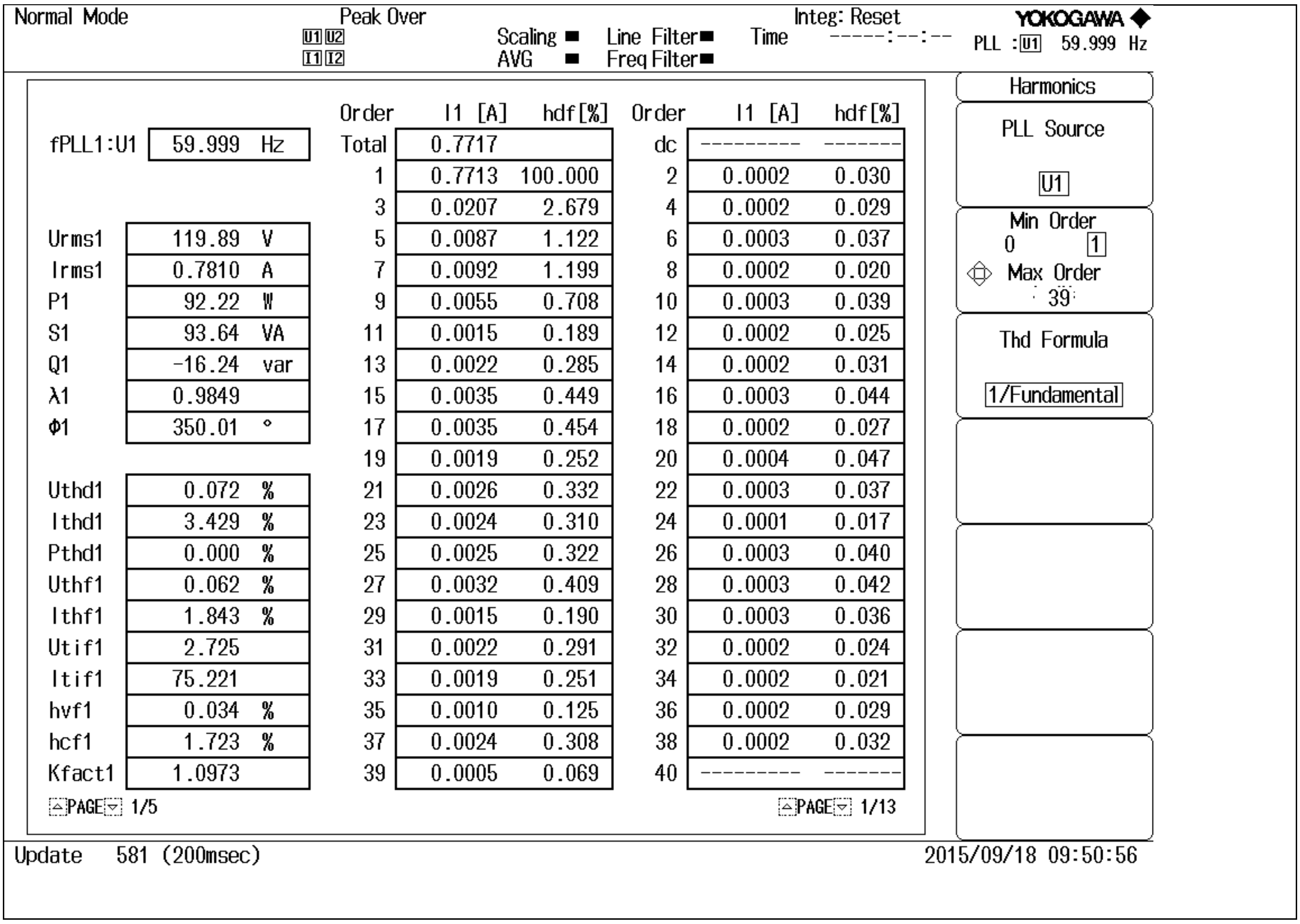
8 Power factor and THD measurements



Power factor and THDi at 90 W load



Efficiency and power losses at 90 W load



Normal Mode | Peak Over U1 U2 I1 I2 | Scaling ■ AVG ■ | Line Filter■ Freq Filter■ | Integ: Reset Time -----:--:-- | YOKOGAWA ◆ PLL :U1 59.999 Hz

Parameter	Value
fPLL1:U1	59.999 Hz
Urms1	119.89 V
Irms1	0.7810 A
P1	92.22 W
S1	93.64 VA
Q1	-16.24 var
λ1	0.9849
Φ1	350.01 °
Uthd1	0.072 %
Ithd1	3.429 %
Pthd1	0.000 %
Uthf1	0.062 %
Ithf1	1.843 %
Utif1	2.725
Itif1	75.221
hvf1	0.034 %
hcf1	1.723 %
Kfact1	1.0973

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Order	I1 [A]	hdf[%]	Order	I1 [A]	hdf[%]
Total	0.7717		dc	---------	-------
1	0.7713	100.000	2	0.0002	0.030
3	0.0207	2.679	4	0.0002	0.029
5	0.0087	1.122	6	0.0003	0.037
7	0.0092	1.199	8	0.0002	0.020
9	0.0055	0.708	10	0.0003	0.039
11	0.0015	0.189	12	0.0002	0.025
13	0.0022	0.285	14	0.0002	0.031
15	0.0035	0.449	16	0.0003	0.044
17	0.0035	0.454	18	0.0002	0.027
19	0.0019	0.252	20	0.0004	0.047
21	0.0026	0.332	22	0.0003	0.037
23	0.0024	0.310	24	0.0001	0.017
25	0.0025	0.322	26	0.0003	0.040
27	0.0032	0.409	28	0.0003	0.042
29	0.0015	0.190	30	0.0003	0.036
31	0.0022	0.291	32	0.0002	0.024
33	0.0019	0.251	34	0.0002	0.021
35	0.0010	0.125	36	0.0002	0.029
37	0.0024	0.308	38	0.0002	0.032
39	0.0005	0.069	40	---------	-------

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Harmonics | PLL Source U1 | Min Order 0 1 | Max Order 39 | Thd Formula 1/Fundamental

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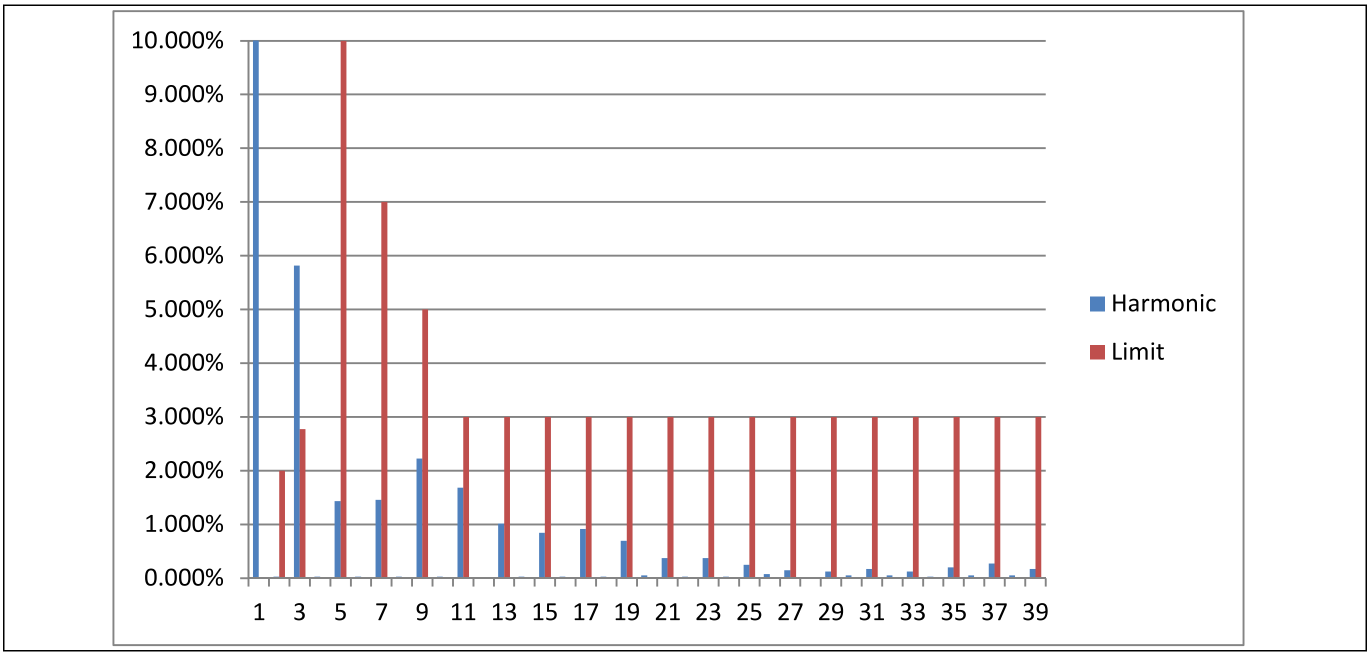
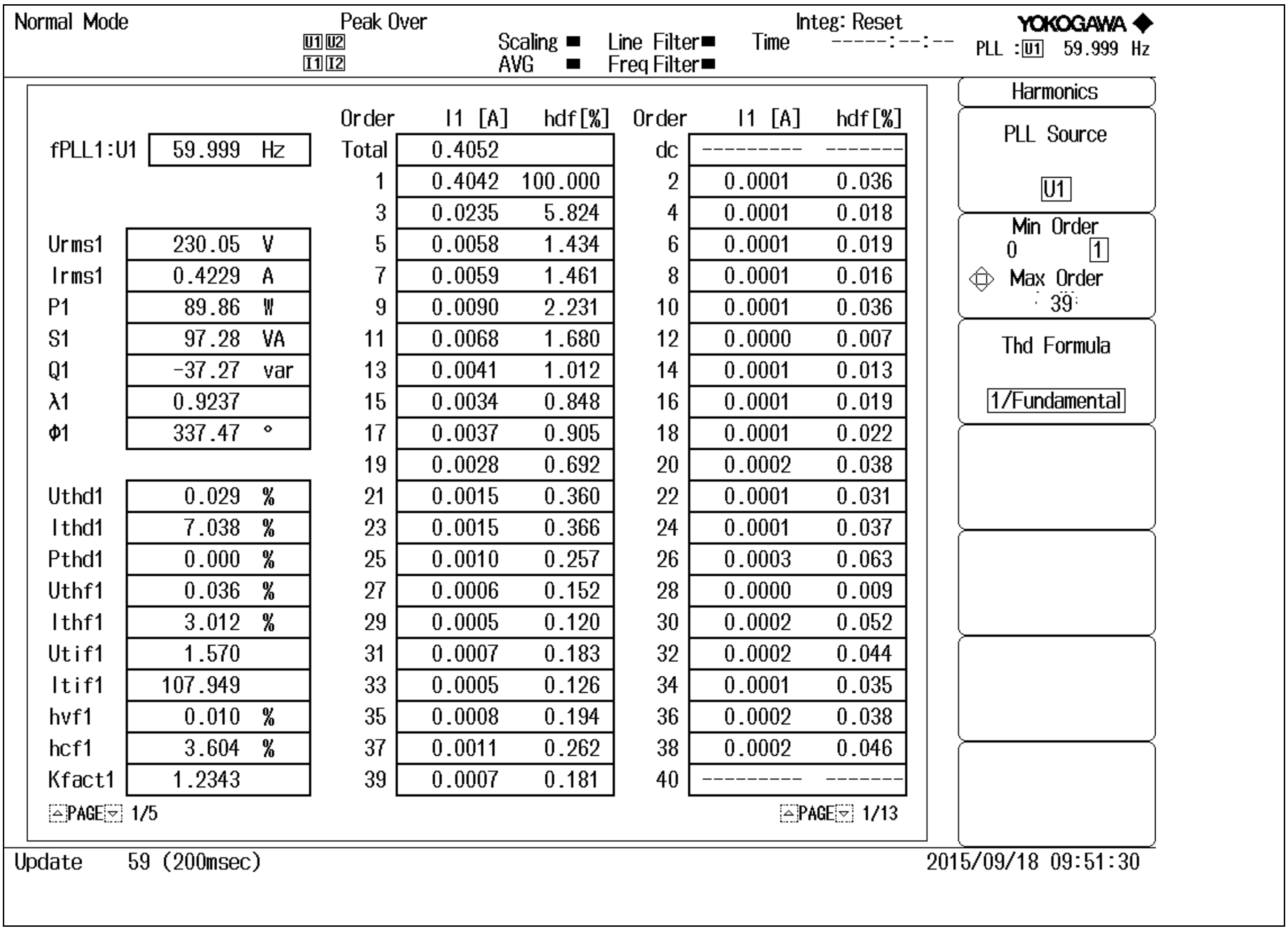
Power factor, THDi and harmonics at 90 W load at 120 VAC



Harmonics vs EN61000-3-2 class C limits at 90 W load at 120 VAC



Normal Mode | Peak Over U1 U2 I1 I2 | Scaling ■ AVG ■ | Line Filter■ Freq Filter■ | Integ: Reset Time -----:--:-- | YOKOGAWA ◆ PLL :U1 59.999 Hz

Parameter	Value
fPLL1:U1	59.999 Hz
Urms1	230.05 V
Irms1	0.4229 A
P1	89.86 W
S1	97.28 VA
Q1	-37.27 var
λ1	0.9237
Φ1	337.47 °
Uthd1	0.029 %
Ithd1	7.038 %
Pthd1	0.000 %
Uthf1	0.036 %
Ithf1	3.012 %
Utif1	1.570
Itif1	107.949
hvf1	0.010 %
hcf1	3.604 %
Kfact1	1.2343

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Order	I1 [A]	hdf[%]	Order	I1 [A]	hdf[%]
Total	0.4052		dc	---------	-------
1	0.4042	100.000	2	0.0001	0.036
3	0.0235	5.824	4	0.0001	0.018
5	0.0058	1.434	6	0.0001	0.019
7	0.0059	1.461	8	0.0001	0.016
9	0.0090	2.231	10	0.0001	0.036
11	0.0068	1.680	12	0.0000	0.007
13	0.0041	1.012	14	0.0001	0.013
15	0.0034	0.848	16	0.0001	0.019
17	0.0037	0.905	18	0.0001	0.022
19	0.0028	0.692	20	0.0002	0.038
21	0.0015	0.360	22	0.0001	0.031
23	0.0015	0.366	24	0.0001	0.037
25	0.0010	0.257	26	0.0003	0.063
27	0.0006	0.152	28	0.0000	0.009
29	0.0005	0.120	30	0.0002	0.052
31	0.0007	0.183	32	0.0002	0.044
33	0.0005	0.126	34	0.0001	0.035
35	0.0008	0.194	36	0.0002	0.038
37	0.0011	0.262	38	0.0002	0.046
39	0.0007	0.181	40	---------	-------

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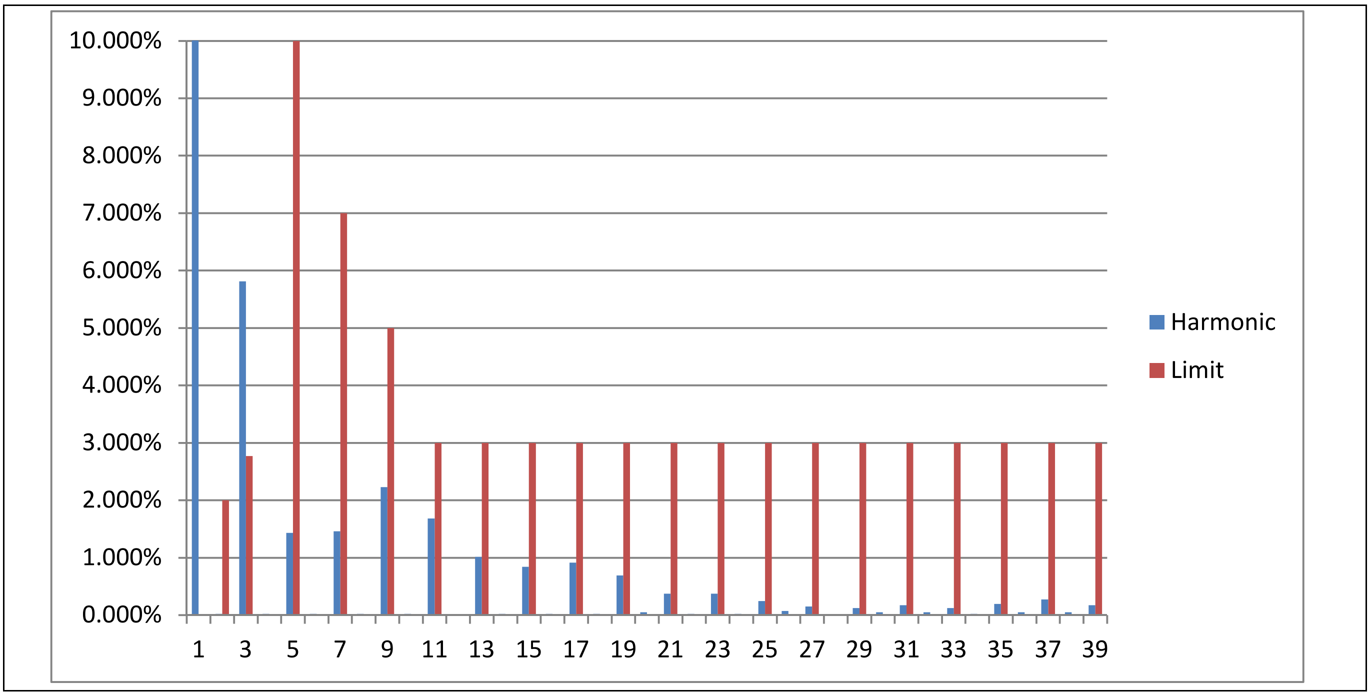
Harmonics | PLL Source: U1 | Min Order 0 1 | Max Order 39 | Thd Formula: 1/Fundamental

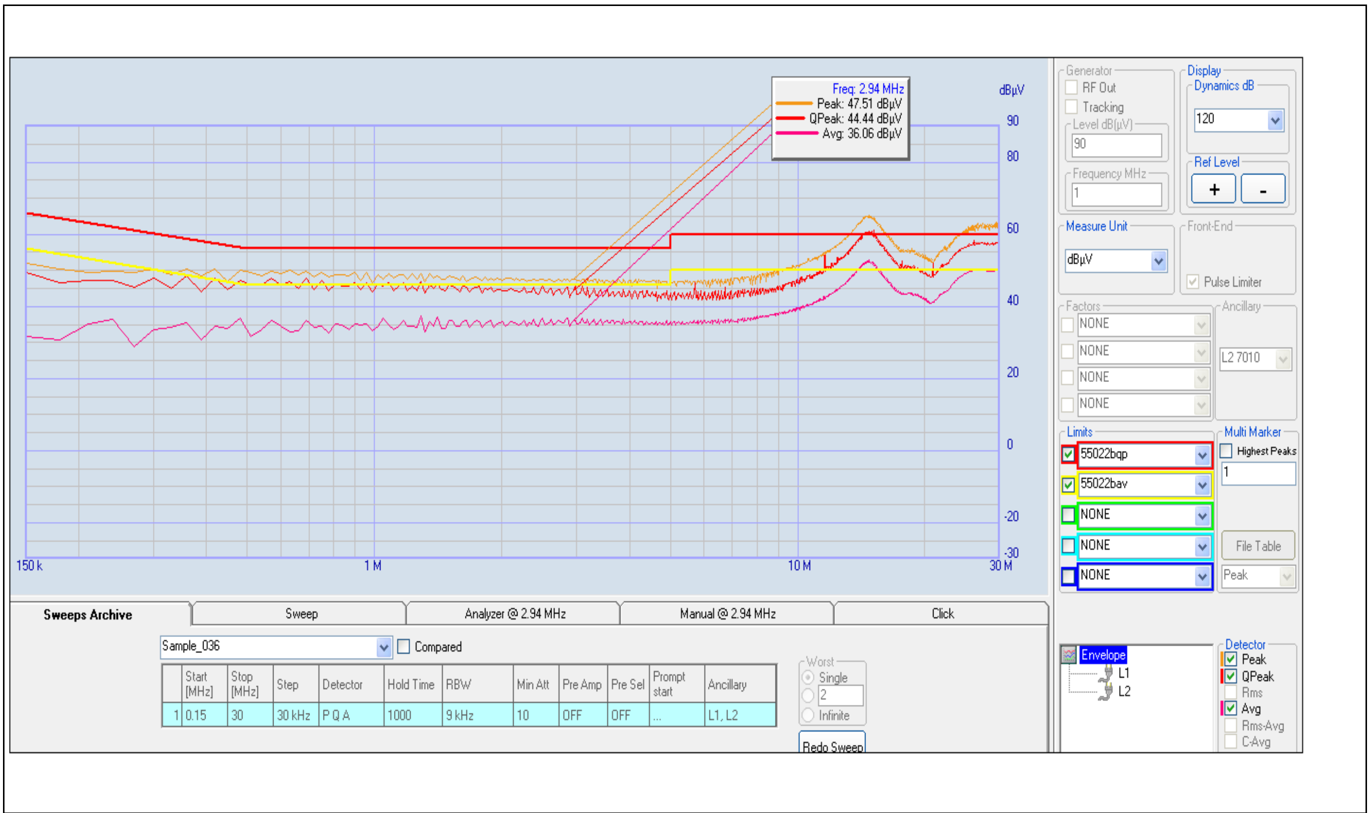
Update 59 (200msec) 2015/09/18 09:51:30

Power factor, THDi and harmonics at 90 W load at 230 VAC

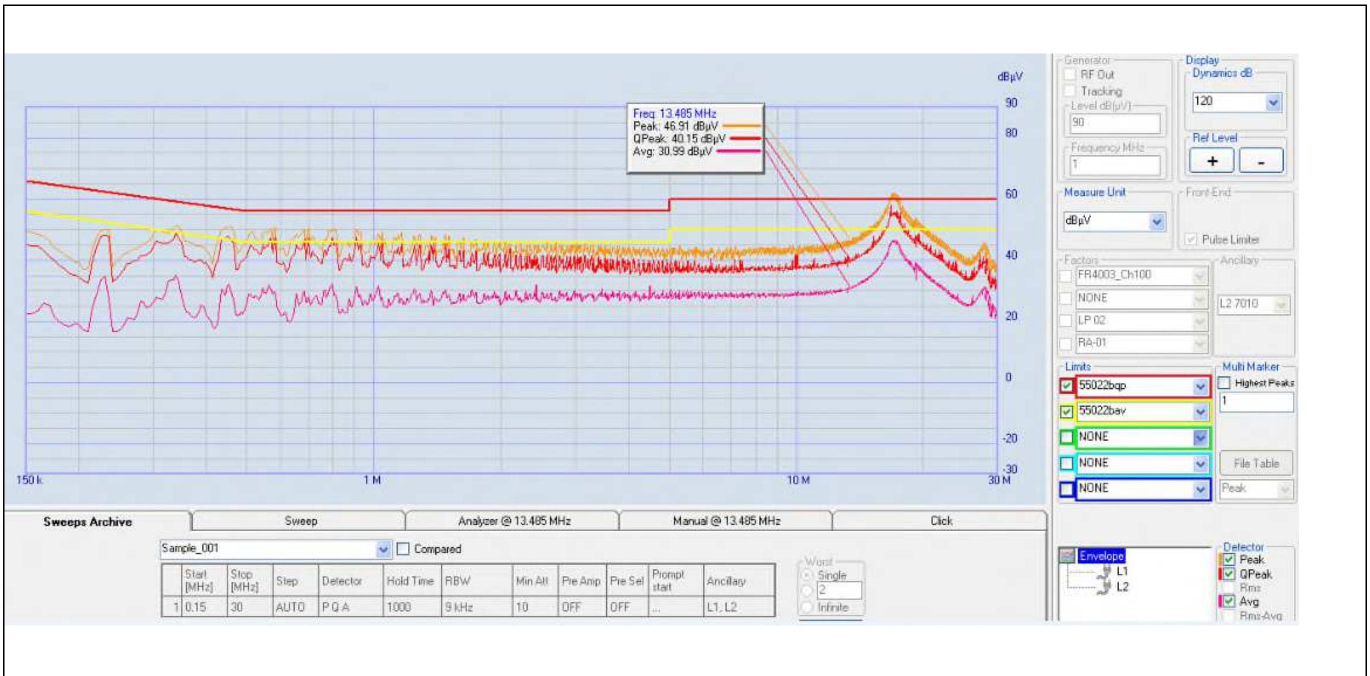


Harmonics vs EN61000-3-2 class C limits at 90 W load at 230 VAC

9 Conducted EMI test measurements



Conducted EMI plot at 90 W load at 120 VAC



Conducted EMI plot at 90 W load at 230 VAC

Note: Infineon Technologies does not guarantee compliance with any EMI standard.

10 Conclusion

The waveforms in figures 4 and 5 show that the switching frequency is 37 kHz at the peak of the AC line at 120 VAC input. At 230 VAC input the frequency increases to 53 kH with an off time of 15 µs, which meets the target value based on the calculated value of LPFC. Switching frequencies match the values calculated from the design tool. Figure 6 shows the peak current reaches 2.1 A, which matches the result from equation 4 when VACMIN is replaced by 120 VAC. The current sense portion of the signal supplied to the VBUS input shows the effect of CVBUS, which provides low pass filtering to turn the ramp waveform into an approximately triangular signal. This causes the voltages from maximum to average and from minimum to average, to be approximately equal where the average in steady state operation, is the VBUSREG value typically 4.1 V.
Figure 8 shows the sinusoidal envelope of the inductor current indicating correct operation at minimum AC line input of 90 VAC with a peak current of 0.165 V/0.39 Ω matching the calculated value of 2.98 A. Figure 9 shows the cycle by cycle current limiting operating when the line input is reduced to 75 VAC and limiting the peak current to 2.95 A, very close to the calculated value.
Start up time is approximately 0.95 seconds at 120 VAC input measuring from switch on until the gate drive first starts up. Another 0.3 seconds is required for the output to reach 420 V. This also matches the predicted value from equation 2. Start up time is reduced to 0.5 seconds at 230 VAC input.
Figures 12 and 13 show the voltage (VZX) signal that appears at the auxiliary winding measured at the ZX test point. As expected the positive and negative peak values vary during the AC line input half cycle but the peak to peak value remains constant. As a consequence the voltage at VAUX from the charge pump circuit is very constant over the line voltage range. There is ample headroom for the linear regulaor circuit to supply VCC at 17.3 V over the full range. Head room cannot however be reduced further without compromising start up performance at low line input. Figures 14 and 15 display the output voltage ripple of around 15V, to verify the calculated CBUC value according to equation 13. Figures 16 and 17 demonstrate the over voltage protection function disabling the gate drive output at startup with light load. Under this condition the output voltage over shoots.
The thermal images in section 7 show that in open air at worst case low line condition, the inductor temperature rise is less than 25°C, the PFC MOSFET is 30°C with the input bridge reaching the highest temperature with a 45°C rise.
In section 8, figure 20 shows that at full load the power factor remains greater than 0.95 over the 90 to 265 VAC input range. The iTHD remains below 5 %, provided the input voltage waveform is a pure sine wave as produced by an electronic AC source. Figure 21 show the efficiency is 94% at 120VAC input and 95 % at 230 VAC input at full load. The individual harmonic measurements are shown in table 2 and table 3 to be well within the class C limits of EN61000-3-2 at full load at 120 VAC and 230 VAC.
Section 9 displays conducted emissions fall within limits over most of the frequency spectrum from 150 kHz to 30 MHz exceeding the limit slightly at around 15MHz. This peak is most likely caused by common mode noise possibly due to test setup or the fact that the board is not enclosed in a metal housing with appropriate screening of the PFC MOSFET. It should be noted that these measurements were not made by a certified test lab and are intended only as an indication of performance.

References

[1] IRS2505LPBF µPFC™ control IC datasheet, Infineon Technologies.

[2] Application Note AN-201508_pl16_012 "IRS2505L µPFC Control IC Design Guide", Peter B. Green, Helen Ding - Infineon Technologies

Revision History

Major changes since the last revision

Page or Reference	Description of change
--	First Release

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