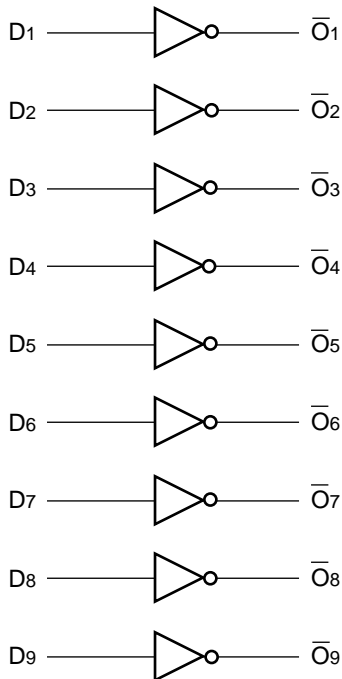


DESCRIPTION

The SY100S321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output.

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 70% faster than Fairchild 300K at lower power
- Internal 75kΩ input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

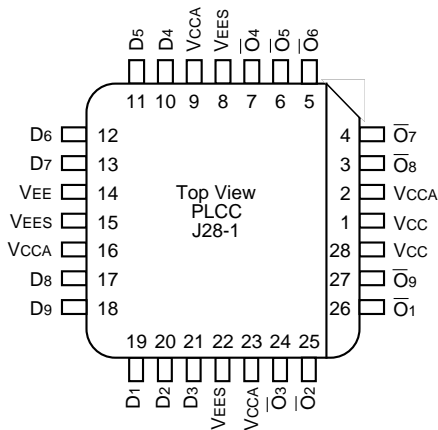
BLOCK DIAGRAM



PIN NAMES

Pin	Function
D1 – D9	Data Inputs
$\bar{Q}1 – \bar{Q}9$	Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S321JC	J28-1	Commercial	SY100S321JC	Sn-Pb
SY100S321JCTR ⁽¹⁾	J28-1	Commercial	SY100S321JC	Sn-Pb
SY100S321JZ ⁽²⁾	J28-1	Commercial	SY100S321JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S321JZTR ^(1, 2)	J28-1	Commercial	SY100S321JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current	—	—	200	μA	$V_{IN} = V_{IH} (Max.)$
I_{EE}	Power Supply Current	-55	-41	-25	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay ⁽¹⁾ Data to Output	300	700	300	700	300	700	ps	
t_{TLH} t_{THL}	Transition Time ⁽¹⁾ 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
$t_s, G-G$	Skew, Gate-to-Gate	—	200	—	200	—	200	ps	

NOTE:

- Reference Figures 1 and 2

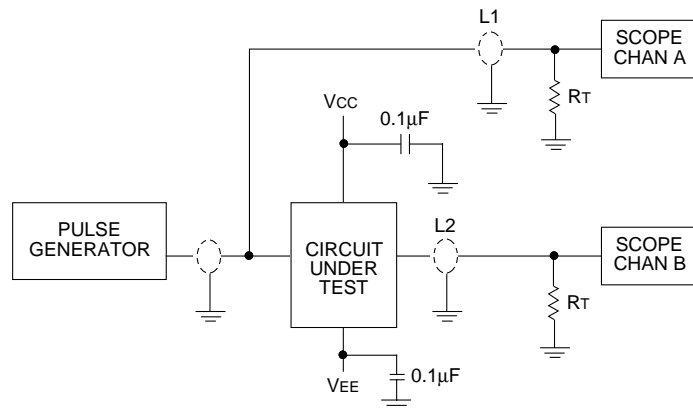


Figure 1. AC Test Circuit

Note:

1. $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$.
 $L1$ and $L2$ = equal length 50Ω impedance lines.
 $R_T = 50\Omega$ terminator internal to scope.
 Decoupling $0.1\mu F$ from GND to V_{CC} and V_{EE} .
 All unused outputs are loaded with 50Ω to GND.
 C_L = Fixture and stray capacitance $\leq 3pF$.

SWITCHING WAVEFORMS

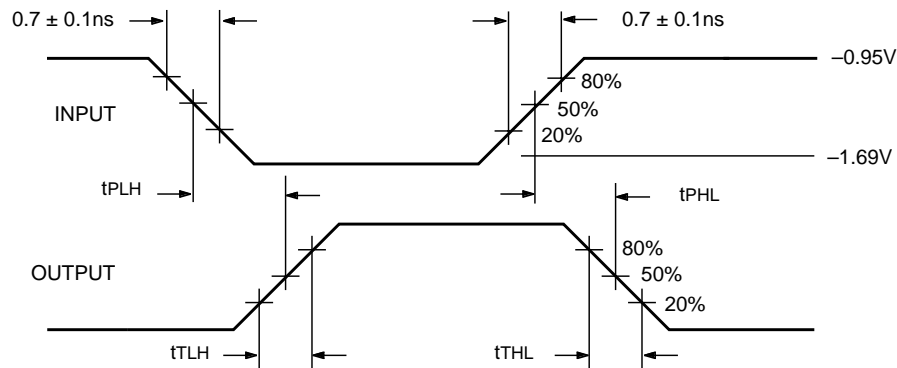
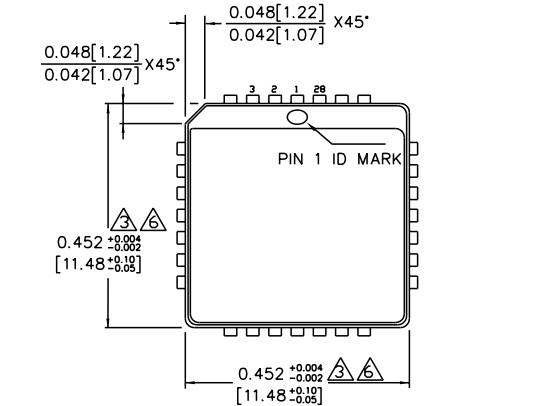


Figure 2. Propagation Delay and Transition Times

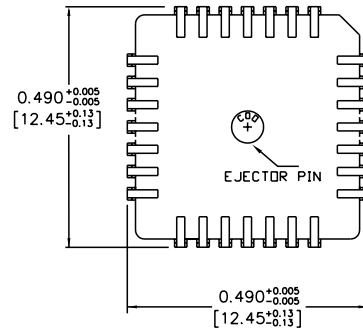
Note:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

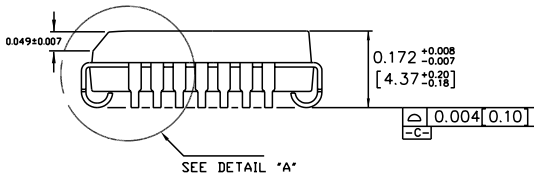
28-PIN PLCC (J28-1)



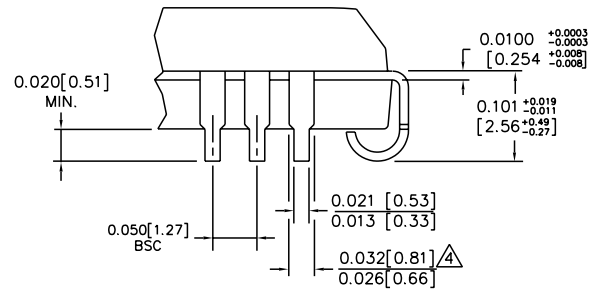
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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